DEVELOPMENT DONE ON DEVICE BONDER TO ADDRESS 3D REQUIREMENTS IN A PRODUCTION ENVIRONMENT

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ABSTRACT

Among competing technologies to shrink the total size of electronic systems, 3D integration incorporating through-silicon-vias (TSV's) is one of the most promising candidates. But despite progress in a number of key process steps, brought about through research efforts conducted at many corporations and institutes and widely reported at technical conferences, cost of ownership remains a major hurdle to adopting 3D integration in high-volume manufacturing (HVM).

Key to the success of 3D integration will be the ability to accurately align and bond devices with aggressive feature sizes. Whether the methodology involves die-to-die, die-to-wafer or even wafer-to-wafer bonding, novel challenges in the areas of bonding metallurgy, materials handling, alignment methods and thermal management must be met simultaneously in order to realize high-performance electronic systems in production.

Through partnerships and equipment installations at several leading research institutes around the world, certain technological advancements have emerged, including:

CEA-LETI, Grenoble, France has presented successful die-to-wafer bonding using 4 µm diameter Au-coated microtubes at 10 µm pitch inserted into pads, as well as a molecular attachment bonding method developed within the Proceed project, Sematech USA and IMEC Belgium have each developed a hybrid collective bonding scheme where accurate die-to-wafer initial bonding is followed by gang bonding to finalize many bonds in parallel,
IME Singapore has developed several solder compositions and methods to create reflow bonding process options.

To realize these and other process options in an HVM environment, the device bonder must incorporate high accuracy placement with high parallelism control at elevated temperatures with high throughput, while accommodating a wide variety of device sizes and thicknesses. Furthermore, many bonding materials will require surface preparation and protection methods either ex-situ, in-situ or both.

This paper will explore the above challenges in 3D HVM and will present solutions and trade-offs using a systems-level approach.

Key words: High precision flip-chip, TSV, 3D integration, HVM

INTRODUCTION

3D Integration is a methodology to increase system density and performance; it has been the subject of numerous projects and publications for several years, with several conferences now dedicated to its exploration.
The initial focus was placed on unit process steps to be used and/or developed and also on tools available from suppliers. A great deal of work has been done to develop and understand the physics and chemistry necessary to increase the density and performance of connections (TSV's, interposers…). It seems that we are now in the phase, announced a couple of years ago, where the cost of ownership starts to be the main focus. What will be the applications which will really launch 3D in production and drive 3D into HVM?

This article will expose different processes explored to meet different requirements of 3D. Then, consequences on the design of production equipment will be discussed.

DEVELOPMENTS DONE

Fine pitch applications

Several papers, since 2009, have been published to explore the possible use of aluminum microtubes to address fine pitch applications, around 10µm, with high-density connections and several millions of bumps. The fabrication of these microtubes, the yield of the electrical connections, the planarity issues of the components themselves and thus the impact on the equipment supporting the components have been reported [1, 2, 3, 4].

Molecular attachment

Another technique, molecular attachment, has been explored for direct copper to copper bonding. It seems also very promising to obtain high density connections for 3D applications. One important advantage is that it is a room temperature process, limiting oxidation of surfaces of metallic layers and minimizing thermal deformations [5, 6]. Other advantages are that no flux is required and process time is short. These characteristics are important for very short cycle time for HVM production. Cleanliness requirements are much more important as this process is very sensitive to particulate contamination. Solutions adapted to the SET FC300 have lowered particle counts at the critical bonding step to acceptable levels; some of these solutions were previously reported. [7] Particulate contamination inside the tool has been reduced thanks in particular to a special cable management and an optimized air flow.

Hybrid collective bonding

For 3D stacking, a die to wafer (D2W) approach presents several advantages (better yield, reduced thermal mismatch, heterogeneous integration…) and one disadvantage compared to wafer to wafer (W2W) approach: it is slower. Some projects have studied the possibilities of hybrid techniques to improve the cycle time. Methods with D2W steps coupled with collective bonding have been explored [8]. Another approach was to use an insertion bonding technique, with recess shape pads to allow the use of a lower process temperature [9].

Solder composition

As throughput may be an issue when stacking several dies on top of each other, solder composition has also been investigated to allow temporary tacking and then a global reflow, still with high electrical connections reliability [10].

All these methods require precise report of components.

TECHNOLOGICAL DEVELOPMENTS DONE ON EQUIPMENT

Equipment involved

Most of the developments reported here have been done on FC300 and FC150 Device Bonders, both from SET.

Stability and precision

Among all parameters involved in such processes, precision and stability of the equipment are some of the key parameters.

Precision tests have been set up using quartz reticles, with chromium verniers. A microscope, dual view, top and bottom, looks alternatively at left and right alignment marks. Analysis of the misalignment between them and a closed loop system with high precision XYTheta stage permit precise alignment of bottom reticle to top reticle. Figure 1 shows the principles of the system.

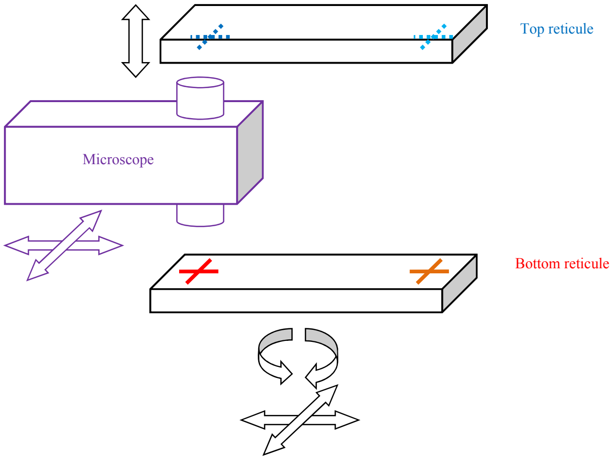


Figure 1. *Schematics of alignment procedure*

The vision system coupled with high resolution optics enables alignment below 0.1 µm, in X, Y and Theta.
Examples of reticles are shown on figure 2.

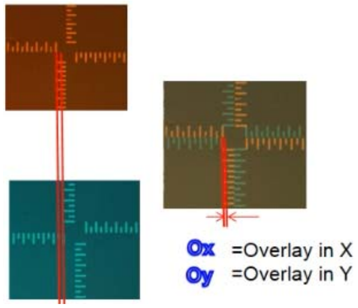


Figure 2. *Precision verification using calibration reticles*

Automatic cycle with all the necessary steps has been created. These steps are: the pick-up of reticles, microscope into alignment position, alignment of reticles, microscope into parking position, search of contact between top and bottom reticles, deposit of the top one onto the bottom one, microscope back again into alignment position, check of the placement accuracy, analysis and recording of positions of alignment marks and repeat again the steps. For this purpose, the duration of each cycle has been set to three minutes and the measurement campaign is pursued during one entire night (typically 14 hours).

Two kinds of measurements have been done, one with both chuck and head (supporting respectively the bottom reticle and the top reticle) at room temperature (typically 21°C in the cleanroom), another one while heating both chuck and head at a temperature of 200°C. The contact force has been set to 100 N (10 kgf).

On the graphs below, we can observe two kinds of curves. Thin ones (on top part of the graph) are temperature measurements done on several locations in the equipment. The purpose is to check for any thermal drift which may influence the stability (induce deformation…). The scale is on the right hand side of the graph, highlighted in pink, unit degrees Celsius.

Bold curves (on bottom part of the graph) show the X and Y errors between top and bottom marks on the left side (point 1) and on the right side (point 2). The scale is on the left hand side of the graph, highlighted in blue, unit micrometers.

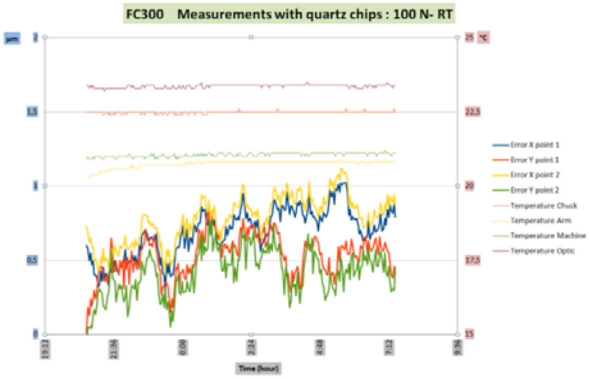


Figure 3. *Repeatability of placement at RT*

We can observe on the figure 3, for RT process, that the recordings of the thermal sensors located in the equipment are very stable, within ± 0.3°C maximum and even better when excluding the warm-up time of the equipment. Stability of the placement accuracy is very good, in the range of ± 0.4 µm.

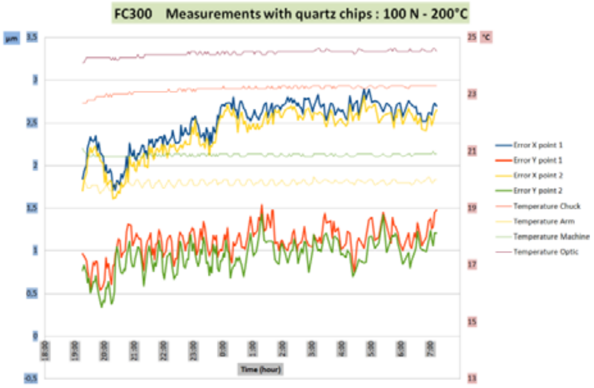


Figure 4. *Repeatability of placement at 200°C*
No change in the machine

We see, in figure 4, for reticules heated at 200°C, that the recordings of the thermal sensors located in the equipment are still quite stable even if the amplitude variation is double, within ± 0.6°C. Here also, results are better if we exclude the warm-up time of the equipment.
Stability of the placement accuracy is still very satisfying, in the range of ± 0.6 µm.

In figure 5, we have imagined to create a perturbation inside the machine. In the morning, around 6AM, we have slightly modified the air flow, creating a small change in the air temperature. This has induced some small temperature changes inside the machine. We clearly can see two "hills" in the curves on the right hand side of the graph. Placement accuracy has increased to ±1µm.

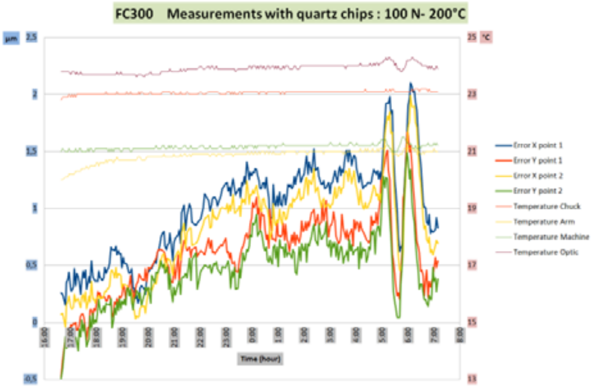


Figure 5. *Repeatability of placement at 200°C*
Change in the machine

Such investigations are now systematically done at SET on any flip-chip bonder. Looking at all the recording curves that have been stored, we observe the trends. One conclusion is environmental contribution is not negligible and even slight changes in the ambient temperature induce some drifts in the final precision. Machine housing and internal airflow are already bringing good results. But we can imagine that if the quality of the cleanroom (stability of the thermal regulation, potentially the one of the pressure…) exhibits high fluctuation of these two parameters, the bonder's housing may be insufficient. Is a real internal enclosure in which the temperature is precisely controlled a solution? Such considerations are in progress and evaluated at SET.

Influence of temperature

To check another influence of the temperature, we have taken the example of a solid part. We have made some theoretical calculations to evaluate the influence of a thermal gradient within a plate on its final shape.

Let take the example of a rectangular plate, total length L and thickness d with a coefficient of thermal expansion (CTE) α.

When both surfaces (and therefore the whole material) are at the same temperature T, the plate is flat.

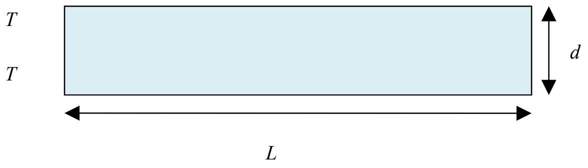


Figure 6. *Side view of a plate at constant temperature*

When one surface is warmer than the other one (T and $T+\Delta T$), a thermal gradient appears in the material. The warmer surface becomes longer than the coolest one, which keeps the same length. The plate is warped.

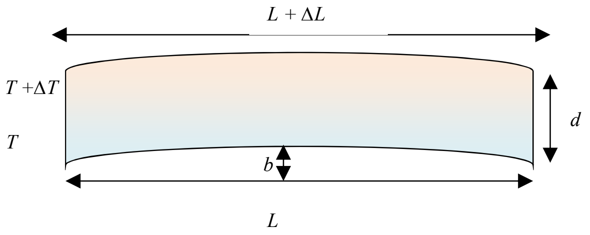


Figure 7. *Side view of a plate at different temperatures*

We assume that the shape is an arc of circle (linear gradient within the thickness, steady state).
The total length of the warmer surface will be:

$$L + \Delta L$$

with

$$\Delta L = \alpha \, . \, L \, . \, \Delta T$$

With geometrical calculations and the approximation of small angles, we obtain a final bending b equal to:

$$b = \frac{\alpha \, . \, L^2 \, . \, \Delta T}{8. \, d}$$

As example, we have made the following calculations for 5 mm thick plates of different materials:

Table 1. *Table of theoretical bending values of a 5 mm thick plate for several materials*

Thickness = d =	5	mm		
ΔT =	10	°C		
Total lenght = L [mm]	Bending = b = [µm]			
Material	Silicium	Steel	Stainless steel	Aluminium
α [ppm/°C]	2,6	11	17	23
10	0,1	0,3	0,4	0,6
20	0,3	1,1	1,7	2,3
30	0,6	2,5	3,8	5,2
40	1,0	4,4	6,8	9,2
50	1,6	6,9	10,6	14,4
60	2,3	9,9	15,3	20,7
70	3,2	13,5	20,8	28,2
80	4,2	17,6	27,2	36,8
90	5,3	22,3	34,4	46,6
100	6,5	27,5	42,5	57,5
110	7,9	33,3	51,4	69,6
120	9,4	39,6	61,2	82,8
130	11,0	46,5	71,8	97,2
140	12,7	53,9	83,3	112,7
150	14,6	61,9	95,6	129,4

This bending is proportional to the CTE of the material, the square of the length and the difference of temperature. Therefore, the equipment is designed with low CTE materials to minimize the differential expansion of various machine components and by managing properly the heat inside the equipment.

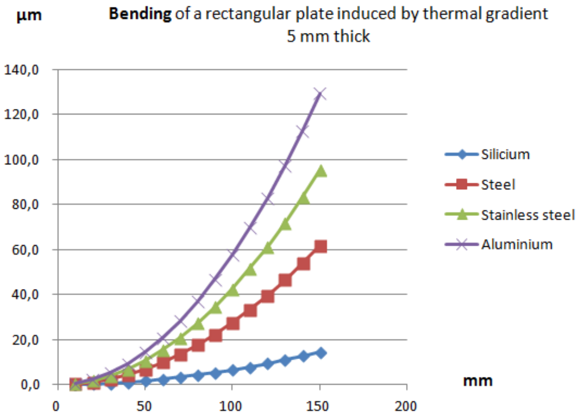


Figure 8. *Graphs of theoretical bending values of a 5 mm thick plate for several materials*

We wish to point out that these theoretical bending values are influenced by the real shape of the parts, presence of holes, pockets, type of machining… Furthermore, thermal expansion (especially in the thickness direction) of the material has also to be taken into account.
Thus, Finite Element Analysis (FEA) with the real design of the parts can be useful.

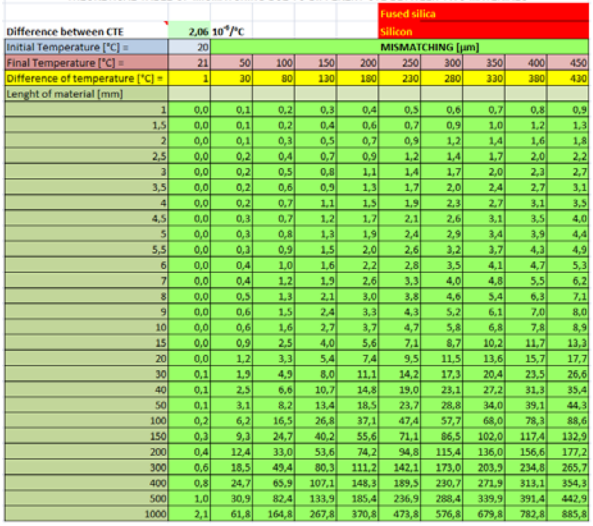
Influence of (non) uniformity of temperature and/or different CTE

Another parameter, also linked to the temperature, is influencing the final precision. It is the difference in CTE among different chip and substrate materials to be bonded together. If the bonding process requires heating of components, a mismatch between them may occur if the coefficients of thermal expansion of their materials are not identical. If the design of both components has been done at RT, the components perfectly fit at RT. While heating, as one is expanding more than the other, a mismatch appears. Final alignment may be difficult, even impossible to achieve. Or a compromise must be done and choose arbitrarily the most appropriate alignment.

As an example, we have chosen fused silica and silicon, materials often used in microelectronics. We have made the assumption that both CTE are constant in the range of interest of temperature. For a thermal difference equal to 30°C, with both designs made at 20°C, a mismatch of up to 6.2 µm can occur between two Ø 100 mm wafers at 50°C.

As heterogeneous integration is almost mandatory, process should be adapted to the materials to be assembled according to their CTE.

Table 2. *Theoretical table of thermal mismatch*



THEORETICAL TABLE OF MISMATCHING DUE TO DIFFERENT CTE BETWEEN TWO MATERIALS										
						Fused silica				
Difference between CTE	2,06	10^{-6}/°C				Silicon				
Initial Temperature [°C] =	20	MISMATCHING [µm]								
Final Temperature [°C] =	21	50	100	150	200	250	300	350	400	450
Difference of temperature [°C] =	1	30	80	130	180	230	280	330	380	430
Lenght of material [mm]										
1	0,0	0,1	0,2	0,3	0,4	0,5	0,6	0,7	0,8	0,9
1,5	0,0	0,1	0,2	0,4	0,6	0,7	0,9	1,0	1,2	1,3
2	0,0	0,1	0,3	0,5	0,7	0,9	1,2	1,4	1,6	1,8
2,5	0,0	0,2	0,4	0,7	0,9	1,2	1,4	1,7	2,0	2,2
3	0,0	0,2	0,5	0,8	1,1	1,4	1,7	2,0	2,3	2,7
3,5	0,0	0,2	0,6	0,9	1,3	1,7	2,0	2,4	2,7	3,1
4	0,0	0,2	0,7	1,1	1,5	1,9	2,3	2,7	3,1	3,5
4,5	0,0	0,3	0,7	1,2	1,7	2,1	2,6	3,1	3,5	4,0
5	0,0	0,3	0,8	1,3	1,9	2,4	2,9	3,4	3,9	4,4
5,5	0,0	0,3	0,9	1,5	2,0	2,6	3,2	3,7	4,3	4,9
6	0,0	0,4	1,0	1,6	2,2	2,8	3,5	4,1	4,7	5,3
7	0,0	0,4	1,2	1,9	2,6	3,3	4,0	4,8	5,5	6,2
8	0,0	0,5	1,3	2,1	3,0	3,8	4,6	5,4	6,3	7,1
9	0,0	0,6	1,5	2,4	3,3	4,3	5,2	6,1	7,0	8,0
10	0,0	0,6	1,6	2,7	3,7	4,7	5,8	6,8	7,8	8,9
15	0,0	0,9	2,5	4,0	5,6	7,1	8,7	10,2	11,7	13,3
20	0,0	1,2	3,3	5,4	7,4	9,5	11,5	13,6	15,7	17,7
30	0,1	1,9	4,9	8,0	11,1	14,2	17,3	20,4	23,5	26,6
40	0,1	2,5	6,6	10,7	14,8	19,0	23,1	27,2	31,3	35,4
50	0,1	3,1	8,2	13,4	18,5	23,7	28,8	34,0	39,1	44,3
100	0,2	6,2	16,5	26,8	37,1	47,4	57,7	68,0	78,3	88,6
150	0,3	9,3	24,7	40,2	55,6	71,1	86,5	102,0	117,4	132,9
200	0,4	12,4	33,0	53,6	74,2	94,8	115,4	136,0	156,6	177,2
300	0,6	18,5	49,4	80,3	111,2	142,1	173,0	203,9	234,8	265,7
400	0,8	24,7	65,9	107,1	148,3	189,5	230,7	271,9	313,1	354,3
500	1,0	30,9	82,4	133,9	185,4	236,9	288,4	339,9	391,4	442,9
1000	2,1	61,8	164,8	267,8	370,8	473,8	576,8	679,8	782,8	885,8

Thermal non-uniformity on either heating chuck or heating head leads to the same kind of mismatch. In the case of large components, or in die to wafer applications, non uniformity in one heating element may induce difference in the thermal expansion of the component itself, with the same consequences as described above.

Influence of process

Looking at these theoretical considerations and also at experimental results, we can foresee that the process used for 3D stacking will influence the design of flip-chip bonders in the race of high precision coupled with high throughput. For R&D equipment, multiple options and configurations are possible. For HVM environment a trade-off will have to be done.

Room temperature processes present the valuable benefits to minimize thermal deformations in mechanical parts (but also in components to be assembled), thermal mismatch between different materials and to improve the cycle time thanks to the lack of ramp-up and cooling times. Oxidation of metallic compounds is also reduced. One such RT process was recently proposed using a binary alloy to create high integrity bonds without temperature excursion [11]. But for some RT processes, high level cleanliness is mandatory. This requirement implies special designs (confinement, choice of adapted materials and air flow management…).

Gluing processes, especially if the glue is UV cured, present also a good alternative. Special care must be brought in case of thermal curing and also in term of cycle time (dispensing time) and cleanliness.

Bonding force is also a parameter which can influence a lot the final precision. The stiffness of the equipment and its sub-modules is a key factor of success. But the behavior of the components themselves and the shape, material and size of the bumps are also influencing a lot the final bonding precision. Reducing the bonding force is obviously a good way to improve final precision, while shortening also the cycle times. Precise control of force and good control of the parallelism between components are already available, but they necessary increase the cycle time.

High temperature processes promote good adhesion between components, but induce collateral effects that must be controlled to maintain sufficient alignment during the hybridization step.

CONCLUSION

This article reports some processes done on high precision of flip-chip bonders, shows their influence on the equipment and describes developments done on them to improve their reliability and stability.

Several effects induced by temperature changes have been studied in particular.

Each type of process has pros and cons, influencing the cycle time and final precision. Thus a trade-off will have to be done. Equipment may have to be dedicated to one specific process, to obtain optimized results.

SET is investigating different scenarios for the design of new equipment, taking into consideration all the items described in this article.

What will be the process(es) used in future 3D applications in a production environment? This will for sure drive new inputs in the developments in the design of high precision and high throughput flip-chip bonders.

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