Pure Chemical Reduction of Tin Oxides to Metallic Tin by Atmospheric Plasma to Improve Interconnection Reflow of Pb-free Solders

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Abstract

Tin alloys are widely used as solder for electronic interconnections. Tin solder surfaces tend to have tin oxides which need to be removed to improve the yield of interconnection reflow processes such as flip chip joining. Conventionally, a strong flux is employed to remove these oxides, however this process has the drawbacks of leaving flux residue which can cause underfill delamination or require a high-cost cleaning process. As solder bump volumes and bump-to-bump spacing decrease, these problems become more difficult to manage in manufacturing. We propose the use of Atmospheric Plasma to reduce these oxides from the bump surfaces to enable the use of very light fluxes, or no flux at all. This process has the advantages of plasma surface preparation without the cost and throughput penalty of vacuum plasma processes. Such a process can increase throughput and yield while reducing the cost. We describe an experiment in which tin foils were treated with a reducing-chemistry Atmospheric Plasma process and then analyzed with X-ray photoelectron spectroscopy (XPS) and Auger Electron Spectroscopy (AES). AES depth profile analyses indicate that the thickness of tin oxides was significantly reduced by the plasma. There was no evidence for any etching of underlying elemental tin. These results suggest that tin oxides are reduced to metallic tin without etching of the underlying tin metal. In another similar experiment using semiconductor chips with SnAg solders, XPS results suggest that the tin oxides were again reduced to metallic tin. In flip chip joining, the joining process with such Atmospheric Plasma-treated chips achieved high interconnect yield, even in the case of poor-quality solder balls with excessive oxidation. It is our understanding that the pure chemical reduction of tin oxides with atmospheric plasma in ambient had not been previously reported.

Key words

Lead-free solder flip chip joining, reduction of tin oxides, atmospheric plasma, and semiconductor interconnection

I. Introduction

Flip chip plastic ball grid array (FC-PBGA) Packages with integrated circuit chips are employed for a wide range of electronic devices such as cellular phones, PCs, communication routers, home electronics, mainframe servers, etc [1]. As shown in Fig. 1, a typical FC-PBGA package consists of BGAs, a laminate substrate (organic chip carrier), controlled collapse chip connection (C4) joints, underfill, a chip, thermal interface material (TIM), and a heatsink [2]. As the density of C4 increases and the size of C4 decreases to enhance the performance, the interconnection becomes more challenging.

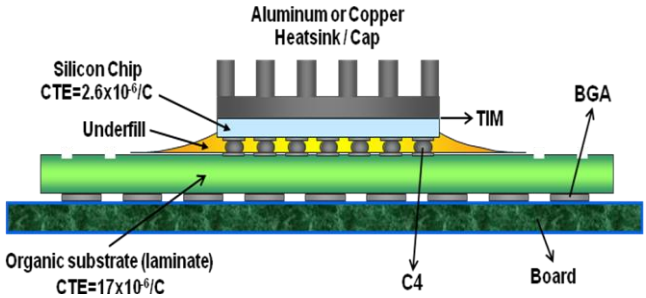

Fig. 1. Flip chip plastic ball grid array (FC-PBGA) package. The chip is interconnected through C4 joints.

Large die flip chip organic packages for high performance computing are facing chip package interaction (CPI) issues [3]. One of the most important issues is a low-k dielectric material crack in the back end of the line (BEOL), which is often called white bump. Mismatch of coefficients of thermal expansion (CTE) between silicon and laminate causes this issue and lead-free solder bumps exacerbate it distinctly due to the hardness of the joint. For an advanced node chip, decrease of dielectric constant in wiring layers is a key trend to enable high speed data transmission. However, such a low dielectric material tends to have fragile mechanical properties. During a bond and assembly process, the thermal shrinkage of the laminate in a cooling stage of chip join reflow and the mechanical damage in post chip join cleaning can make the low-k dielectric materials of the silicon die cracked to result in white bumps. Modeling and experiments showed that the stresses are built up in the cooling stage of the chip join reflow.

In order to reduce the stresses on C4 joints, a concept of in-line underfill has been developed [4], [5]. In the cooling stage of the chip join reflow, underfill material is introduced to the gap between chip and laminate at 100-120 ^{o}C as shown in Fig. 2. Gelling of the underfill at the same or higher temperature in the range of 100-130 ^{o}C would prevent the stresses building up at C4 joints so that formation of white bumps can be prevented. Since it is not easy to clean flux residue at a high temperature, it would be beneficial if the cleaning process is not included in the entire assembly process. For such an approach, a concept of no clean flux (NCFx) has been studied [5] but it seems difficult to formulate a perfect NCFx material that provides perfect wetting, no residue and tackiness (or viscosity).

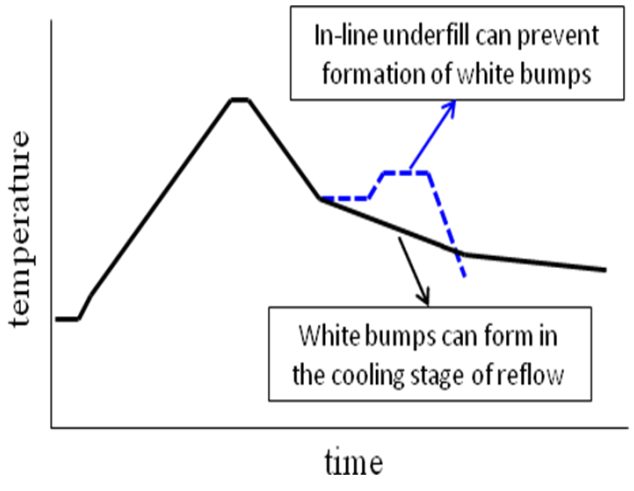

Fig. 2. Concept of in-line underfill. Underfill is applied at a high temperature and gelled to distribute the stresses on C4 joints so as to prevent formation of white bumps.

As the density of Controlled Collapse Chip Connection (C4) arrays and the chip size increase, the joining process sometimes produces non-wets at a corner of the large chip due to the smaller C4 size and the larger warpage of a substrate. We have learned that Pb-free solders are more difficult to be joined than leaded ones and that plated Pb-free solders are more difficult to be joined than C4NP Pb-free ones [6]. It also becomes more difficult to clean flux residue, formed during flip-chip joining, out of the narrow chip-substrate gap of the large chip package. Non-wets which make electrical open should be avoided, and flux residue often causes delamination between underfill and chip or between underfill and substrate, resulting in failure of flip-chip packages.

Pb-free solder balls in a wafer level tend to have a range of tin oxide layers as well as tin oxide particles at their surfaces. A relatively strong flux can make such solders melt and joined in a reflow process but it tends to leave flux residue which is typically cleaned after the reflow. However, such a strong flux cannot be employed as a NCFx since it leaves residue which causes delamination of underfill from the chip surfaces. If the tin oxides at the solder ball surfaces can be reduced prior to a chip join reflow process, a relatively mild NCFx can be employed for the in-line underfill.

Here we report on the reduction of tin oxides or Pb-free solder balls with atmospheric plasma, an automated process of which can be applied to a manufacturing process without much difficulty. We also investigated typical flip chip joining with 2D hardware.

II. Experiments

A. Atmospheric Plasma Surface Treatment

Recent developments in the field of atmospheric plasma equipment [7], [8] have produced an atmospheric plasma head which is capable of running a reducing chemistry (hydrogen-based) through a dielectric barrier plasma region within the head, and through a linear aperture to supply a uniform source of downstream hydrogen radicals to a chip or wafer surface placed below the aperture and under room-ambient conditions (no vacuum system). Fig. 3 is a schematic representation of the cross-section of the plasma head, showing gas flow from top to bottom of the head, transiting the plasma region. The downstream radicals produced in the plasma region have sufficient lifetimes to exit the aperture and react with the chip or wafer substrate below. The outward flow of gas between the plasma head face and the substrate purges all room atmosphere from the reaction zone, creating a pristine controlled environment for the radical reactions with the surface.

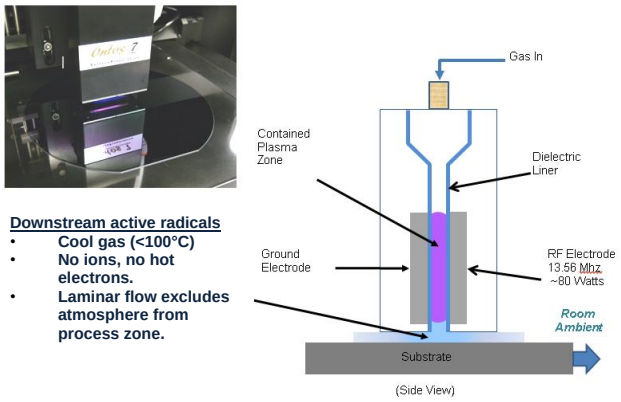

Fig. 3. Atmospheric plasma head (schematic representation)

The major advantage of the atmospheric plasma system is the ability to treat surfaces on a continuous throughput basis without the time-consuming and expensive steps involved with conventional vacuum systems. The substrate (die or wafer) is simply translated below the plasma head linear aperture by a conveyor or similar, in open air. Additional benefits include the fact that the plasma is remote from the substrate, and therefore the substrate is not subjected to high-energy ions or hot electrons which could damage highly sensitive circuitry or semiconductor devices. The plasma gas mixture is non-toxic and non-flammable, and thus it is simply collected by normal clean room exhaust systems.

B. Reduction of tin oxides on tin foils

Tin foils were purchased from Sigma-Aldrich and were cut into 10 mm × 10 mm coupons, which were cleaned with acetone and then 2-propanol to remove gross contamination left by foil production and handling. Ellipsometer readings were made on the Sn coupon surface to establish a baseline measurement of the oxide residing on the surface. Two different types of foil samples were processed – one with only native oxides accumulated since foil production; and another which had received forced oxide growth through a temperature and humidity stress (85 ºC, 85% RH, 24 hr). The Sn coupons then received treatment with the Atmospheric Plasma system, employing the reducing chemistry (inert carrier gas + ~1% hydrogen). A scan rate over the chip surface was 1.0 mm/second, and the gap between chip and plasma aperture was set at 1.0 mm. Low plasma power was utilized to slow down the surface reactions and enable time-phased measurement of the evolution of the surface oxide back to Sn metal. Ellipsometer readings were taken after each scan of the atmospheric plasma, and the raw "Δ" value from the ellipsometer was plotted as a function of scan number.

Fig. 4 shows the evolution of the Sn foil surface as the unforced native oxide is reduced back to pure metal. (Note: lower Δ readings signify thicker oxide; increasing Δ readings signify less and less oxide on the metal surface.)

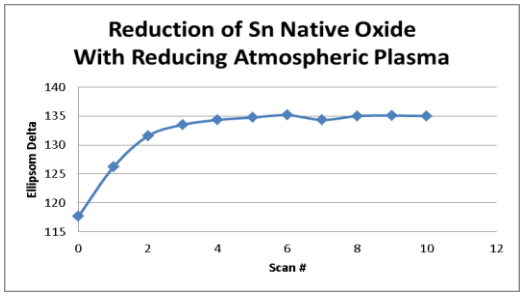

Fig. 4. Ellipsometer tracking of SnOx reduction using Atmospheric Plasma treatment with reducing chemistry (higher Delta signifies thinner SnOx surface film).

At this low plasma power, it appears that 5-6 scans are sufficient to reduce the surface back to metallic Sn. A higher plasma power will accomplish the same in 1-2 scans.

The forced-oxide foils had a much thicker oxide to enable accurate XPS measurements by eliminating the background XPS return from underlying Sn metal. These samples received 3 times the number of scans as the native oxide samples in order to produce a measurable depth of reduced surface.

Following the atmospheric plasma treatment, the samples were packaged in Fluoroware containers, sealed inside aluminum-coated bags, and purged with nitrogen. The samples were then shipped by overnight delivery to IBM for surface analysis.

C. Treatment of bad chips with the reducing chemistry atmospheric plasma

Silicon chips with known-bad SnAg bumps were treated with Atmospheric Plasma to reduce the surface tin oxides in order to improve bonding quality. These chips received the same atmospheric plasma surface treatment as described above. The treated chips were shipped by overnight delivery to IBM for chip assembly.

A commercial flux was applied onto a laminate followed by placing and aligning a chip. The chip-laminate module went through a typical reflow process with its peak temperature of 245 ºC. The chip-joined modules were then cleaned with DI water at 80 ºC and 65 psi. The cleaned modules were inspected with X-ray using a Nikon XTV-160 machine for any C4 defects such as bridges and micro solder balls.

III. Results and Discussion

A. Reduction of tin oxides on tin foils

To prove the reduction of tin oxides, we first investigated an analysis technique with X-ray photoelectron spectroscopy (XPS) since a 24-hr delay between plasma treatment at SETNA and XPS analysis at IBM is expected. A chip was diced out of a wafer which was purposely processed to yield a relatively thick layer of tin oxides. As shown in Fig. 5a, XPS shows only peaks corresponding to SnOx but no peaks due to metallic tin. Ar sputtering at 150 W under 30 mTorr for 2 min etched off some SnOx to reveal metallic tin [Sn(0)]. XPS in Fig. 5b shows new peaks due to Sn(0). This treated chip was left in ambient for 48 hr and analyzed the surface again. As shown in Fig. 5c, the intensity of Sn(0) peaks decreased but still distinguishable. This experiment proves that an XPS analysis within 48 hr after the reducing chemistry atmospheric plasma treatment would reveal the bands due to Sn (0) if SnOx were reduced by the plasma.

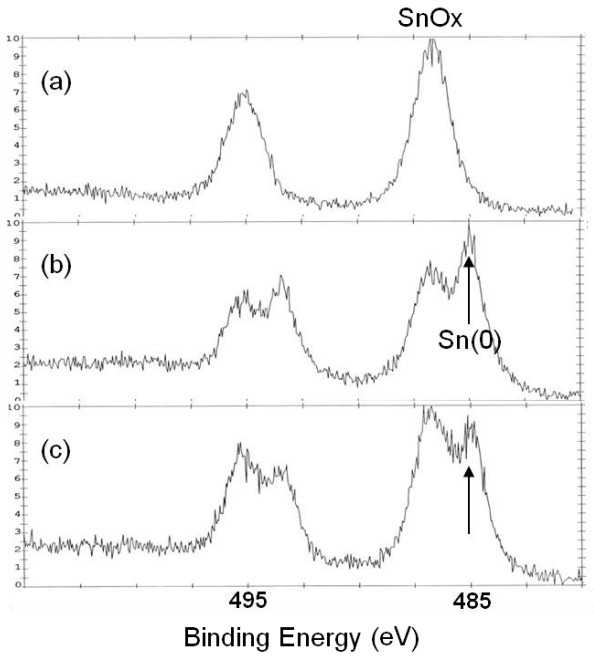

Fig. 5. XPS Sn3d bands: (a) Solder balls of a chip with a relatively thick layer of SnOx; (b) Treated with Ar sputtering (150 W, 30 mTorr, 2 min) to etch off SnOx; (c) 48-hr in air after the Ar sputtering.

Tin foils are known to have a thick layer of SnOx at their surfaces. Such tin foils were treated with the reducing chemistry atmospheric plasma at SETNA and then analyzed after 24 hr of the plasma treatment. XPS in Fig. 6b shows the bands due to Sn(0), indicating that SnOx layers were reduced to Sn(0). An AES depth profile in Fig. 7 indicates that the thickness of SnOx was reduced from approximately 10 nm to approximately 2 nm which looks like native oxides formed in air after the plasma treatment. Angle-resolved XPS shows that the surface is enriched with SnOx as expected.

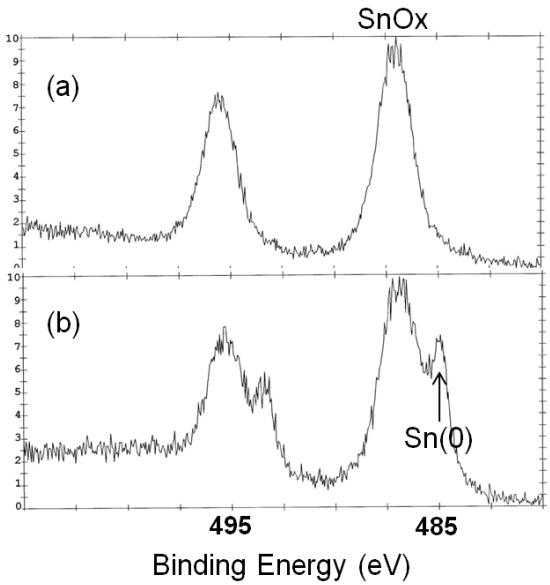

Fig. 6. XPS Sn3d bands: (a) Tin foils and (b) treated with the reducing chemistry atmospheric plasma at SETNA.

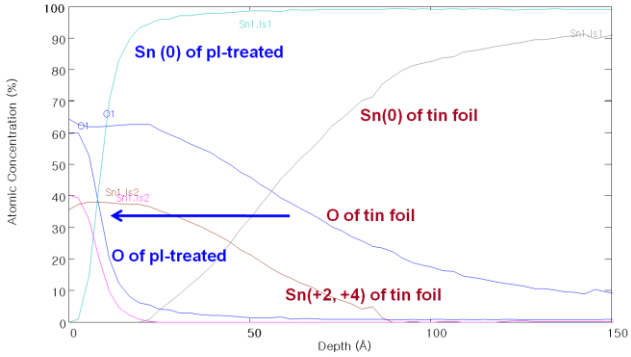

Fig. 7. AES depth profile of tin foils. The atoms from a tin foil are labeled with red letters while the atoms from the tin foil treated with the reducing chemistry atmospheric plasma with blue letters.

It is reasonable to hypothesize that, as illustrated in Fig. 8, the entire layer of SnOx was reduced by the reducing chemistry atmospheric plasma treatment and then native oxides were formed in ambient during the delay between plasma treatment and analysis.

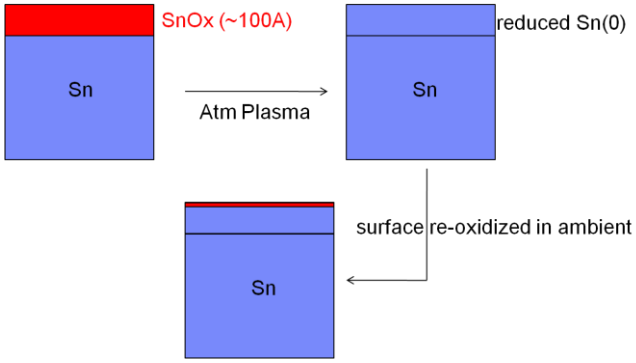

Fig. 8. Proposed reaction scheme of tin foils. Atm plasma means a reducing chemistry atmospheric plasma.

B. Flip chip joining with the chips treated with the reducing chemistry atmospheric plasma

Typical solder balls of a semiconductor chip in production tends to have 1-2 nm thick SnOx which does not cause any non-wets. As the size of a chip increases to enhance the performance, the number of solder balls increases. A very small number of solder balls sometimes have lumps of SnOx which can cause formation of post solidification deformation (PSD), bridges or micro solder balls as shown in Fig. 9. To ensure a perfect interconnection in flip chip joining, bad chips with a relatively thick layer of SnOx and/or SnOx lumps were prepared in a wafer-level process. Such chips were employed in the development of flip joining processes for the purpose of abundant precaution in the production of semiconductor packages, especially for mainframe servers.

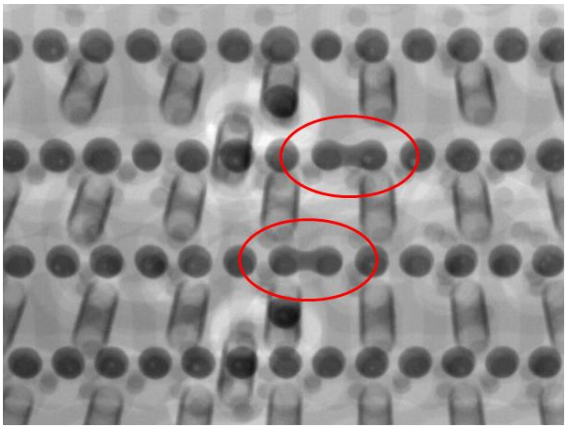

Fig. 9. Bridges were formed from a chip join reflow process with a bad chip and a mild flux. Treatment of such bad chips with the reducing chemistry atmospheric plasma decreased the defect level from 83% to 14%.

In a series of experiments with more than 100 packages with the bad chips and a relatively mild flux, approximately 80% showed defects of PSDs, bridges and/or micro solder balls. The defects can be prevented with a relatively strong flux but the strong flux left a flux residue.

Seven chips from the same wafer batch of the bad chips were treated with the reducing chemistry atmospheric plasma treatment. After a 24-hr delay, the treated chips were joined to laminates with the same mild flux. The level of defects decreased from 83% to 14%. The modules with 83% defects have multiple PSDs or micro solder balls but the module with 14% defects has only one micro solder ball. This result indicates that the reducing chemistry atmospheric plasma treatment decreased the level of SnOx so as to reduce the level of defects even with the bad chips.

It is noted that our one-time attempt for fluxless flip chip joining with the reducing chemistry atmospheric plasma did not produce a good joining result and that we have not pursued any further experiment even though the fluxless soldering technology is quite attractive [9], [10].

IV. Conclusion

Tin oxides at the surfaces of tin foils or tin-containing solders are chemically reduced to metallic tin by the reducing chemistry atmospheric plasma, by which no etching of metal or metal oxides occurs. The atmospheric plasma enables known-bad chips joined to a substrate and it also helps employ a relatively mild flux so as to leave no or less flux residue than untreated chips.

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