Alternative Approach to Die-to-Wafer Bonding Utilizing Atmospheric Plasma Cleaning

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Extended Abstract

This paper presents an alternative approach for direct placement die-to-wafer bonding without the reliance on a carrier wafer, tailored specifically for hybrid bonding, 3DIC, and integrated photonics applications. Die-to-wafer bonding stands as a pivotal process in heterogeneous, vertically integrated device fabrication, often involving the intermediary step of placing individual dies onto a carrier or handle wafer before integration onto the target wafer. This conventional method adds cost, complexity, potential compatibility issues, and process steps. In this study, we propose a streamlined process eliminating the need for a carrier wafer, thereby simplifying integration, and reducing fabrication steps. Leveraging atmospheric plasma cleaning, we clean and activate the surfaces of both the die and the target wafer to facilitate direct placement bonding. Through experimental validation, we demonstrate the feasibility and efficacy of this approach. Our results showcase successful die-to-wafer bonding with minimal interface contamination and enhanced bond strength. Furthermore, we explore the influence of atmospheric plasma cleaning parameters on bond quality, providing insights for process optimization. This research offers a promising alternative for die-to-wafer bonding, advancing the efficiency and simplicity of vertically integrated circuit fabrication, particularly in the domains of hybrid bonding, 3DIC, and integrated photonics applications.

Introduction

Die-to-wafer integration represents a fundamental step in the fabrication process of vertically integrated circuits, marking the convergence of various semiconductor components and materials onto a single substrate. In this intricate process, individual dies, each containing specialized functionalities such as logic, memory, or photonics properties, are strategically integrated onto a target wafer. This allows for heterogeneous integration and the use of known-good die for maximum yield. [1-3]

Die-to-wafer integration serves as a cornerstone for emerging technologies such as 3D integrated circuits (3DIC) and hybrid bonding. In 3DIC architectures, the vertical stacking of dies enables dense integration of components, offering superior performance and functionality compared to conventional 2D designs. Hybrid bonding techniques further expand the capabilities of die-to-wafer integration by enabling the integration of disparate materials, such as silicon and III-V compounds, in a seamless manner.

Furthermore, die-to-wafer integration fosters heterogenous integration by enabling the stacking of dies with diverse functionalities onto a single substrate. This integration paradigm facilitates the combination of specialized components optimized for distinct tasks, leading to enhanced system performance and functionality. For instance, integrating photonic components alongside traditional electronic circuits enables the development of advanced systems for telecommunications, sensing, and optical computing.

Conventional methods for die-to-wafer bonding, however, often involve attaching individual dies onto a carrier wafer before integration onto the target wafer, which introduces additional processing steps and

potential contamination issues. In this study, we propose a streamlined process that eliminates the intermediate carrier wafer, thereby simplifying the integration process and reducing fabrication complexity.

Die-to-Wafer Bonding Processes

Carrier wafers are commonly used in die-to-wafer bonding processes to facilitate handling of individual dies during the cleaning and plasma activation steps before integration onto the target wafer (Fig. 1A-B). This is because the cleaning and vacuum plasma systems typically require work pieces to be in wafer form, not individual dies. The long process time required to pump down and vent vacuum plasma systems also necessitate batch processing for increased throughput.

While the use of carrier wafers is currently the mainstream approach, it also comes with many drawbacks, including additional processing steps and cost, increased risk of contamination, and limited design flexibility. Of course, there is the cost of designing and producing the carrier wafers and temporary bonding materials. Utilizing a carrier wafer adds extra processing steps to the fabrication process, including attaching the dies to the carrier wafer, aligning the dies, bonding them, and later detaching them from the carrier wafer. Each additional step increases fabrication time and complexity, adding to higher costs. Introducing a carrier wafer into the fabrication process can also increase the risk of contamination, particularly if the bonding process involves the use of temporary bonding materials. Contamination from the bonding materials can negatively impact device performance, reliability, and yield. The use of a carrier wafer imposes constraints on the design and layout of the integrated circuit, as the placement and alignment of the dies must conform to the dimensions and specifications of the carrier wafer. Furthermore, in the case of collective bonding, die thickness must be closely matched so that uniform force is applied during the bonding process.

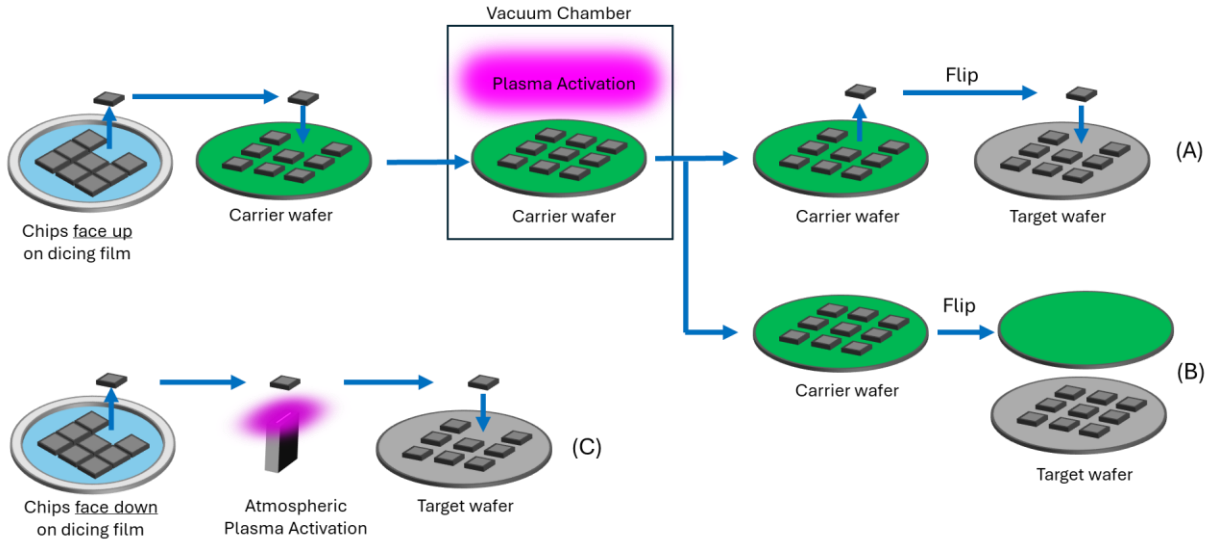

Figure 1: Die-to-wafer bonding approaches: (A) Sequential bonding with carrier wafer. (B) Collective bonding with carrier wafer. (C) Direct placement without carrier wafer, utilizing atmospheric plasma activation, enables a simple process flow.

To avoid all these challenges, we propose the approach of direct placement of dies onto the target wafer utilizing an innovative atmospheric plasma system (Fig. 1C) so that devices may be treated individually or in wafer form. Atmospheric plasma does not require a vacuum chamber to pump down and can be easily installed inline within die-to-wafer bonding equipment to plasma clean and activate individual die just before bonding (Fig. 2). Stand-alone atmospheric plasma systems can also replace vacuum plasmas for

treating whole wafers before loading into the bonder. Whole wafer treatment is achieved by raster scanning the entire wafer surface.

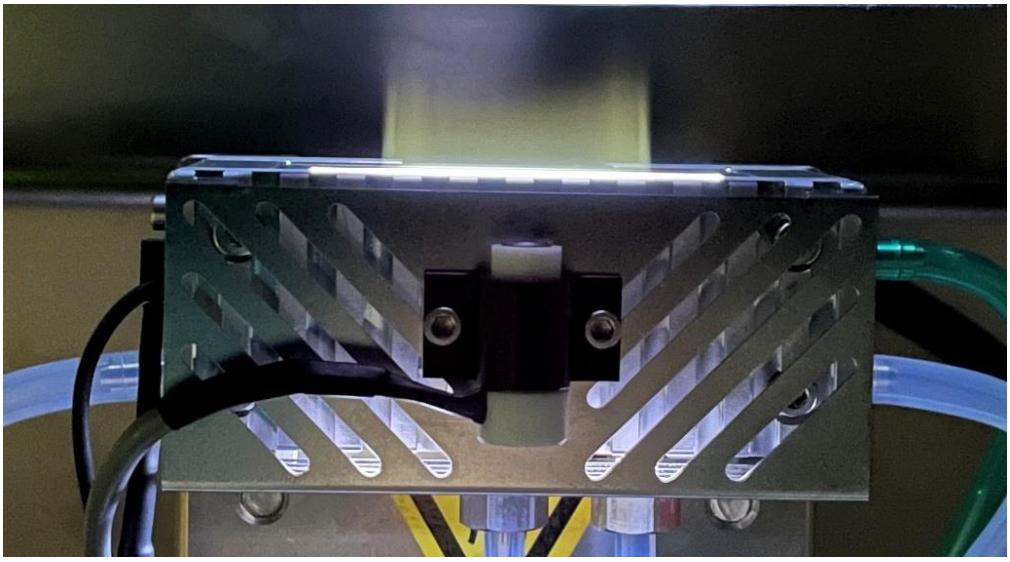

Figure 2: Atmospheric plasma head with plume exiting from the top. Dies are passed over the plume for plasma cleaning and activation just prior to bonding onto the target wafer. Plasma is created in ambient atmospheric pressure, no vacuum chamber required. Plasma plume is 40mm wide in this example.

Using the much simpler direct placement approach, we demonstrate its feasibility by bonding multiple dies onto target wafers (Fig. 3). The ability to produce plasma at atmospheric pressure (i.e. outside of a vacuum chamber) makes this approach possible. Prior work by our research group has shown significant cleaning of die even after contacting surface with various dicing films and gel materials. [4]

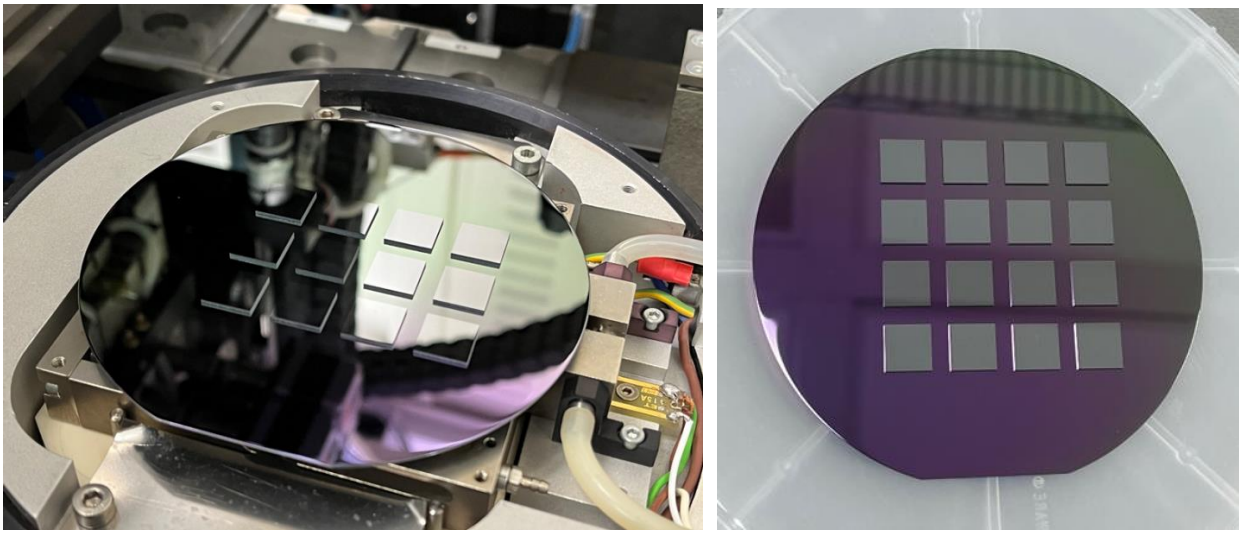

Figure 3: Examples showing results of direct placement of multiple dies onto target wafer (100mm) utilizing atmospheric plasma activation.

Conclusion

Atmospheric plasma enables a streamlined process that eliminates the intermediate carrier wafer, thereby simplifying the integration process and reducing fabrication complexity. Atmospheric plasma is employed to activate the surfaces of both the die and the target wafer, promoting adhesion and enabling direct placement integration. We demonstrate the feasibility and effectiveness of this approach through experimental validation of bonding multiple dies onto target wafers with good adhesion. Furthermore, we will explore the influence of atmospheric plasma parameters on bond quality and device performance, providing insights for process optimization. This research presents a promising alternative approach for die-to-wafer bonding of integrated photonics devices, offering a simplified and efficient pathway towards the realization of vertically integrated hybrid bonding, 3DIC, and integrated photonics applications.

References

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