1st Workshop on Indigenization of Strategic Technologies: Government, Stakeholder and Think tank's perspectives (IST:GST)

IIT Bombay, Mumbai - 400076

Professor Subhananda Chakrabarti

SET Corporation

SMART EQUIPMENT TECHNOLOGY

*

FLIP-CHIP ASSEMBLY FOR FOCAL PLANE ARRAY

omscientific

Pascal METZGER, PhD, CEO

OUTLINE

- Presentation of SET
- Wavelengths
- Applications
- Materials
- Flip-chip assembly
- SET experience and solutions
- Conclusion

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Paris
3h by train

Lyon
1h30 drive

Geneva
40 min drive

Chamonix
Mont-Blanc
50 min drive

Annecy
45 min drive

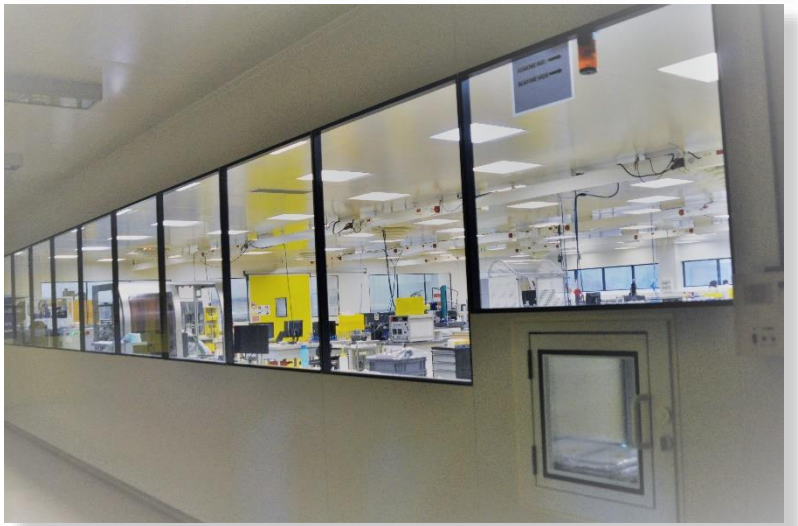
Grenoble
(CEA-Leti)
1h45 drive

DIGITAL GRENOBLE
FRENCH TECH IS ON THE WAY

set
Smart Equipment Technology

SET Corporation AT A GLANCE

- **Since 1975: Equipment for semiconductor** celebrating 40 years in 2015!
- **1981: 1st flip-chip bonder** installed at **CEA-Leti**
- SET former Device Bonder division of **SÜSS MicroTec** (1993-2007)
- SET focuses on **designing**, **assembling** and **selling high precision "flip-chip" bonders**
- **Installed base > 280 Flip-Chip Bonders** all around the world
- **Total surface of facilities** **2 600 m²**
  Clean rooms surface (ISO 7, 6 and 5) **700 m²**



PARTNERSHIPS & COLLABORATION

Member of **SEMI**

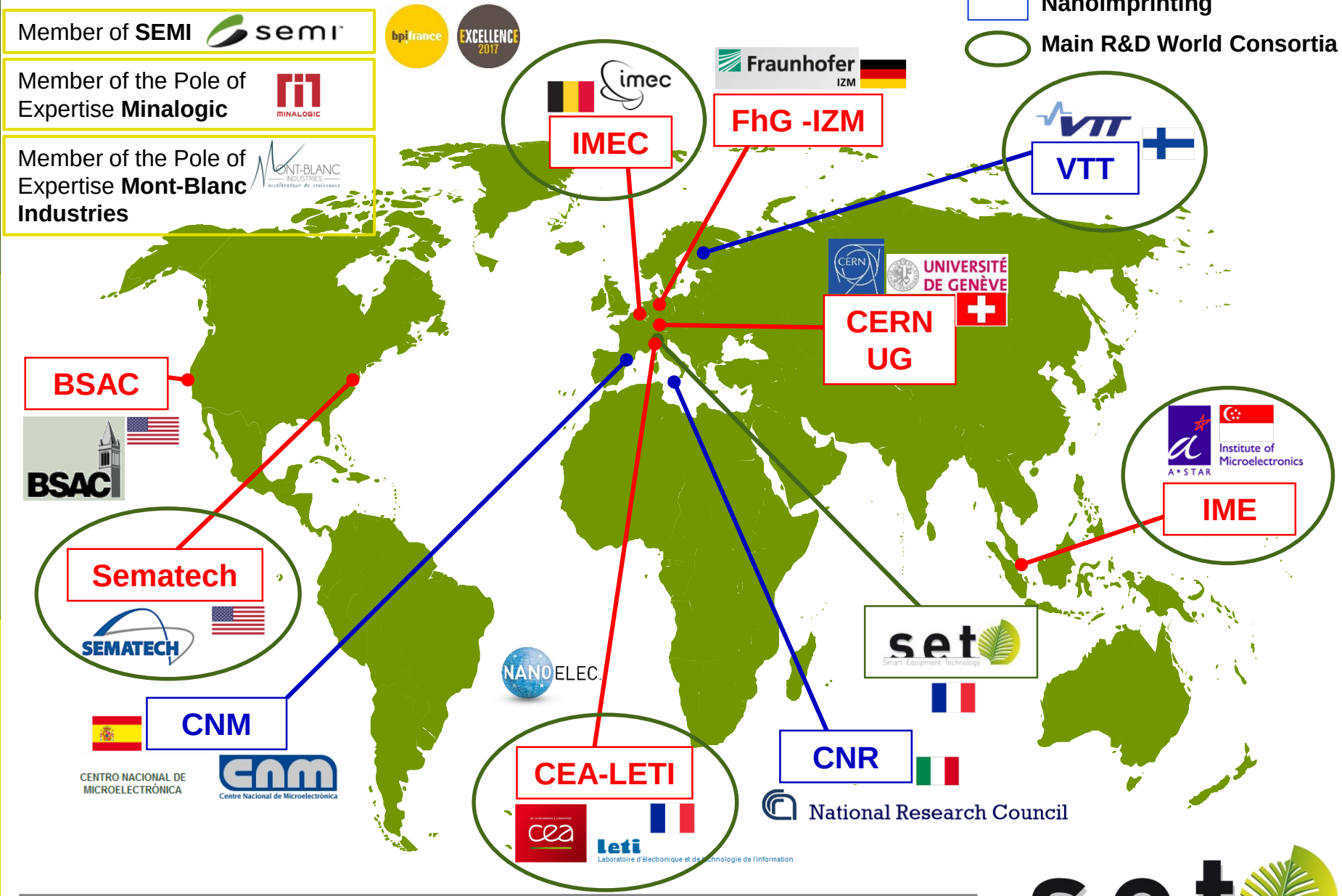
Member of the Pole of Expertise **Minalogic**

Member of the Pole of Expertise **Mont-Blanc Industries**

Die Bonding

Nanoimprinting

Main R&D World Consortia



Main CONFERENCES and EXHIBITIONS for 2017

- **European 3D Summit**, Grenoble, January
- **Semicon Korea**, Seoul, February
- **IMAPS**, Scottsdale, March
- **Semicon China***, Shanghai, March
- **SSI**, Cork, March
- **EXPO Electronica**, Moscow, April
- **SMT***, Nuremberg, May
- **MiNaPAD**, Grenoble, May
- **ECTC**, Las Vegas, June
- **Nordic Conference**, Gothenburg, June
- **Semicon West**, San Francisco, July
- **Semicon Taiwan**, September
- **CIOE**, Shenzhen, September
- **EMPC**, Varsaw, September
- **European Imaging & Sensors Summit**, Grenoble, September
- **NEPCON**, Hanoi, September
- **IWLPC**, San Jose, October
- **Semicon Europa*** (/Productronica), München, November
- **IST:GST**, Mumbai, November
- **Semicon Japan**, Tokyo, December
- **IWPSD**, New Delhi, December

EUROPEAN 3D SUMMIT
23-25 Jan 2017 • Grenoble, France

SEMICON KOREA

IMAPS International Microelectronics Assembly and Packaging Society

SEMICON China

smartsystemsintegration
International Conference and Exhibition

E·X·P·O ELECTRONICA

smthybridpackaging
System Integration in Micro Electronics

MiNaPAD Forum 2017
5th Micro Nano-Electronics Packaging and Assembly
May 17-18 2017 - WTC GRENOBLE France

ECTC 2017
IEEE Electronic Components and Technology Conference

SEMICON WEST
SMART STARTS HERE

SEMICON TAIWAN
Sept 13-15, 2017
Taipei Nangang Exhibition Center
Taipei, Taiwan

CIOE CHINA INTERNATIONAL OPTOELECTRONIC EXPO

EMPC 2017
21st EUROPEAN MICROELECTRONICS AND PACKAGING CONFERENCE (EMPC) & EXHIBITION
WARSAW UNIVERSITY OF TECHNOLOGY
POLAND, SEPTEMBER 10th TO 13th 2017

EUROPEAN IMAGING & SENSORS SUMMIT
20-22 SEP 2017
GRENOBLE FRANCE

NEPCON Vietnam 2017

SEMICON EUROPA
Nov 14-17, 2017
Messe München
Munich, Germany

IWLPC
International Wafer-Level Packaging Conference
Silicon to Systems
October 24 - 26, 2017
DoubleTree by Hilton San Jose
San Jose, California, USA

SEMICON JAPAN

IWPSD 2017
XIX International Workshop on The Physics of Semiconductor Devices

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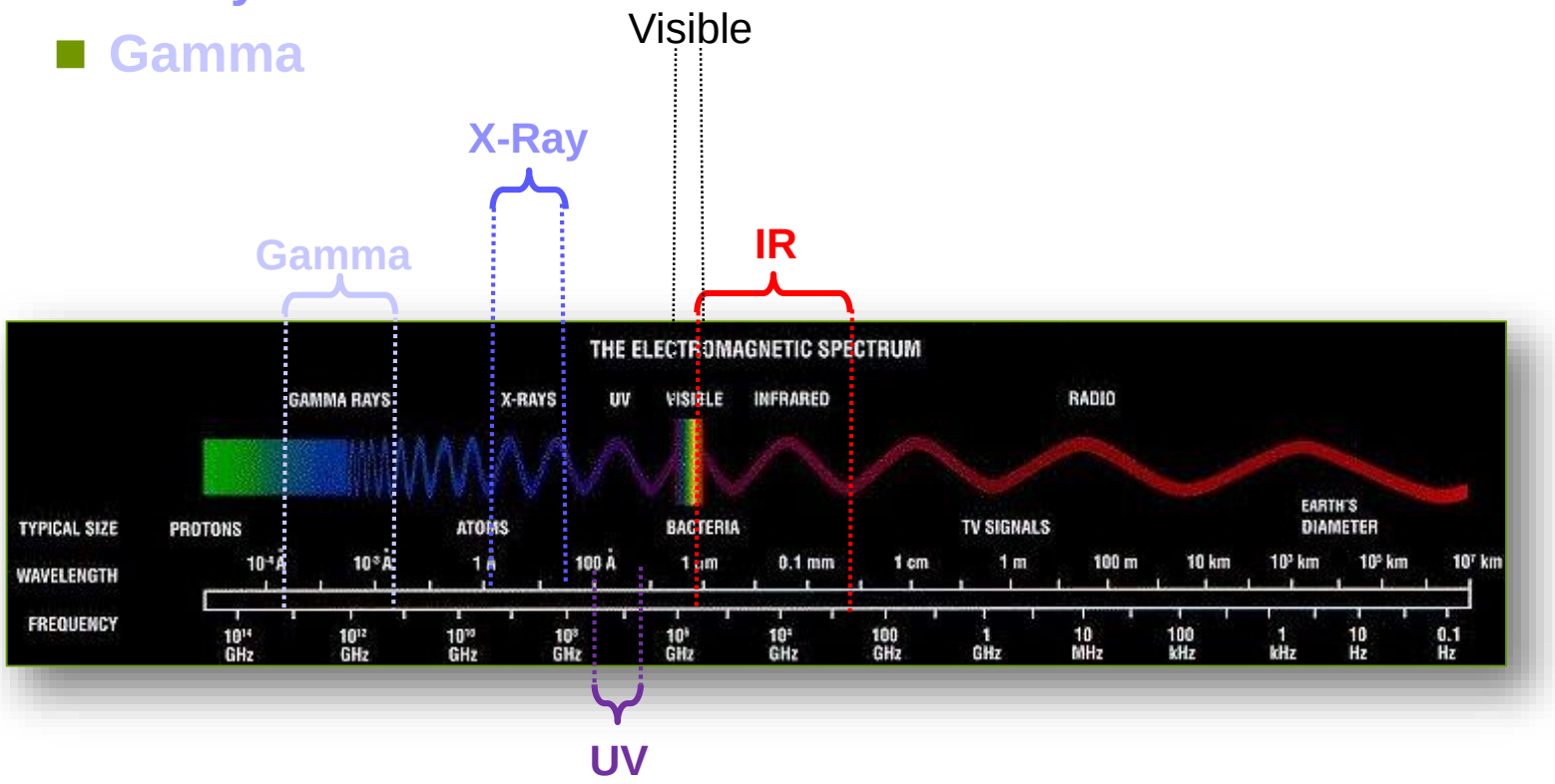
WAVELENGHT

- FPA can detect different wavelengths:
  - Infrared
  - UltraViolet
  - X-Ray
  - Gamma



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SOME APPLICATIONS

- **Infrared is the radiation of heat energy, related to the temperature of objects**

Visible image **Infrared image**

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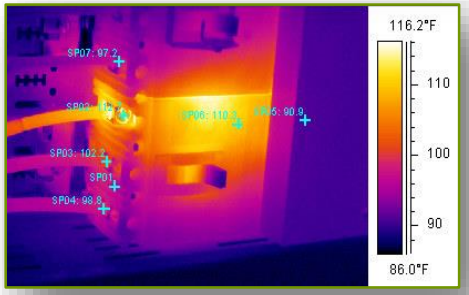
INFRARED APPLICATIONS

Strategically important applications
Restricted technology
Available to few countries/companies

Monolithic

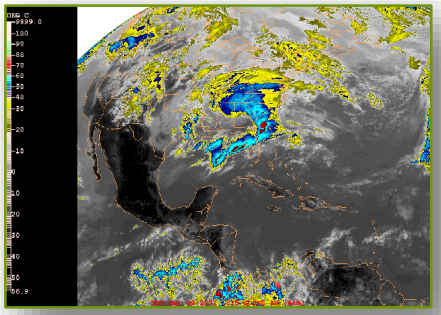
Energy conservation



Industrial

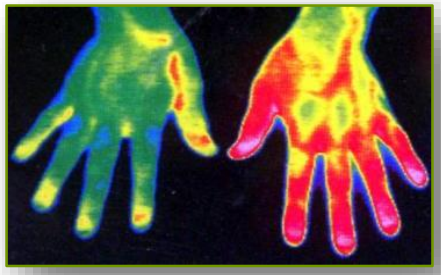
Automotive Night Vision

DC + ROIC



Weather Satellites

Space / Astronomy



Medicine

Military Night Vision

Security/Law Enforcement

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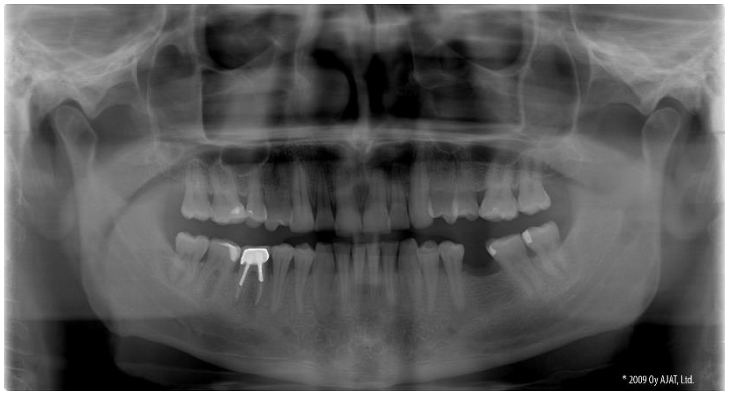
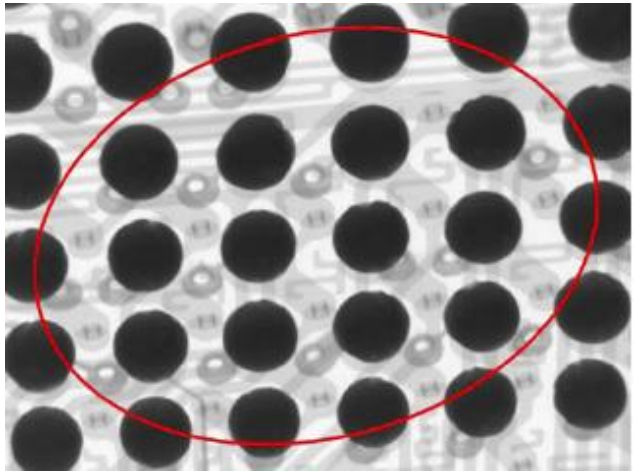
X-RAY APPLICATIONS



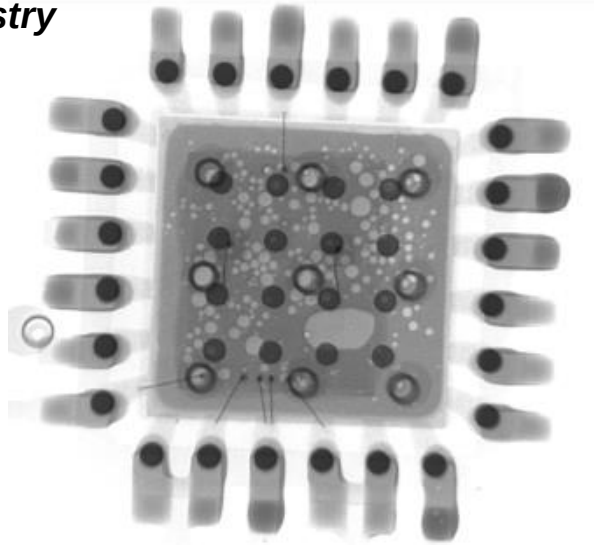
Medical

- **Cameras for dentist/medical applications**
- **In the industry for assembly analysis**

Industry



Shorted vias in a 3D package



Voids on a glued BGA

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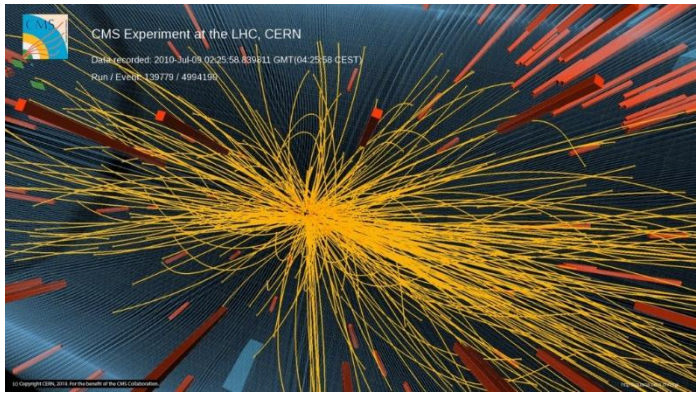
GAMMA and UV APPLICATIONS

Research



CERN (Switzerland): Higgs boson

- **Research for scientific experiments**
- **Aerospace applications to give higher inspection capacities**

Aerospace

Andromeda galaxy (UV picture)

Andromeda galaxy (visible light picture)

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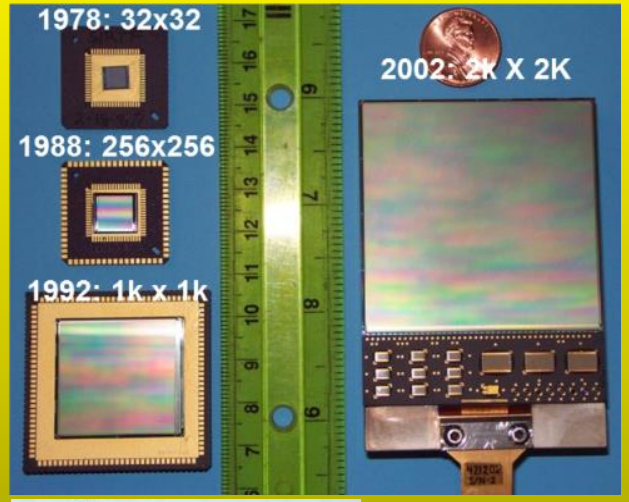
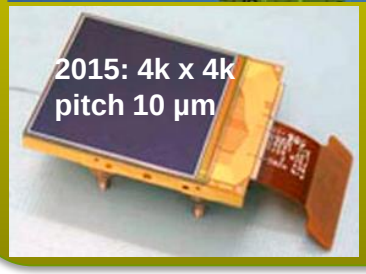
DETECTOR MATERIALS and WAVELENGTH SENSITIVITIES

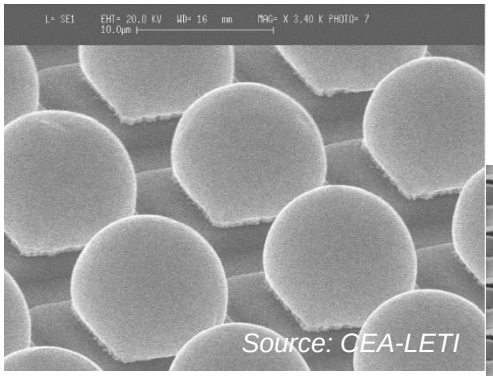
Detector material	Short-Wave IR λ: 1.4-3 µm	Mid-Wave IR λ: 3-8 µm	Long-Wave IR λ: 8-15 µm	Cost
InGaAs (Indium-Gallium-Arsenide)	X			€
InSb (Indium-Antimonide)	X	X		€€
Bolometer		X	X	€-€€
QWIP, SLS, Q-dot		X	X	€€€€
HgCdTe (Mercury-Cadmium-Telluride)	X	X	X	€€€€

FPA DETECTORS and BUMPS

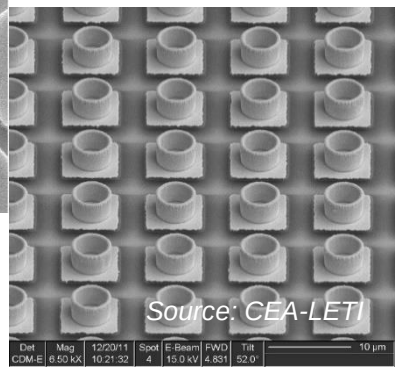




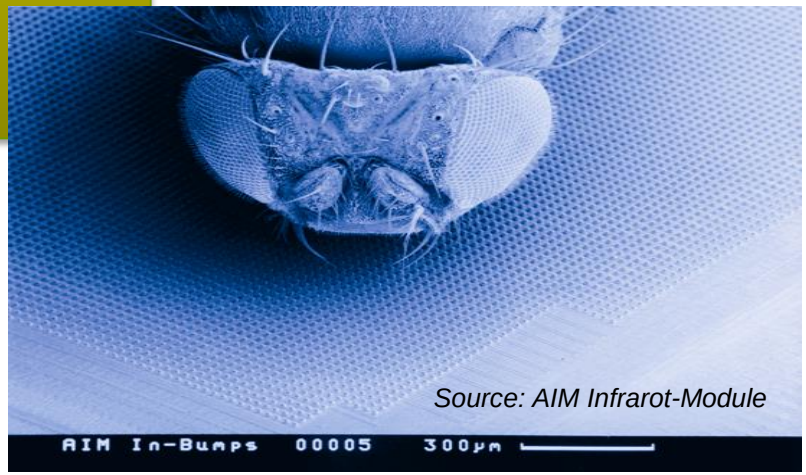
IR detectors



Reflow indium bumps (15 µm pitch)



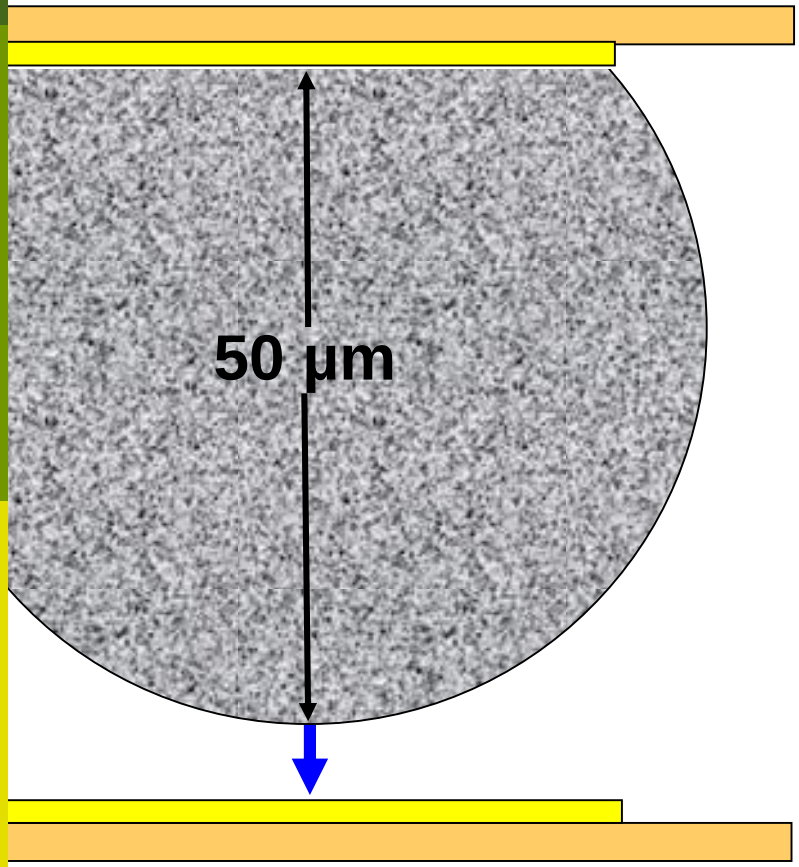
Microtubes (10 µm pitch)



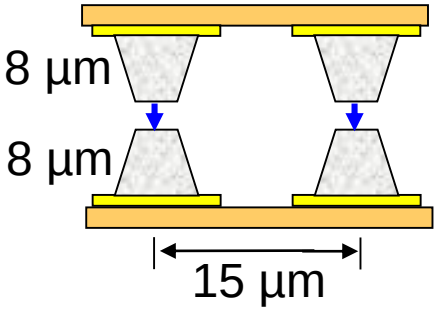
Joint shaping on indium bumps (15 µm pitch)

FLIP-CHIP BUMPS

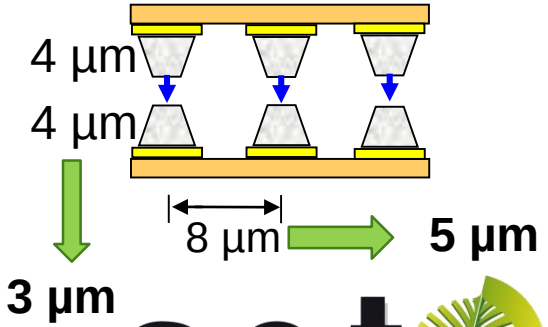
Conventional flip-chip solder ball



Indium-bumped FPA today



Indium-bumped FPA tomorrow



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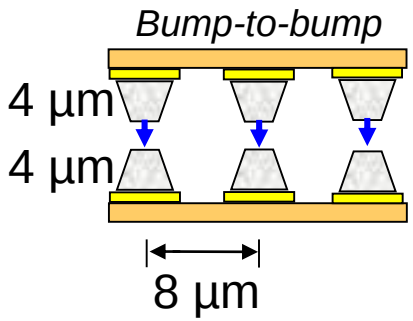
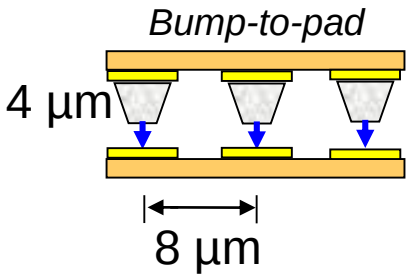
FPA CHALLENGES: SMALLER PIXEL & BUMP SIZE

- **2 different approaches: Bump-to bump** and **bump-to-pad**





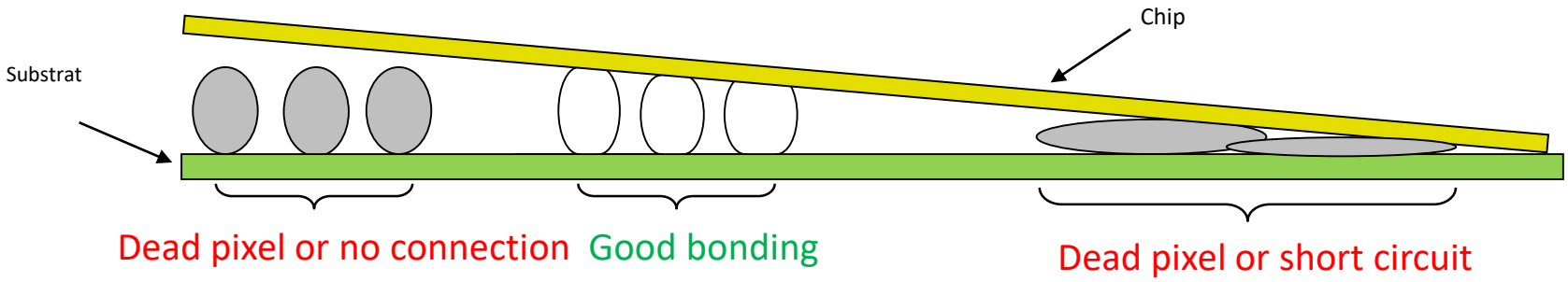
- **Very important for FPA:**
  - Sub-micron alignment in XYΘ,
  - Guaranty parallelism,
  - Deal with strong oxide layer on tiny indium bumps.

//

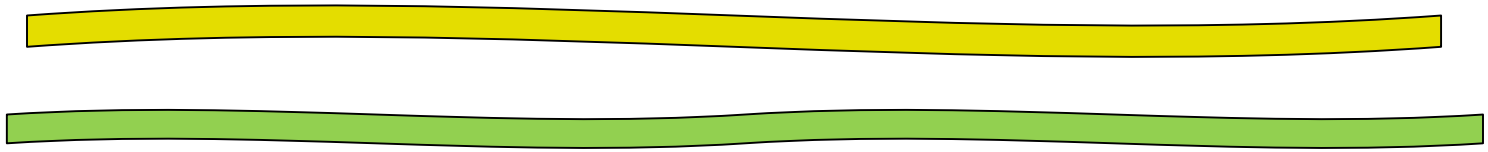
Smart Equipment Technology

FPA CHALLENGES: SMALLER PIXEL & BUMP SIZE

- **Parallelism constraints**
  - // - Flatness



  - // - Waviness



FLIP-CHIP ASSEMBLY

- **Several techniques:**
  - Thermo-Compression or Room Temperature Compression
  - Tacking + Reflow in Oven (under controlled atmosphere)
  - In-situ Reflow with Chemical Flux
  - In-situ Reflow with Mechanical Scrubbing
  - In-situ Reflow with Formic Acid Vapor

FLIP-CHIP ASSEMBLY
Thermo-Compression or Room Temperature Compression

REQUIRES:

- **High accuracy** for alignment and parallelism
- **High pressure/force** linked to size/number of bumps
- **Sensitive and accurate force control** from touch-down, up to final force
- **High stiffness of bonder** to maintain alignment and parallelism accuracy when applying force
- **Good management of temperature** to control the thermal expansion during bonding

Note: Oxide is broken when applying the force.

- **Pros: Low temperature process (even room temperature)**
- **Cons: Oxide residues stay in the indium bumps**

FLIP-CHIP ASSEMBLY
Thermo-Compression or Room Temperature Compression

STATUS

- **4kx4k pixel arrays = Current state-of-the-art**
- **6kx6k pixel arrays = Being attempted now**
- **Larger arrays = Coming**

FLIP-CHIP ASSEMBLY
Tacking + Reflow in Oven

REQUIRES:

- **High accuracy** for alignment and parallelism
- **Chemical flux** to prevent oxidation
- **Sensitive and accurate force control** from touch-down, up to final force
- **External oven (under controlled atmosphere)**

- **Pros:**
  - **Low force tacking**
  - **Many assemblies reflowed simultaneously → Higher throughput**

- **Cons:**
  - **Delicate transfer from bonder to oven → Can affect alignment**
  - **After reflow, flux must be cleaned → Difficult process because small gap between the dies**

FLIP-CHIP ASSEMBLY
In-situ Reflow with Chemical Flux

REQUIRES:

- **High accuracy** for alignment and parallelism
- **Chemical flux** to prevent oxidation
- **Sensitive and accurate force control** from touch-down, up to final force
- **Good management of temperature** to control the thermal expansion during reflow
- **Pros:**
  - **Components secured during the entire process**
  - **Oxide easily removed**
  - **Quality of indium joint very good**
- **Cons:**
  - **Dispense of chemical flux is not a clean process**
    → Not compatible with high accuracy bonder
  - **After reflow, flux must be cleaned**
    → Difficult process because small gap between the dies

FLIP-CHIP ASSEMBLY
In-situ Reflow with Mechanical Scrubbing

REQUIRES:

- **High accuracy** for alignment and parallelism
- **Sensitive and accurate force control** from touch-down, up to final force
- **Good management of temperature** to control the thermal expansion during reflow
- **Mechanical scrubbing system** which respects the high alignment accuracy

Note: Oxide is broken when applying the force.

- **Pros:**
  - **No post bond cleaning because no flux**
- **Cons:**
  - **Oxide residues stay in the indium bumps**
  - **Difficulty to keep the alignment accuracy after scrubbing**

FLIP-CHIP ASSEMBLY
In-situ Reflow with Mechanical Scrubbing

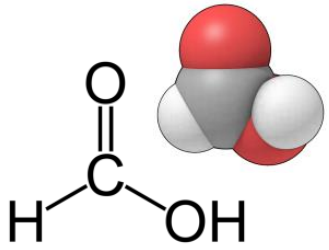
STATUS

- **Reflow of FPAs up to 1kx1k has been demonstrated** using chemical flux or mechanical scrubbing to break through indium bump oxide skin

- **However, larger arrays would require more scrubbing force which is not compatible with the high alignment accuracy** required by tiny bumps and small pitches

- **Large arrays have also their own thermal expansion (≠ CTE between Detector and ROIC) → Mismatch at high temperature**

FLIP-CHIP ASSEMBLY
In-situ Reflow with Formic Acid Vapor



REQUIRES:

- **High accuracy** for alignment and parallelism
- **Sensitive and accurate force control** from touch-down, up to final force
- **Good management of temperature** to control the thermal expansion
- **Gas control (formic acid vapor)**

- **Pros:**
  - **Oxide is easily removed**
  - **Quality of indium joint is very good**
  - **No post-reflow cleaning**
  - **Formic acid cleaning offers a good surface preparation to flow the underfill material**
- **Cons:**
  - **Long desoxidation process (2 to 4 minutes typical)**

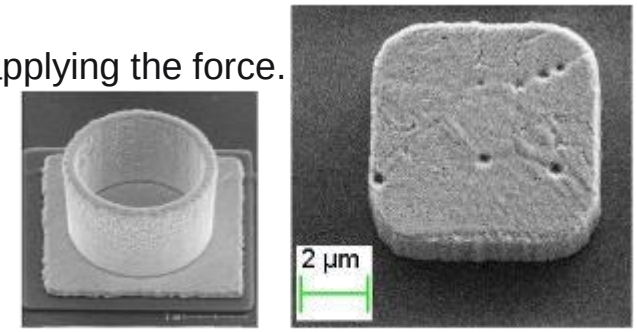
FLIP-CHIP ASSEMBLY
Microtubes

REQUIRES:

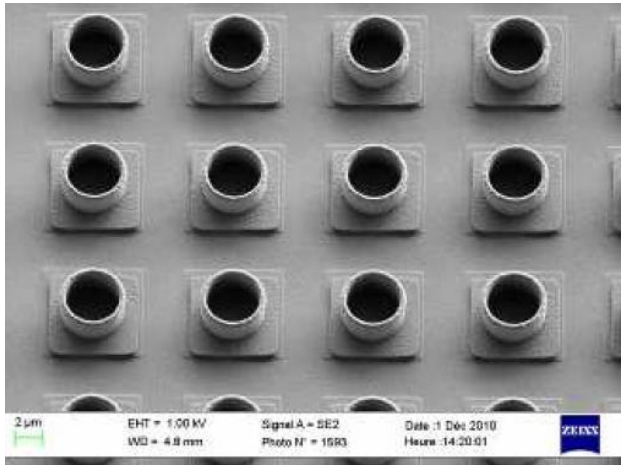
- **High accuracy** for alignment and parallelism
- **Sensitive and accurate force control** from touch-down, up to final force
- **CEA-Leti's patent on technique to develop the microtubes** before assembly

Sources illustrations: CEA-LETI

Note: Oxide is broken when applying the force.



4µm diameter micro tube (left) and ductile pad (right)



- **Pros:**
  - **Low temperature process (even room temperature)**
- **Cons:**
  - **Oxide residues stay in the interconnection**
  - **Requires a patent (royalties)**

FLIP-CHIP ASSEMBLY
Some references

REFERENCES

[1] F. Marion *et al.*, "Electrical characterization of high count, 10 µm pitch, room temperature vertical interconnections" IMAPS International Conference on Device Packaging March 9-12, 2009

[2] B. Goubault de Brugière, F. Marion *et al.*, "A 10µm Pitch Interconnection Technology using Micro Tube Insertion into Al-Cu for 3D Applications", Electronic Components and Technology Conference, May 31st - June 3rd, 2011

[3] F. Marion *et al.*, "Aluminum to Aluminum Bonding at Room Temperature", Electronic Components and Technology Conference, May 28–31, 2013

[4] A. Bedoin *et al.*, "Micro-tube insertion into aluminum pads: Simulation and experimental validations", IMAPS 2013, September 30 - October 3, 2013

[5] L. Sanchez *et al.*, "Chip to wafer direct bonding technologies for high density 3D integration", Electronic Components and Technology Conference, May 29 - June 1, 2012

[6] Y. Beilliard *et al.*, "Chip to wafer copper direct bonding electrical characterization and thermal cycling", 3DIC October 2-4, 2013

[7] K. Cooper et al., "Process and Equipment Enhancements for C2W Bonding in a 3D Integration Scheme, IWLPC Oct. 5-7, 2011.

[8] D. Pascual *et al.*, "Thin die interconnect process for 3DIC utilizing multiple layers of 50 µm thick dies on 300 mm wafers with a tack and collective bonding approach for manufacturability", IWLPC November 5-7, 2013

http://www.set-sas.fr/en/tp1-Technical-papers.html

Technical papers

Focus on bonding | Focus on nanoimprinting | Conference proceeding | NIL technology

Technical papers: Focus on bonding!

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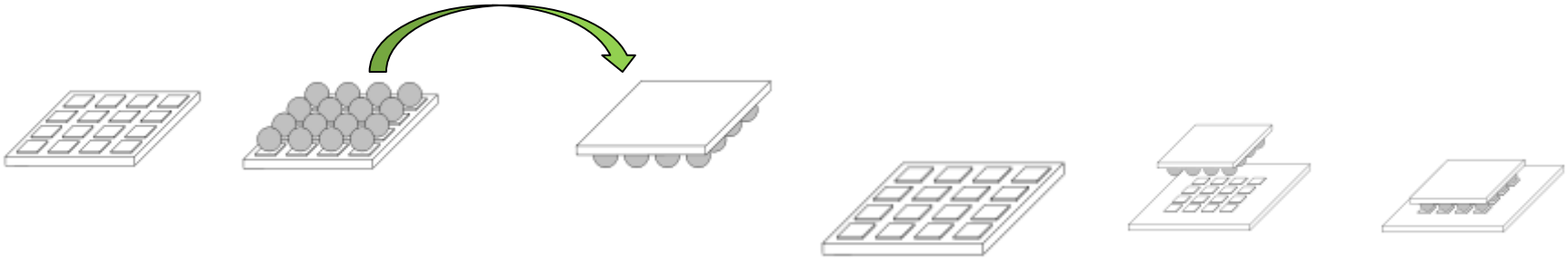
SET EXPERIENCE AND SOLUTIONS

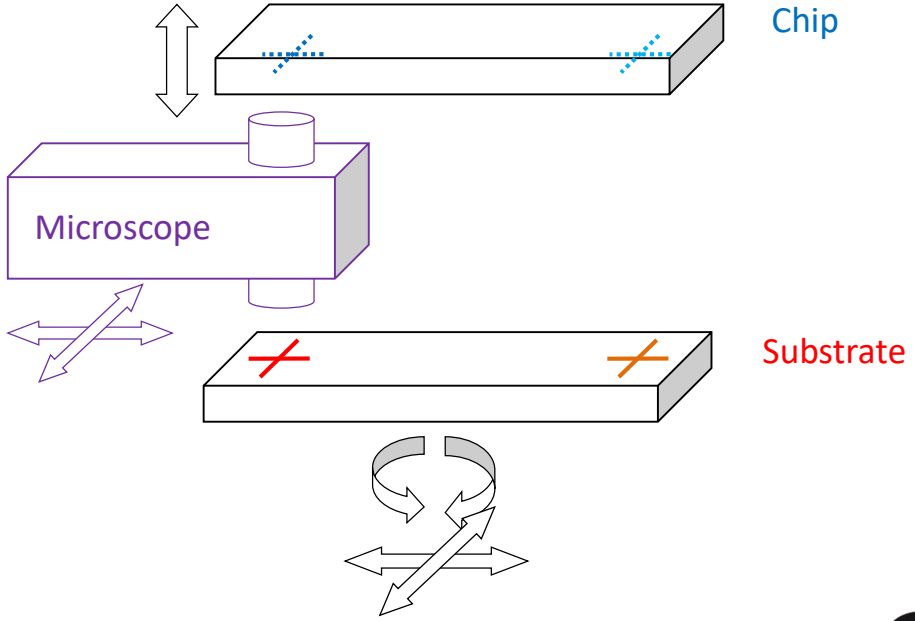
- **1975: Creation of the company (42 years ago)**
- **1982: Beginning of flip-chip with Reflow + Flux techniques with CEA-Leti (35 years experience in flip-chip)**
- **1990's: Development of high force / room temperature solutions in collaboration with American private companies**
- **2008: Introduction of formic acid vapor solution, qualified by several important names of FPA manufacturers in the world**
- **2010: CEA-Leti technique with microtubes developed on SET Bonder**

SET SOLUTIONS PRINCIPLES

- **Flip-Chip technology**



- **General architecture of SET bonders**



set Smart Equipment Technology

SET SOLUTIONS
R&D BONDER FC 150
Flip-Chip Bonder

- **Bumps pitch down to 15 µm**
- **± 1 µm post-bond accuracy**
- **Force from 25 to 200 kgf**
- **Temperature up to 450°C**
- **High Process Flexibility:**
  - Thermo-compression
  - Room temperature compression
  - Reflow
  - Formic acid vapor
- **Automatic mode for production**

SET SOLUTIONS
R&D BONDER FC 300
Flip-Chip Bonder

- **Bumps pitch down to 5 µm**
- **± 0,5 µm post-bond accuracy**
- **Force from 100 to 400 kgf**
- **Temperature up to 450°C**
- **High Process Flexibility:**
  - Thermo-compression
  - Room temperature compression
  - Reflow
  - Formic acid vapor
  - Force control / Z control
  - Higher stifness
- **Automatic mode for production**

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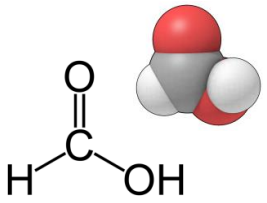
SET SOLUTIONS
Oxide removal with formic acid vapor



- **Unique concept based of semi-open chamber with injection of formic acid vapor**
- **All vapors are exhausted for safe use**
- **Formic acid vapor is built-in thanks to an evaporator**
- **Allows to:**
  - Remove oxide on bumps
  - Shape the bumps
  - Generate a good adhesion indium-to-indium bumps
  - Get a good diffusion of indium bumps on gold pads
- **Additional benefit:**
  - Get better flow of underfill

SET SOLUTIONS
Parallelism

- **Actually, 3 (optical) possibilities to measure parallelism**
  - Autocollimator:
  - Laser leveling:
  - Optical sensors :

SET SOLUTIONS
LARGE DEVICE PRESS LDP 150

Large Device Press

When arrays become very large (i.e. 4kx4k)
→ Very high force is required at room temperature

Detector and ROIC are aligned and pre-bonded on FC150 or FC300
→ Then LDP150 applies the remaining pressure.

- **XY accuracy is maintained within 3 µm**
- **Parallelism is maintained**
- **Self levelling system**
- **Force up to 100 kN (10,000 kgf)**
- **Room temperature**

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OUTLINE

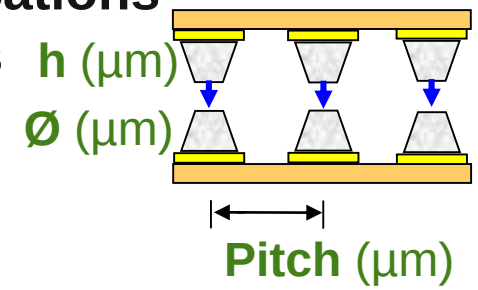
- Presentation of SET
- Wavelengths
- Applications
- Materials
- Flip-chip assembly
- SET experience and solutions
- **Conclusion**

CONCLUSION

- **Strategic FPAs market growing**

- **Challenges very well identified:**
  - Array size increasing → Higher bonding force required
  - Pixel size shrinking → Higher bonding accuracy required

- **Flip-chip method to be chosen:**
  - **According** to constraints of **final products/applications**
  - **Size** and **Pitch** of the **bumps** are **key parameters**



- **To get a good FPA:**
  - Flip-chip assembly must be **accurate**
  - Bonder must **flexible** to run all these different techniques on the same platform, from R&D to production purposes.

Thank you for your attention

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