

Evaluation of Sn-based Microbumping Technology for Hybrid IR Detectors, 10 μ m Pitch to 5 μ m Pitch

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Abstract

Hybridization of Infrared detectors has relied on Indium balling for the last decades. Whereas this well-established process has proven its reliability through out the years, it becomes challenging to further decrease the balling pitch below 10 μ m, due to balling volume limitation.

In this study we developed a wafer level bumping process for 10 and 5 μ m pitch Sn microbump. Different test materials with 10 and 5 μ m pitch Sn microbumps were processed to mimic 1024 X 768 (XGA) and 3072 X 3072 pixels formats respectively.

We show that the 10 μ m pitch assemblies can undergo successfully 960 cycles between room temperature and cryogenic temperature, meeting stringent reliability requirements of such device. On the pitch scaling side, we show that initial 5 μ m pitch microbumps have been successfully fabricated, assembled and underfilled. The observed failure modes are discussed.

Introduction

Hybrid detectors rely on the heterogeneous stacking of Si Read Out Integrated Circuit (ROIC) and other narrow band gap materials sensitive in the infrared wavelengths. Such components are susceptible to operate at cryogenic temperature and the dissimilar Coefficient of Thermal Expansion (CTE) are extremely challenging for the assembly and for the reliability of the component. So far Indium interconnects have proven to meet the necessary requirement for such applications. However, in order to achieve a higher spatial resolution, the number of pixel needs to be increased. Indium based balling, usually involves lift-off processes that inherently limit the interconnect density and poses manufacturing challenges for large bump arrays, and overall manufacturing yield.

In this study, we evaluated the use of microbumps consisting of Cu, a Ni barrier layer and Sn finish as a potential replacement of indium, for pitch inferior to 10 μ m. Sn based microbumps have been reported to have electromigration (EM) lifetimes similar to or greater than low melting point bumps such as PbSn [1,2] and their potential for fine pitch scaling has been frequently investigated in a recent past [3].

As pitch decreases, the challenge upon assembly is to avoid shortcuts between the bumps, while at the same time providing enough compliance to obtain proper yield of the interconnects. For smaller pitches below 15 μ m, seed removal becomes challenging as well due to higher undercut with wet processes. There have been studies to reduce the undercut including study by Hess with using ion beam etching

processing, however the process suffered from an incoherent tin layer with a crown formation around the top surface [4]. In another approach reported by Yu [5], electroless Ni/Au is plated on already formed Al bumps to reduce the undercut. However, the use of gold close to the ROIC and at narrow gap can be problematic. It has been reported, possibly prematurely, that below 15 μ m pitch it is not possible to use wet etch processes due to high undercut. In this paper we report on the process with reduced undercut and no bump delamination down to 5 μ m pitch.

As a benchmark towards In, on the reliability side, we evaluate the reliability of the Sn based microbumps under cryogenics conditions. In effect, a large variety of infrared detector operate under cryogenic conditions, and no data is available about Sn microbump under cryogenic temperature. This being one of main reason why indium is still widely used [6].

Evaluation methodology

Cu/Ni/Sn Microbumps were developed and produced on 200mm Si wafer mimicking different imager formats. They consist of area array of bumps, with a pitch of 10 and 5 μ m, for a total chip size of a few cm².

Following this, the 10 μ m pitch samples were assembled onto HgCdTe substrates, which were finished by a realistic Under Bump Metallization (UBM) for such devices. We evaluated the assembly conditions and their related different failure modes. Furthermore, the generated stacks underwent 80K/293K temperature cycles and the morphology of the sample was evaluated.

On the 5 μ m pitch, most of the work was focused on providing 5 μ m pitch Cu/Ni/Sn microbumps, which is already far beyond state of the art. Still we could evaluate the assembly conditions for Si/Si stacks. This part of the work, was used to validate some of the process steps to manufacture ultra fine pitch such "bumps".

10 μ m pitch Wafer Level Bumping

200 mm Si wafers were bumped with Cu/Ni/Sn microbumps. The bumping process involves the use of seed layer deposition, 1X lithography, semi-additive plating, resist removal and seed wet removal. More details have been reported elsewhere ref [7]. An aerial view of a typical wafer after manufacturing is shown on figure 1. On figure 2 we show the microbump thickness wafer to wafer non uniformity. The detailed morphology of the microbumps is shown on figure 3, prior to assembly.

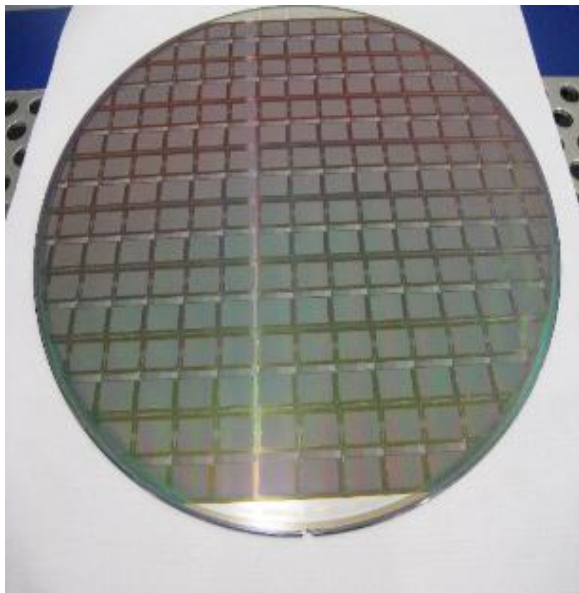


Figure 1. Photograph of Si wafer bumped with 10 μ m pitch

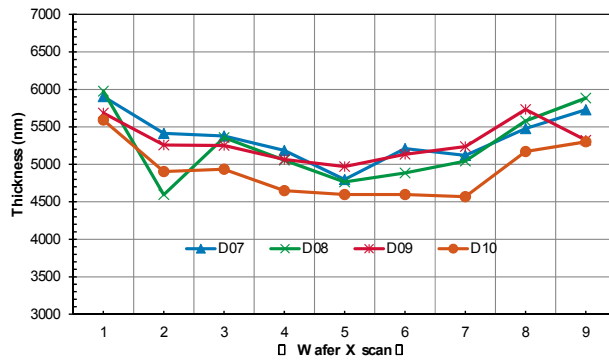


Figure 2: Across wafer bump height measurement.

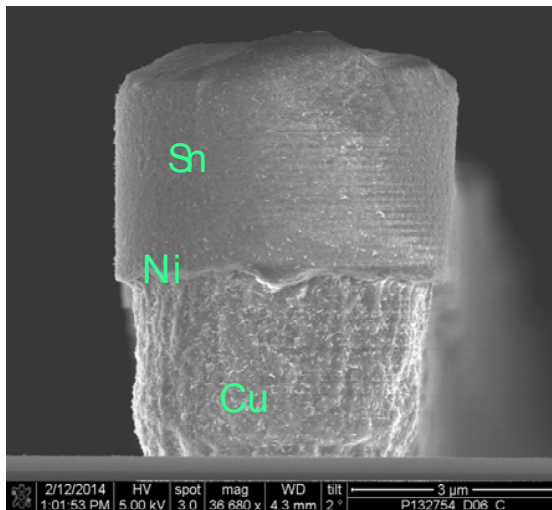


Figure 3. SEM photograph of typical 10 μ m pitch bump

5 μ m pitch Wafer Level Bumping – High Aspect ratio mini Sn pillars

As can be seen on figure 4, a typical showstopper to pitch scaling is the undercut process observed at the base of microbumps.

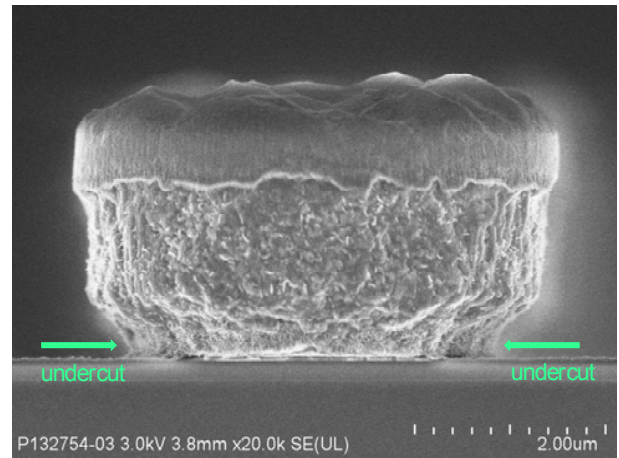


Figure 4. Microbump undercut

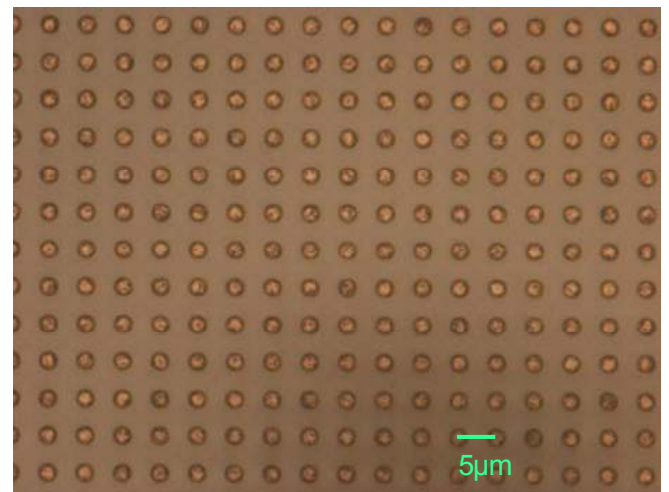


Figure 5. Aerial microscope image view of 5 μ m pitch bump array

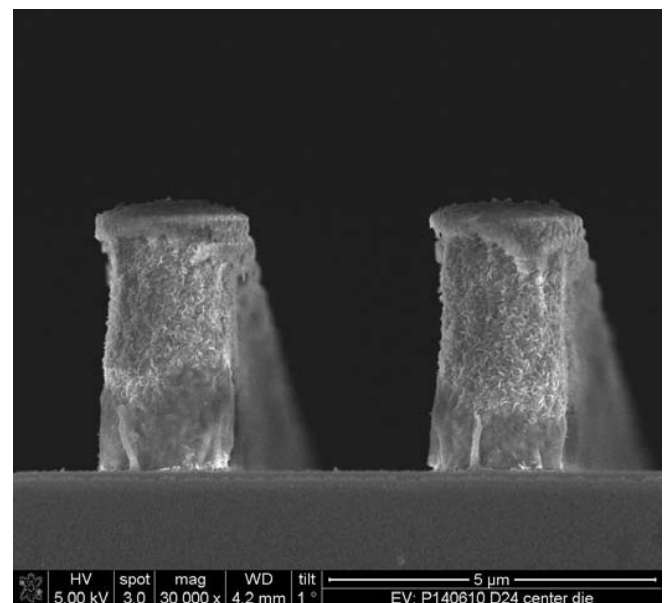


Figure 6. SEM photograph of 5 μ m pitch bump array

In order to circumvent the undercut issue, IMEC developed a specific process to prevent the undercut at the base of the bumps and produce high aspect ratio mini pillars which will in return ease the subsequent underfill process. With such process it is possible to produce microbumps that have a width of 2µm with a spacing of 3µm between bumps. The microbumps are planarised by mean of CMP technique, and offer a within die non uniformity of less than 0.6µm.

On figure 5 and 6, we show an aerial view of the wafer and a SEM picture of the microbumps.

10µm pitch - Assembly and Reliability

The 10µm pitch Si bumped samples were hybridized onto HgCdTe “dummy detector” chips, which had the standard UBM metallization process. The hybridization is realized by mean of thermo compression bonding followed by capillary underfilling. The assembly of the samples was performed in a SET FC150 precision bonder. Temperatures of less than 250C were used.

COMPONENT ID	short test	SEM analysis	cross section analysis	Cross section
PID				
1	OK	-		
2	-	OK	OK	
3	-	OK	OK	
4	-	NOK	NOK	
5	-	OK		OK
6	-	OK		OK
7	-	OK		OK
8	-	OK		OK

Table 1: overview of reliability results for 10µm pitch

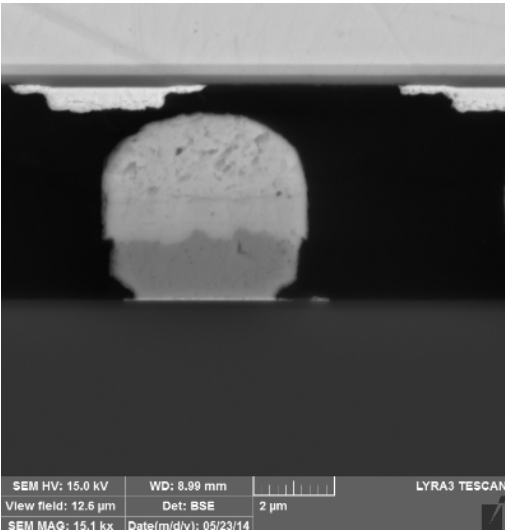


Figure 7. Failure observed on 10µm pitch sample

Among 8 components that were destined to reliability investigation purpose, only one had an interconnect issue, as displayed on figure 8. On this specific component, at least 50% of the µbumps did not connect the detection circuit and a strong misalignment was observed, as shown in figure 7.. The

remaining 7 components had an interconnect yield of 100 % and a misalignment below 2 µm. An overview of the different evaluations of such assemblies is given on table 1 .

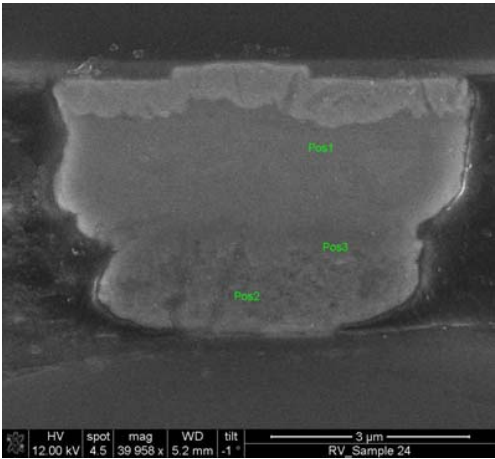


Figure 8. FIB SEM CUT photograph for EDX

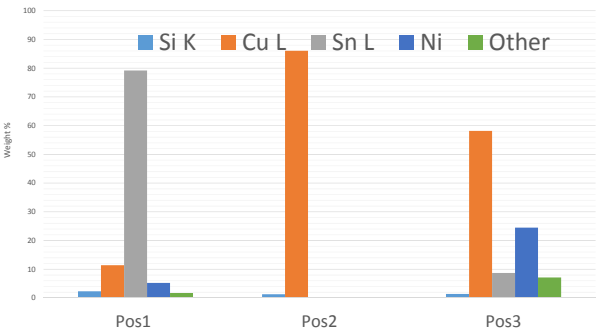


Figure 9. EDX data at different positions of the bonded microbump

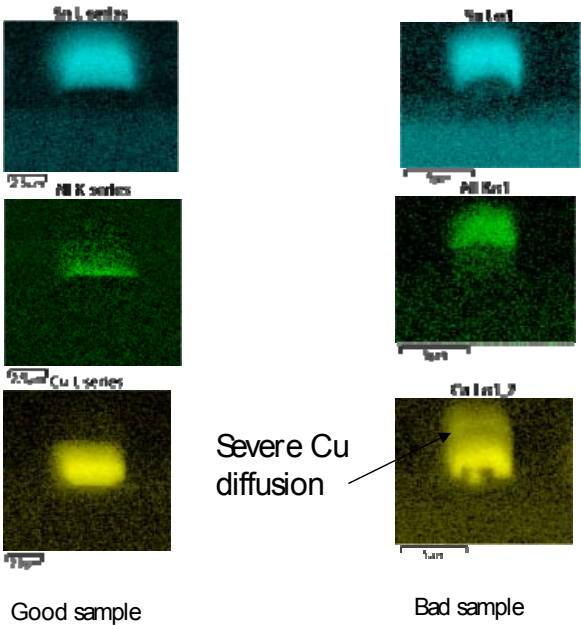


Figure 10. EDX comparison between good and bad bonded samples

On figure 8 we show a FIB cut and related EDX scan on figure 9 , indicating that proper metallurgical reaction has occurred between the Sn and the detector UBM, and Ni barrier was acting as such..

Among other samples - that did go through TC- we however identified improper bonding. An EDX analysis revealed that Cu had diffused into the Sn (see figure 10). A structure analysis reveals that the Ni layer was too thin to act as a proper diffusion barrier, and that Cu had already diffused into Sn prior assembly, preventing proper bonding.

After thermal cycling the physical integrity of 4 samples was investigated. No sign of failure could be observed after 960 cycles (see figure 12).

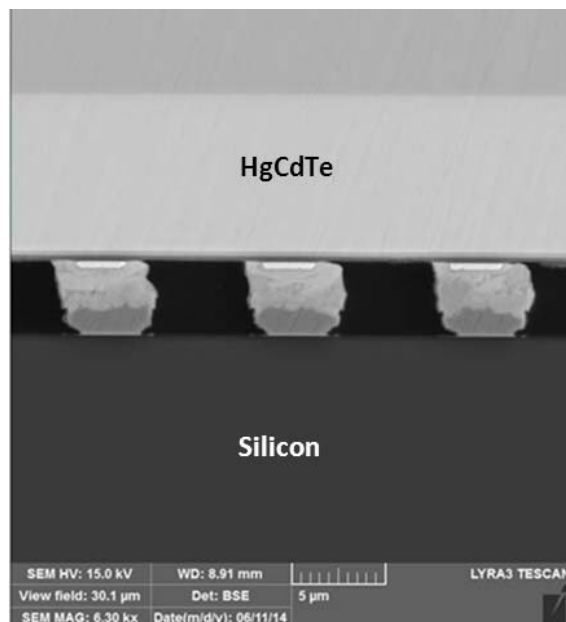


Figure 11. SEM picture of a 10µm pitch cross section after 960X cycles between 80K and 293K

5µm pitch - Assembly

The 5µm pitch Si bumped samples were hybridized onto Si “dummy detector” chips, which had the standard UBM metallization process. The bonding was performed using a precision bonder FC150 with a theoretical accuracy of +/-1 µm 3 sigma post bonding.

The hybridization is realized by mean of thermo compression bonding at less than 250°C during 15 min followed by capillary underfilling.

As can be seen on figure 12 and 13, the dies were bonded and underfilled successfully. Among the multiple hybridizations, we noticed some discrepancies with the alignment. Nevertheless, some submicron alignment assemblies were accomplished. On properly bonded samples, we noted that capillary underfill with 5 µm pitch µbumps could be achieved without visible voids. This was confirmed by SAM and SEM microscopy

However, as shown on figure 14, the junction between the bump and the UBM, appears to be partially complete, we attribute this to improper eutectic point of the solder due to

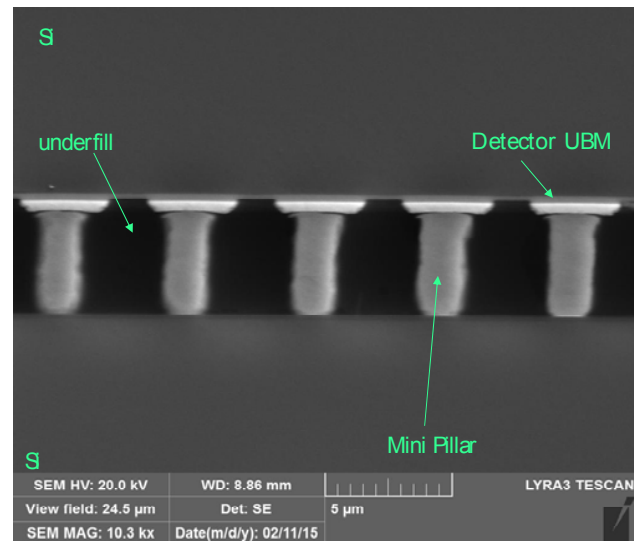


Figure 12: XSEM view of bonded 5µm pitch sample

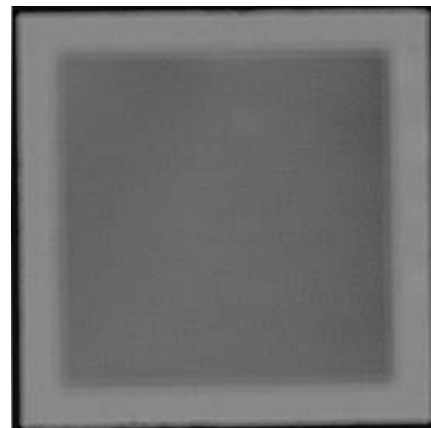


Figure 13: Scanning Acoustic Microscopy view of bonded 5µm pitch sample.

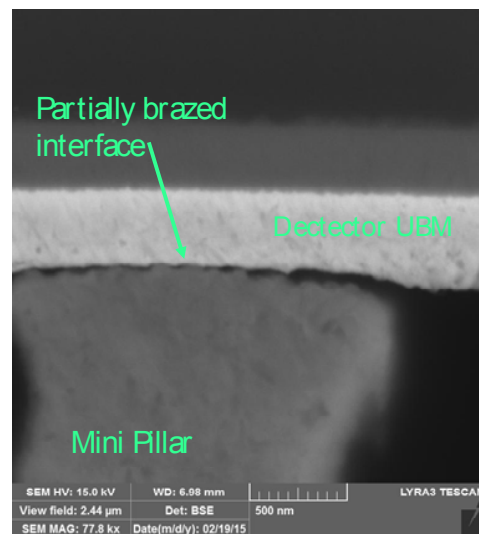


Figure 14: XSEM Interface detail.

Cu contamination and/or lack of Sn. It appears that the sample did not have enough pure Sn to allow for low enough temperature melting point. This means that the assembly can

be further optimized by improving the respective amount of Cu, Ni and Sn.

Discussion

Bumping & Assembly

While the 10 μ m pitch process presents a rather high level of maturity – in a research context –, more disruptive technique involving advanced lithography, CMP had to be used to generate the 5 μ m samples. At 5 μ m pitch, the comparison of underfill structured is depicted for Indium ball and a mini-pillar (Figure 15). It appears clearly that the underfill glue has more space to spread in the second configuration. If we evaluate the ratio (space for underfill/complete volume between components) for the 5 μ m pitch optimal structures, we could anticipate a ratio up to 87% for the mini pillar structure (figure 16).

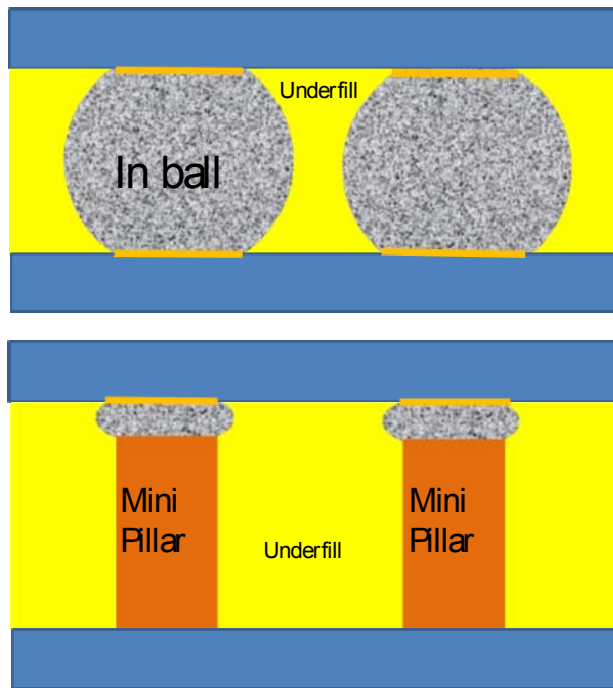


Figure 15: Drawing showing the advantages of pillars (bottom) Vs balls (top) with respect to capillary underfill processes.

5 μ m pitch	μ balls	μ bumps
average diameter	4 μ m	2 μ m
average gap	3 μ m	4 μ m
space for underfill (ratio)	53%	87%

Figure 16: Extrapolated structures for 5 μ m pitch

This type of interconnect structure tends to prove that capillary underfill processes is still an alternative to PAUF (Pre-Applied Underfill) for fine pitch flip chip bonding.

Failure modes

During the execution of the assembly and reliability experiments, the following processing failures have been identified :

- Improper bonding due to Cu diffusion into Sn
- Improper bonding due to non planarity/ sample contamination
- Misalignment

It is worth mentioning that the 10 μ m pitch samples that were good after thermo compression bonding did survive all the thermal cycle tests and that no additional failure was observed. This means that Sn – in a microbump shape- has potential to be used under harsh conditions such as, cryogenic temperature.

Conclusions

200mm Si wafers were successfully bumped down to 10 and 5 μ m pitch.

In term of reliability, the 10 μ m pitch Cu/Ni/Sn samples were successfully hybridized to large array HgCdTe detection circuits 1024 X 768 (XGA). These components followed 960 thermal cycles 80K/293K without any visible structural change, showing similar reliability response than classical indium from a thermo mechanical point of view.

The 5 μ m pitch material was assembled and a narrow gap of 4 μ m was successfully underfilled, a specific process was used to avoid bump undercut and produce 5 μ m pitch mini pillars. Despite the small gap the 5 μ m pitch samples were underfill thanks to the high aspect ratio of the mini pillars. We have identified the lack of Ni barrier as main failure mode during assembly. This can be corrected by electro-plating optimization.

Finally, we show that the Sn based microbump technology has the potential to address both the extreme pitch scaling and reliability constrains of such high density interconnections of heterogeneous material, operating under extreme temperature variations. On figure 17, we show the dramatic increase that such interconnect density can bring for an hybrid IR sensor, using wafer scale bumping processes

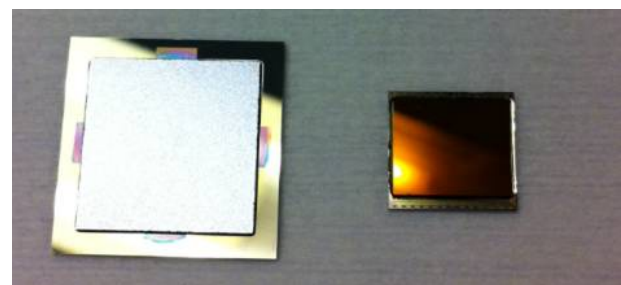


Figure 17. Comparative picture of : Left 5 μ m pitch 3072 X 3072 (about 9 MPixels) and Right 15 μ m pitch 640 X 512 (about 0.3 Mpixels) sensor formats

Acknowledgments

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