Wafer-level 3D integration with 5 micron interconnect pitch for infrared imaging applications

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ABSTRACT

The use of 3D integration technology in focal plane array imaging devices has been shown to increase imaging capability while simultaneously decreasing device area and power consumption, as compared to analogous 2D designs. A key enabling technology for 3D integration is the use of high density metal-metal bonding to form pixel-level interconnects between device layers. In this paper, we review recent progress in high density, sub-10 µm pitch interconnect bonding for 3D integration of imaging systems. Specifically, we will present results from successful demonstrations of the use of Cu microbumps for the interconnection of 5 µm pitch 640×512 and 1280×1024 arrays. Operability of the arrays of bonded interconnects in two-layer silicon die stacks was greater than 99.99% with good electrical isolation between bonds.

Keywords: Cu-Cu bonding, 3D integration, heterogeneous integration, 3D interconnects

1. INTRODUCTION

The use of 3D integration technology for the fabrication of imaging systems provides system designers with access to powerful new multifunctional imaging capabilities while at the same time reducing size, weight, and power usage. Stacking of semiconductor devices with through-chip electrical connections can enable multi-spectral imaging through the incorporation of multiple detector layers or create 3D readout integrated circuits (ROICs) in which the analog and digital readout circuitry is vertically integrated, providing increased on-chip signal processing behind each pixel [1]. Figure 1 shows a scanning electron micrograph (SEM) image of a cross-section of a device from a recent demonstration of mixed-signal 3D integration in which analog and digital ROICs were integrated with pixel-level connections between the layers [2]. This process utilized 3D integration technology to allow for the fabrication of heterogeneous devices in optimum design rules, increasing the yield of the constituent chips, decreasing the circuit footprint required for each pixel, and decreasing the system power usage.

In order to increase the resolution of these advanced 3D-integrated detectors, while maintaining or shrinking the system size, the focal plane arrays (FPAs) will need to be fabricated at ever decreasing pixel pitch. The next generation of FPAs will require higher pixel density with a concurrent increase in the density of metal interconnects suitable for 3D integration processes. Previous work at RTI has shown the scalability of Cu/Sn-Cu and Cu-Cu bonding to create high yielding metal-metal interconnects down to 10 µm pitch [3, 4].

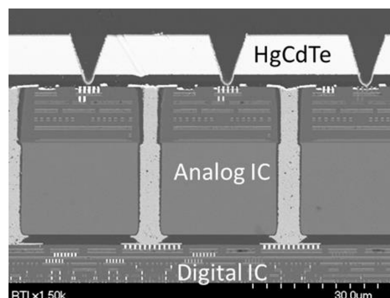

Figure 1. Cross-section SEM micrograph of a 3D integrated infrared detector, composed of a HgCdTe photodiode array and a 3D ROIC.

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Cu-Cu thermocompression bonding has been shown to offer a reliable and scalable method for forming interconnects between ICs [3, 5-8]. Hybrid bonding, in which coplanar Cu and oxide surfaces are bonded simultaneously, has very stringent requirements for planarity, surface preparation, and surface cleanliness. For this approach, there is no gap between the die and particles in the bondline could potentially inhibit interconnect bond formation. Also, the combination of the short length of the interconnects between chips and the high annealing temperature required after bonding could pose a reliability concern for large area array heterogeneous bonding, such as the hybridization of FPA detectors fabricated in compound semiconductors to Si ROICs.

In this paper, a process for the fabrication and bonding of large area arrays (1280×1024 and 640×512) of 5 µm pitch Cu interconnects is demonstrated. Figure 2(a) shows the proposed incorporation of the 5 µm pitch bonding module in a "vias-middle" 3D integration process flow, starting after IC-1 wafer backgrinding and through-silicon via (TSV) reveal. To ensure electrical isolation of the bond pads/microbumps from the substrate, the silicon is slightly recessed below the plane of the exposed Cu TSVs using reactive ion etching (RIE). Following the RIE step, silicon oxide (SiO_2) is deposited on the backside surface of the IC-1 wafer to provide the isolation. The temperature at which the SiO_2 deposition can be done is limited by the thermal budget of a temporary wafer carrier and the adhesive layer. Chemical mechanical polishing (CMP) of the backside dielectric and Cu TSVs is used to create a planar dielectric-Cu surface. Cu pads/microbumps that connect to TSVs are then patterned on the backside wafer surface. These Cu microbumps, together with the corresponding Cu microbumps on the IC-2 wafer, are used to bond the thin IC-1 die to IC-2 die, which creates both the mechanical bond between the die and pixel-level electrical interconnects.

For the purposes of the current demonstration, Cu bond pads were formed on two full-thickness passive Si wafers which were then diced. The die were bonded in a face-to-face configuration, as shown in Figure 2(b) to create area arrays of Cu interconnects in either 640×512 or 1280×1024 format, both with the pitch of 5 µm. The interconnects were electrically tested to determine the interconnect array operability (bond yield) and verify the electrical isolation between neighboring interconnects.

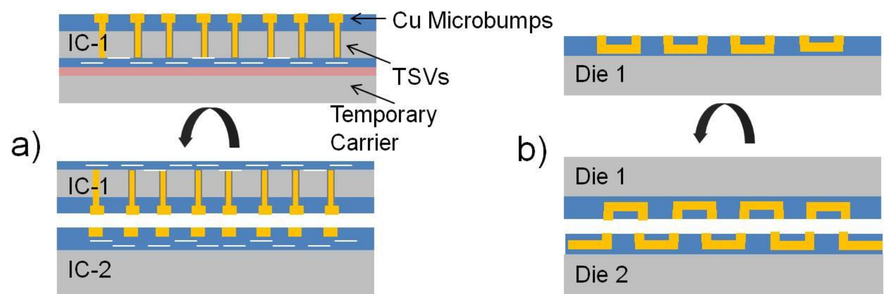

Figure 2: Schematic diagram illustrating the use of high density Cu-Cu bonding to integrate two die. In a) after backside TSV reveal, Cu interconnects are formed over TSVs then the thin die is bonded to a mating die. In b) Cu pads are formed on the test wafers, then the die are bonded, which results in daisy chains of inter-layer interconnects.

2. FABRICATION OF THE TEST VEHICLES

Test vehicles were fabricated on 150 mm silicon wafers. First, a metal routing layer was patterned by e-beam deposition and lift-off, simulating IC top metal. The metal routing layer provided the electrical connections in the chains of bonds as well as the probe pads located at the perimeter of the die for testing of the electrical conductivity of the chains. The metal routing layers and Cu interconnects were designed for compatibility with a 640×512 detector with 5 µm pitch pixels. The design also included die with a 1280×1024 area array on the same pitch. Each of the daisy chains (channels) contained 1280 bonds connected in series for two-wire resistance measurement. In this layout, a single nonfunctional bond renders the channel electrically open. The routing pattern is illustrated in Figure 3.

Two different methods were used to fabricate the vertical Cu interconnects; one used an approach in which silicon oxide was deposited over Cu pads and polished using CMP, and one was based on a Cu damascene approach. We will refer to these methods as "oxide-polish" and "Cu-polish" methods, respectively. These two methods are illustrated in Figure 4 and described below.

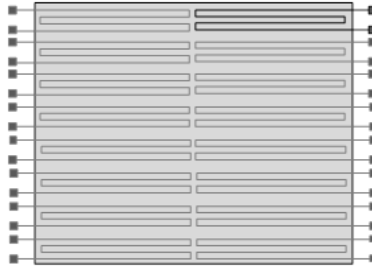

Figure 3. Schematic diagram of the testing structure in plan view showing the layout of the individual test channels. Each die contains 256 test channels and each channel contains 1280 microbumps connected in series.

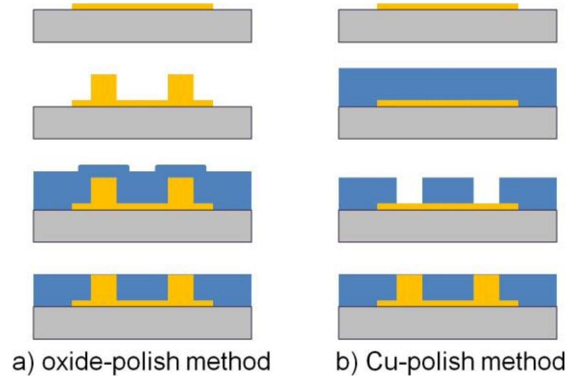

Figure 4: Schematic diagram of the two methods used to fabricate the 5 µm pitch vertical Cu interconnects. For the a) oxide-polish method, conformal oxide was deposited over Cu microbumps, then polished to create the planar surface. For the b) Cu-polish method, Cu was deposited into oxide vias after which the Cu overburden was removed by CMP.

In the first case, shown schematically in Figure 4(a), after the routing metal was formed, 3 µm diameter Cu microbumps were formed by electroplating Cu into a photoresist template. A conformal SiO_2 was deposited from a tetraethyl orthosilicate (TEOS) precursor over the Cu microbumps. It should be noted that the use of the TEOS-based deposition is limited to cases where the wafer does not need to be thinned below ~200 µm. Thinning wafers to less than 200 µm typically requires the use of a carrier wafer and an adhesive. The thermal budget of currently available temporary adhesives limits the SiO_2 deposition temperature to ~250°C or less, compatible with a silane-based PECVD but not TEOS-based CVD. The PECVD technique results in the deposition of films with a smaller degree of conformality than that achievable in TEOS CVD, which may require an adjustment of the geometry of Cu microbumps. After the SiO_2 deposition, CMP was used to remove the oxide from the top of Cu bumps and to provide a final polish to the Cu microbump surface.

In the second case, shown in Figure 4(b), following the patterning of metal routing layers, SiO_2 was deposited by PECVD. An I-line stepper was used to pattern 3 µm diameter features in a photoresist layer; the pattern was then transferred into the oxide using RIE. In the implementation of this process for building interconnects on the backside of IC wafers with TSVs, the oxide etch step would expose TSVs for connection to Cu microbumps. A conformal deposition of Cu by metal-organic chemical vapor deposition (MOCVD) was used to fill the oxide vias. The excess Cu was polished back using CMP, stopping at the copper-insulator interface. The polish must be carefully controlled to avoid recessing the Cu below the oxide surface which would inhibit good Cu bond formation.

Atomic force microscope (AFM) measurements were taken to determine the surface roughness of the Cu prepared by SiO_2 polishing and Cu polishing. Selected wafers from both the oxide-polish and Cu-polish splits were etched to recess the oxide below the plane of the top of the Cu microbumps. This recessing of the oxide was done to increase the particle tolerance of the die bonding process. As mentioned earlier, when two planar surfaces are brought into contact, a particle can cause a large disturbance in the bondline, resulting in a local cluster of non-bonded interconnects [8]. The gap that forms as a result of the recess needs to be sealed or underfilled in order to prevent corrosion of the Cu interconnects.

For both the oxide-polish and Cu-polish methods, we included dummy (electrically inactive) Cu features to maximize bump height uniformity. In the oxide-polish case, Cu bumps were electroplated, so dummy Cu features were added to

maintain uniform pattern density across the wafer, necessary for bump height uniformity both within the array and across the wafer. Without these dummy features, the bumps near the edge of that array would plate higher and the subsequent oxide polish may not be sufficient to correct the non-uniformity. Similarly, for the Cu-polish case, the inclusion of dummy features around the perimeter of the array is important to avoid local changes in the chemical and mechanical polish rate of Cu near the edges of the array. Because of the non-compliant nature of Cu-Cu bonding, small changes in the height of Cu microbumps can decrease the interconnect yield.

3. BONDING AND CHARACTERIZATION

Once the Cu pad fabrication process was completed, both top and bottom wafers were diced, and the die were bonded using thermocompression during which the die are held together under heat and pressure in order to form the metal-metal bonds. The bonding was performed in a SET FC150 precision bonder under nitrogen purge. This bonder has ± 1 µm alignment accuracy during cold placement. The alignment of the bonder was calibrated using test bonds that occur at the same bond force and temperature as those in device die. Prior to bonding, Cu pads were chemically pre-treated with a weak sulfuric acid solution to remove Cu oxides. The bonding was performed at 290°C for 900 s; there was no annealing of the samples after bonding.

SEM was used to image test wafers with bond pads and to image cross-section samples prepared from bonded die. To facilitate cross-sectioning, the bonded die pairs were underfilled with an experimental, unfilled epoxy from Lord Corp. The mechanical strength of the bonded die was measured through die shear testing in a Nordson Dage 8400 Bondtester with a 100 kg load cell. The bonded die pairs were electrically characterized by two-wire probing of daisy chains of interconnects. Electrical testing was used to check for continuity of all 256 channels from each die. I-V curves were also acquired from selected channels to determine the linearity of the channel resistance and to check for leakage current between neighboring channels.

4. RESULTS

Following the wafer fabrication process, AFM and optical interferometry were used to characterize the Cu roughness and microbump height uniformity. Figure 5 shows sample AFM images taken from an oxide-polish sample and a Cu-polish sample. The Cu pads formed by oxide polish had an average roughness (*Ra*) of 4.6 nm, while the Cu pads formed using a Cu-polish method had an *Ra* of 15.6 nm. Optical interferometry measurements showed a local difference in the microbump height of approximately 70 nm for oxide-polish samples and almost no measureable difference (less than 10 nm) in the microbump height for Cu-polish samples. Characterization of Cu microbumps after electroplating, but prior to oxide deposition, showed similar height results, suggesting that the nonuniformity of the plated Cu was the primary contributor to the height nonuniformity after oxide CMP.

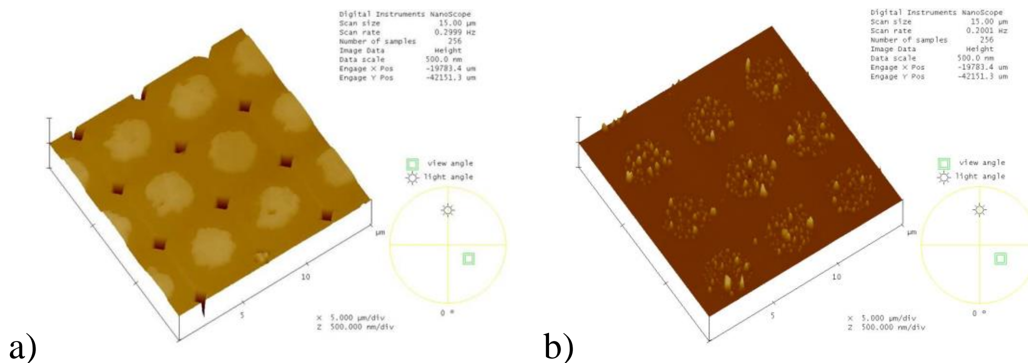

Figure 5. AFM scans of the Cu microbump surfaces formed by a) oxide-polish and b) Cu-polish methods. The Cu bumps formed by oxide polish had an Ra of 4.6 nm, while the Cu bumps formed using a Cu-polish method had an Ra of 15.6 nm.

SEM images of Cu interconnects formed by oxide polish are shown in Figure 6. The oxide surface on the substrate wafer, shown in Figure 6(a), was left flush with the Cu microbumps, while in Figure 6(b), the oxide was recessed back from the plane of the top of the Cu microbumps to create a gap between the oxide surfaces of the two die when they are bonded. The oxide deposited over the Cu-plated bumps was seen to leave small diamond-shaped gaps between bumps. If this feature is found to be undesirable, an increase in the oxide deposition thickness would fill the gap due to the highly conformal nature of the TEOS deposition.

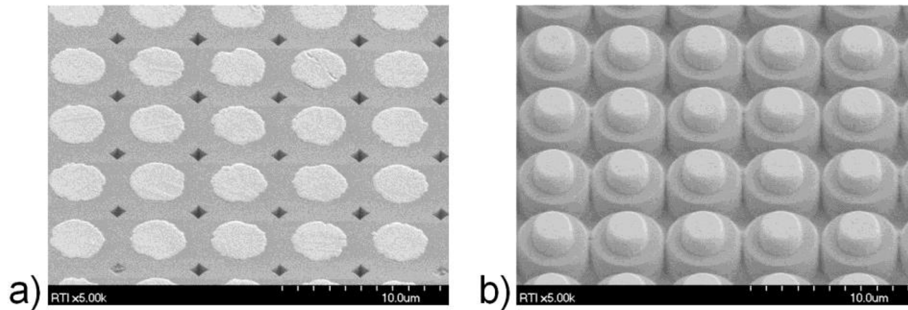

Figure 6. Top down SEM images of Cu interconnects formed by oxide-polish. Images are shown of a) the substrate with a flush oxide and Cu surface and b) the chip wafer in which the oxide was etched back to create greater particle tolerance during bonding.

To determine the bonding force required for high interconnect yield, initial bonding experiments focused on channel yield as a function of bonding pressure at the 290°C bonding temperature. Figure 7 shows the channel yield as a function of the bond pressure for both oxide-polish and Cu-polish die pairs. High yielding die pairs were produced at a bond pressure of 240 MPa for Cu-polished 640×512 arrays and oxide-polished 1280×1024 arrays. Higher pressure (320 MPa) was required for high yielding die pairs of oxide-polished 640×512 arrays.

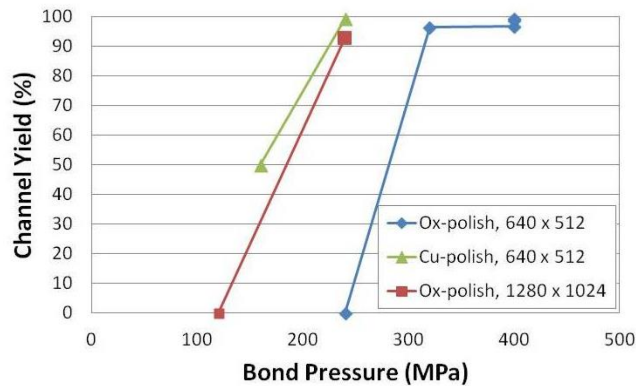

Figure 7: A graph of the channel yield of bonded devices versus the bond pressure for die with 640×512 arrays and 1280×1024 arrays of Cu interconnects from the oxide-polish lot and 640×512 arrays of Cu interconnects from the Cu-polish lot.

4.1 Oxide-polished samples

After the initial screening, multiple die bonds were performed using the oxide polished 640×512 arrays at 400 MPa to determine the repeatability of the bonding process. One of the 400 MPa samples was sheared at 9.4 kgf. Electrical testing was used to determine channel resistance, channel yield, and the number of channels containing bonds that were shorted to each other. The results of the electrical testing are shown in Figure 8. The average channel yield was 97.6%. Open channels, defined as channels having resistance greater than 5 kΩ, were generally randomly scattered among the 256 channels. Based on visual inspections showing that the open channels were generally due to randomly scattered bond defects, these channel yields correlate to an estimated interconnect operability of the 640×512 arrays of greater than 99.99%. Randomly tested channels exhibited ohmic responses for -5 V to +5 V sweeps; a representative result is shown in Figure 9. Because of the serpentine routing of the channels, channels having a resistance of less than 150 Ω were considered to be shorted. None of the samples had more than four channels with shorts, similar to the case of 10 µm pitch 640×512 arrays bonded using the Cu/Sn–Cu material system [4].

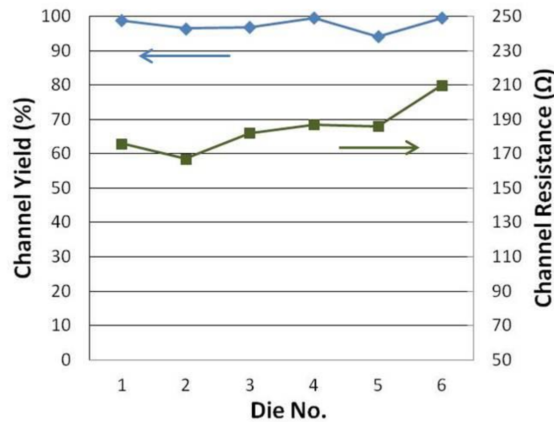

Figure 8: A graph of the channel yield and median channel resistance measured from test vehicles with 640×512 area arrays on 5 µm pitch. Each die pair contains 256 channels, with each channel consisting of 1280 serially-connected interconnects.

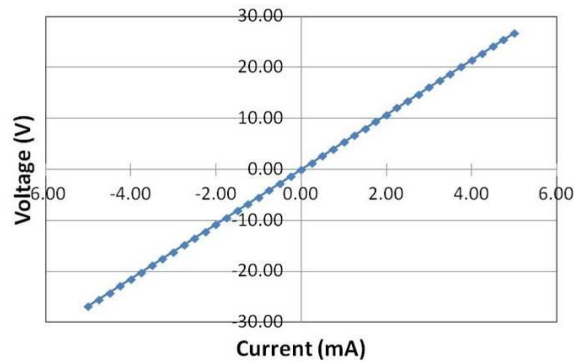

Figure 9: An I-V curve taken from a representative channel of a 5 µm pitch 640×512 array test vehicle.

In the layout of the test die, each pair of neighboring channels has 320 pairs of interconnects that are located 5 µm, center to center, from each other. Leakage current measurements between neighboring channels of interconnects were used to assess the isolation between the microbumps. Four randomly selected channel pairs were measured for two bonded die. All the channel pairs tested exhibited less than 22 pA of current at up to 5 V of applied bias, a resistance of over 225 GΩ, indicating good electrical isolation between neighboring interconnects.

The bonded parts were subsequently underfilled and cross-sectioned along the rows of interconnects. Figure 10 shows two of the cross-section SEM images from an oxide-polished 640×512 array. The alignment of this particular bond in the plane perpendicular to the bond direction was within 0.6 µm; the bondline between Cu interconnects is only faintly visible indicating good physical contact. The gap between the two oxide surfaces, 1.3 µm in height, was fully filled with the epoxy applied after bonding. The standoff height from the routing layer to the routing layer is 4.5 µm. More work is needed to correlate the standoff height with reliability of the interconnects, when bonding heterogeneous semiconductors with varying coefficients of thermal expansion.

4.2 Cu-polished samples

The initial bonding tests, shown earlier in Figure 7, indicated that high bond yield was achievable at lower bond pressures with Cu-polished die samples compared to oxide-polished samples. While the *Ra* of the Cu interconnects was higher for Cu-polished samples, the optical interferometry measurements on these samples indicated smaller nonuniformity in local microbump heights, which may explain the lower bond force requirement. Further bonding experiments using Cu-polished die are being used to gather statistics on the bond yield and the die yield. The results of this study will be published in the future.

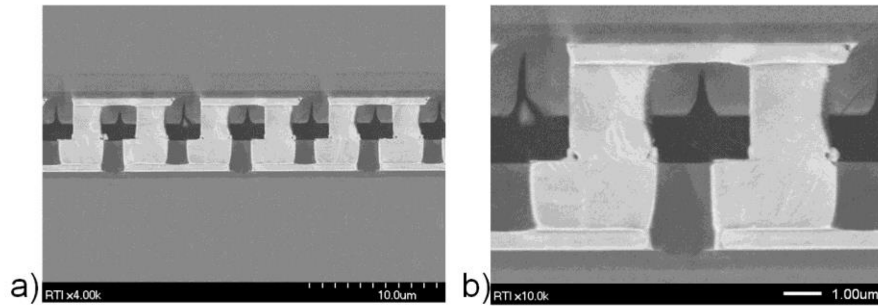

Figure 10: Cross section SEM images of bonded 5 µm pitch Cu–Cu interconnects, showing a) six consecutive bonded interconnects and b) one pair of interconnects. These interconnects were formed using the oxide-polish method. The oxide on the top chip was recessed before bonding to create greater particle tolerance. The alignment of this bond is within 0.6 µm.

5. CONCLUSIONS

We have successfully demonstrated two methods for the formation of 5 µm pitch Cu interconnects and performed high yield bonding of these interconnects in both 640×512 and 1280×1024 area arrays in die-to-die configuration. Electrical testing showed the high bond yield of the interconnect arrays (>99.99%) and the high degree of electrical isolation between long rows of neighboring interconnects (>225 GΩ resistance at 5V). Despite a 2× reduction in the pitch of the bonded interconnects, the low occurrence of channels with shorting interconnects compared favorably with previous results from 640×512 10 µm pitch arrays bonded with the Cu/Sn – Cu metal system. The two Cu interconnect formation processes used here, a Cu-polish approach and an oxide-polish approach, create a 1 µm or greater standoff height between die for greater particle tolerance of the bonding process. These fabrication processes are also compatible with temporary wafer carrier systems which are used to support thin wafers during the formation of 3D interconnects between stacked die that contain TSVs. The high density metal interconnects offer a solution for the hybridization of next generation focal plane arrays with Si ROICs.

6. ACKNOWLEDGEMENTS

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