High Density Interconnect Bonding of Heterogeneous Materials Using Non-Collapsible Microbumps at 10 µm Pitch

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***Abstract*— This paper reports on a successful demonstration of the use and reliability of Cu/Sn microbumps for the fine pitch interconnection of heterogeneous semiconductor die. InP die have been bonded to Si substrates using a 6.4 mm × 5.12 mm area array of alloyed Cu/Sn microbumps on 10 µm pitch. After bonding, 256 separate channels, each connecting 1280 microbumps, were electrically tested on each die; the channel yield was used to estimate the operability of the 640 × 512 arrays, which was found to be greater than 99.99% for both InP-Si die pairs and Si-Si control die pairs. After 500 thermal cycles from -40 °C to 125 °C, no significant change in the channel yield was seen for the homogeneous Si-Si die pairs. The InP-Si die pairs underfilled with an experimental epoxy had a 2.8% decrease in channel yield while those die pairs without the underfill saw a 13.9% decrease. The channels that failed during thermal cycling were predominately located near the edges of the die pairs, indicating that the bump failures were due to the difference in thermal expansion between InP and Si. Cross-sectional SEM images taken from the edge areas of both underfilled and non-underfilled InP-Si die pairs were used to assess the failure mode in the non-underfilled samples and to demonstrate the positive effects of the use of the underfill.**

Keywords— Cu/Sn bonding, heterogeneous integration, InP, Near-infrared sensors, 3D integration, reliability, microbumps

I. INTRODUCTION

While the continued scaling down of transistor dimensions is reaching its physical limits, 3D integration of electronic devices offers a path toward further increases in computing power and system performance. One of the most powerful aspects of 3D integration is the ability to closely integrate heterogeneous materials. Various semiconductor devices, such as Si CMOS ICs, InGaAs detectors, and GaN power amplifiers, could be fabricated separately using the optimum facilities and process conditions for each material/technology, then seamlessly integrated to create powerful systems that are only realizable using the short electrical connections and/or massively parallel signal processing enabled by 3D integration.

A key technological challenge facing the 3D integration of heterogeneous semiconductors is the formation of high density metal interconnects between dissimilar substrates, such as compound semiconductors (CS) and Si. Due to the difference in the coefficients of thermal expansion (CTE), one can expect: 1) some misalignment between microbumps fabricated on the CS substrate and the Si substrate during bonding at an elevated temperature; and 2) bond interconnects will experience shear strain as the bonded die pair is cooled to room temperature and during any subsequent thermal excursions. To estimate the magnitude of the misalignment, we calculated the relative change in distance between corner microbumps in a 10 µm pitch 640 × 512 array on CS die vs. Si die, using the equation $DNP*(CTE_{CS}-CTE_{Si})*\Delta T$, where *DNP* is the distance to the neutral point (die center), and ΔT is the temperature difference. Figure 1 plots this CTE-induced misalignment for InP, GaN, InGaAs, and GaAs. The CTE's of these materials are 4.75, 5.60, 5.66, and 5.86 ppm/°C, respectively, compared to Si at 2.9 ppm/°C. Once the bonding takes place, a shear strain will develop in the bonds upon cooling to room temperature and upon subsequent temperature excursions. To the first order, the strain is given by $\rho=DNP*(CTE_{CS}-CTE_{Si})*\Delta T/H$, where H is the height of the bond. The equation indicates that, like the misalignment, the shear strain increases with the distance from the chip center, so the corner microbumps and large arrays experience the largest shear forces. Underfill of the die after bonding provides mechanical support for the microbumps and can more evenly distributes thermal stress across the assembled structure.

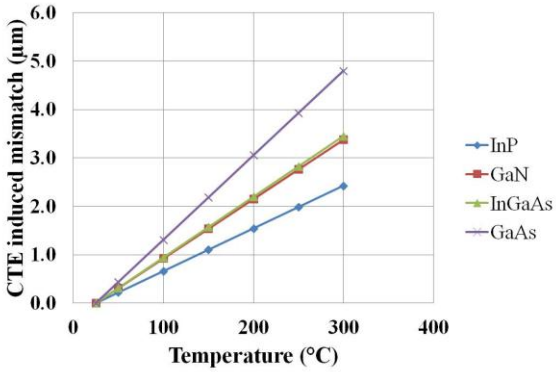

Fig 1. A graph of the CTE induced misalignment between corner bumps on Si and on four other semiconductor materials vs. temperature for a 6.4 mm x 5.12 mm array size, assuming they are aligned at room temperature

To counter the effect of CTE mismatch, high density bonding of heterogeneous semiconductors has typically been achieved using collapsible bumps, such as indium. While the low bonding temperature and modulus of indium is desirable in this application to reduce shear strain, the low melting point of the bumps can be a concern if additional processing is needed to stack die or complete 3D interconnects. In such cases, a non-collapsible bump would be preferred [1].

Non-collapsible Cu/Sn microbumps are one such interconnect choice [2-3]. The rigid nature and high melting point of the Cu_3Sn intermetallic bond allows subsequent high temperature processing to be done without the risk of collapsing the bumps and causing electrical shorting in high density area arrays. These attributes have led to the Cu/Sn metal system being used for advanced integration of Si ICs, yet very little has been reported on the use and reliability of Cu/Sn for the integration of dissimilar semiconductor substrates with varying CTE's.

This study explores the use and reliability of Cu/Sn microbumps for high density integration of InP and Si die. The integration of electronic devices fabricated on InP substrates with Si CMOS ICs is important for a variety of applications such as wide bandwidth analog-to-digital converters (comprised of InP heterojunction bipolar transistors coupled with Si CMOS) [1] or uncooled, near-infrared sensors (comprised of epitaxial InGaAs focal plane arrays on InP substrates bonded to Si readout integrated circuits) [4]. For this work, InP die with 640 × 512 area arrays of Cu/Sn microbumps have been bonded to Si die with corresponding arrays of Cu microbumps.

II. Fabrication and Bonding

A. *Test Vehicle Fabrication*

To generate die for the interconnect bonding experiments, we fabricated "top die" and "bottom die" routing metal patterns on InP and Si wafers. The routing metal connects the 640 x 512 array of microbumps on a 10 µm pitch into electrically testable channels. The "top die" patterns were formed on 75 mm InP and 75 mm Si wafers, while the "bottom die" patterns were fabricated on 200 mm Si wafers. The bottom die are slightly larger than top die to accommodate probe pads for each channel. Each channel consists of 1280 bonds connected in series for two wire resistance measurement. In this layout, a single nonfunctional bond renders the channel electrically open. The routing pattern is illustrated in Figure 2. The InP wafers were test grade wafers of (100) orientation, 600 µm thick, and S-doped (InPACT S.A). The Si wafers were test grade, (100) orientation, and were either 725 µm thick for 200 mm wafers or 380 µm thick for 75 mm wafers.

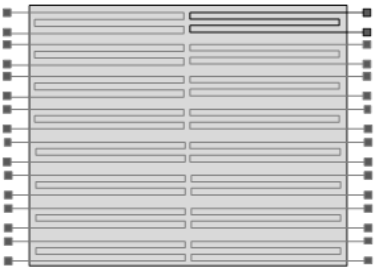

Fig 2. Schematic diagram of the testing structure in plan view showing the layout of the individual test channels. Each die contains 128 channels on each side and each test channel contains 1280 microbumps connected in series.

The process flow used to fabricate the routing layers and microbumps on both the Si and InP wafers is shown in Fig. 3. Routing metal was deposited by e-beam evaporation and patterned by metal lift-off. The metal was 0.5 µm thick Cu with an adhesion layer of Ti. A plating seed layer consisting of another Ti adhesion layer and a 0.15 µm thick layer of Cu was sputtered on all wafers. Next, an 8 µm thick layer of 9260 positive photoresist (AZ Electronic Chemicals) was spun on both sets of wafers and patterned using contact lithography. The Cu bumps were plated to nominally 3 µm in thickness using a methanesulfonic acid–based copper plating solution from Enthone Inc. Additive levels in the plating bath were controlled to obtain flat, rather than domed, microbumps. On the top wafers, Sn was plated on the Cu microbumps using Technistan JM6000 Sn solution from Technic, Inc. Figure 4 shows a scanning electron micrograph (SEM) image of the

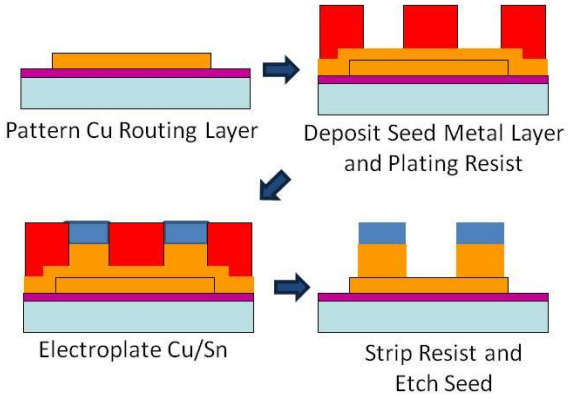

Fig. 3. Diagram of process used to form routing metal and 10 µm pitch Cu/Sn microbumps

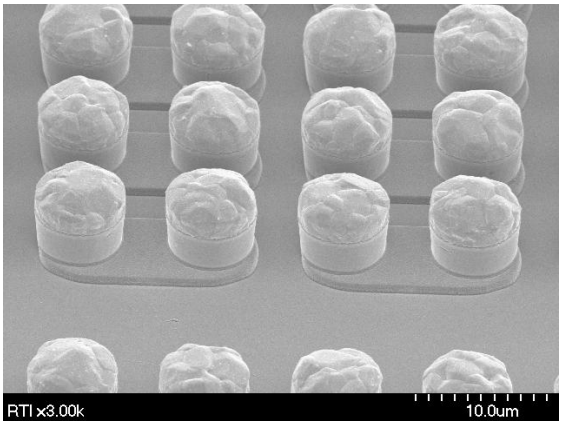

Fig. 4. SEM image of Cu/Sn bumps at 10 µm pitch on an InP substrate

TABLE 1. POST BONDING ELECTRICAL DATA SUMMARY

Die type	Si – Si		InP – Si	
Underfill	no	yes	no	yes
Sample IDs	1, 2	3, 4	5 – 7	8 – 10
Channel yield per die (%)	96.9 - 98.4 (Avg. 97.7)	96.9 - 99.6 (Avg. 98.2)	96.1 - 98.0 (Avg. 97.4)	96.5 - 98.4 (Avg. 96.9)
No. of open ch. per die	4 - 8 (Avg. 6)	1 - 8 (Avg. 4)	4 - 9 (Avg. 7)	5 - 10 (Avg. 8)
No. of shorting ch. per die	1 - 26 (Avg. 14)	6 - 6 (Avg. 6)	2 - 9 (Avg. 5)	5 - 8 (Avg. 6)
Median resistance per ch. (Ω)	74 - 148 (Avg. 111)	73 - 74 (Avg. 74)	70 - 83 (Avg. 77)	70 - 89 (Avg. 80)
Extrapolated bond yield (%)	>99.99	>99.99	>99.99	> 99.99

Cu/Sn bumps on an InP wafer. Ion milling was used to remove the seed layer from between the routing metal links. Electrical testing was used to verify electrical isolation between adjacent bumps and the routing metal.

B. Die Bonding Experiments – Cu/Sn

All die-to-die bonding experiments were performed using an SET FC150 precision bonder with split optics, allowing for alignment in "cold placement" with accuracy of ±1 µm. Prior to bonding, the Cu bottom pads were treated with a dilute sulfuric acid solution to remove copper oxide. The Cu/Sn top pads were treated with RTI's Plasma Assisted Dry Soldering (PADS) process [5] which enables fluxless bonding. The bonding was performed using a pressure of 5×10^6 kg/m^2 at a temperature of 250°C for 180 s under N_2 gas flow. Bonded die pairs consisting of Si "top die" to Si "bottom die" were used as control samples, and bonded InP "top die" to Si "bottom die" as experimental samples. Destructive die shear testing was done on select die pairs using a Dage 8400 bond tester with a 100 kg load cell. After bonding, half of the die pairs were selected at random for capillary underfill with a developmental, one component, unfilled epoxy with a cure temperature of 170°C.

III. RESULTS AND DISCUSSION

A. Mechanical Testing

Four InP–Si die pairs were chosen for destructive die shear testing. The shear values recorded from these samples were 15.8 kgf, 11.4 kgf, 22.6 kgf, 35.1 kgf. The failure interface was in the Cu-Sn intermetallic portion of the bond for the first three samples. The failure mechanism for the fourth die appeared to be mainly fracturing of the InP die. These shear values are comparable to Si–Si values of 18.1 kgf and 44.3 kgf, and they substantially exceed the 2.5 kgf value that MIL-STD-883G recommends for a die of this size [6].

B. Electrical Testing Prior to Thermal Cycling

The bonded die were electrically tested to determine, channel resistance, channel yield (defined as the number of open channels measured divided by 256, the total number of channels on each die) and the number of channels containing bonds that were shorted to each other. All 256 channels of each die were tested for electrical continuity in a 2-wire resistance measurement. Channels measuring above 15 kΩ were designated as opens and channels measuring below 60 Ω were designated as shorted. The results of the initial electrical testing are shown in Table 1. The median channel resistance of the die pairs was 70 – 89 Ω for InP-Si die pairs and 73 – 74 Ω for Si-Si die pairs, except for sample no. 1 which was bonded at a lower temperature. The average channel yield for both Si–Si die and InP–Si die pairs was comparable; 97.9% and 97.1%, respectively. Assuming that the open channels were due to randomly scattered bond defects, these channel yields correlate to an estimated interconnect operability of the 640 x 512 arrays of greater than 99.99%. The details of the extrapolation method are found here [2]. Before thermal cycling the electrically open channels were randomly scattered.

TABLE 2. AS-BONDED VS. POST THERMAL CYCLING ELECTRICAL YIELD AND RESISTANCE DATA

	Electrical Connectivity (% channels)			Median Channel Resistance (Ω)		
Die IDs	As-Bonded	Post Thermal Cycling	Avg. Change	As-Bonded	Post Thermal Cycling	Avg. Change
1	96.9	97.7	0.4%	148	147	0.4%
2	98.4	98.4		74	76	
3	96.9	96.5	-0.6%	74	74	0.0%
4	99.6	98.8		73	73	
5	96.5	87.1	-13.9%	81	84	1.7%
6	97.3	74.6		89	89	
7	98.4	89.8		70	71	
8	96.5	96.1	-2.8%	79	80	0.9%
9	98.0	96.9		70	71	
10	96.1	89.5		83	83	

C. Electrical Testing After Thermal Cycling

The Si-Si and InP-Si die pairs were exposed to 500 cycles of -40°C to 125°C with 20 min ramps and 10 min dwells at each temperature extreme. After thermal cycling the electrical testing was repeated. The comparison of electrical test results before and after thermal cycling for underfilled and not-underfilled die pairs is shown in Table 2. The average channel resistance of the die pairs did not show a significant change after thermal cycling for any of the four sample variations. The Si-Si die pairs exhibited less than 1% change in yield and average channel resistance for both underfilled and non-underfilled samples. This result correlates well with our previous work that examined thermal cycling of Si-Si die pairs bonded with Cu/Sn-Cu microbumps [2, 3]. The InP-Si die pairs without underfill exhibited a 13.9% decrease in channel yield after thermal cycling. The new channel opens seen after

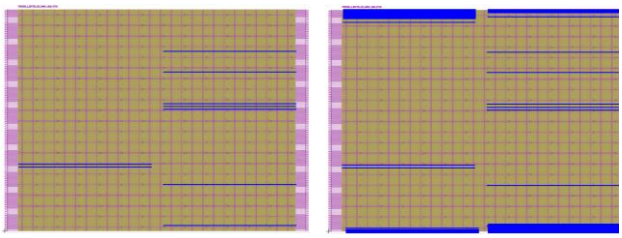

Fig. 5. Yield maps highlighting electrically open channels on a representative, non-underfilled InP-Si die pair (a) before and (b) after thermal cycling. Blue lines show the location of open channels. Before thermal cycling the opens are randomly scattered. After thermal cycling new open channels are congregated near the die edges.

thermal cycling occurred almost entirely in adjacent channels near the top and bottom edges of the die pairs. Figure 5 illustrates this effect with channel yield maps highlighting the open channels from a representative InP-Si die before and after thermal cycling. The average location of these new channel failures was within ten channels from the top and bottom edges. For any given channel in a heterogeneous die pair, the bumps that will see the largest amount of thermally induced stress will be those with the greatest DNP. Thus the point of bump failure in a channel is most likely near the left or right edge. The bumps at the edges of channels 10 and 118, which are ten channels from the top and bottom of each die, are 0.4 mm from the die corner or 3.9 mm radial DNP.

The InP-Si die pairs that were underfilled before thermal cycling exhibited only a 2.8% decrease in channel yield. Two of the three die pairs had less than three new open channels after thermal cycling, some of which were not near the top or bottom edges. The underfilled InP-Si die pair that exhibited the largest drop in the channel yield, sample 10, had a grouping of higher resistance channels near the edges before thermal cycling that was not seen in the other die samples and that corresponded directly to failures seen after thermal cycling, indicating a possible pre-existing weakness in some of the bump bonds near the die edges.

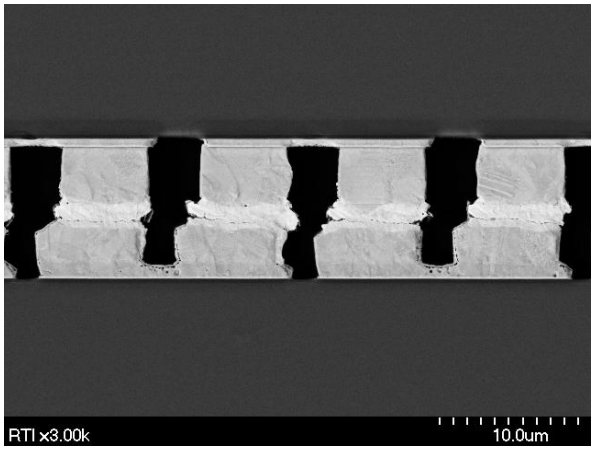

Fig. 6. Cross section SEM of a Si – Si die pair after capillary underfill and thermal cycling. The Sn has been fully consumed into Cu_3Sn intermetallic in the bondline.

D. Cross Section Analysis

After electrical testing to determine bond yield, cross-section samples were prepared from each device set. Die pairs that had not previously been underfilled were underfilled in preparation for the cross-sectioning; these samples will still be referred to as "non-underfilled". The cross-sectioning of the die pairs was done near channel no. 10, about 0.4 mm away from the edge of the array. The cross-sectioning was performed to examine possible failure mechanisms in the non-underfilled InP-Si die pairs, and then to compare the same device area in the underfilled InP-Si and Si-Si die pairs.

Figure 6 shows a cross-section SEM image taken of an underfilled Si-Si die pair. The free Sn from the bumps on the top die has been fully converted to Cu_3Sn intermetallic in the bondline. As expected from a CTE-matched die pair, the bond-to-bond alignment is consistent across the die from edge to edge. Some slight voids are seen in the bondline similar to what has been reported previously on highly reliable Cu/Sn interconnects [2, 3, 7].

Fig. 7 is a cross-section SEM image taken from a non-underfilled InP-Si die pair. As previously described, electrical testing of this sample revealed new opens after thermal cycling that occurred in the first 12 channels near the die edges. In this sample, cracks are seen to have developed in the bondline

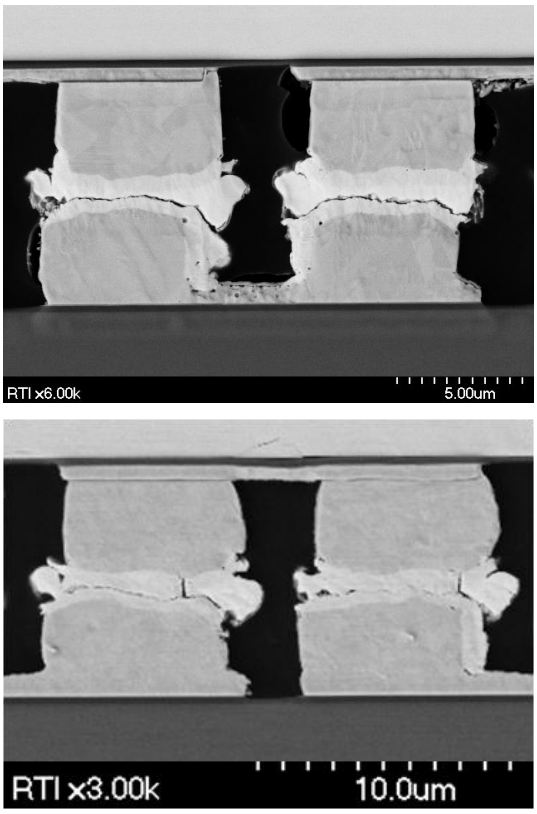

Fig. 7. Cross section SEM images of an InP – Si die pair without capillary underfill after thermal cycling taken 0.4 mm from the top edge of the array (which is into the direction of the page) and either a) 50 um from the right edge or b) 150 um from the right edge. In a) cracking has appeared along the original bond interface between the Sn of the top die and the Cu bump of the bottom die. In b) vertical cracks are apparent in the CuSn intermetallic.

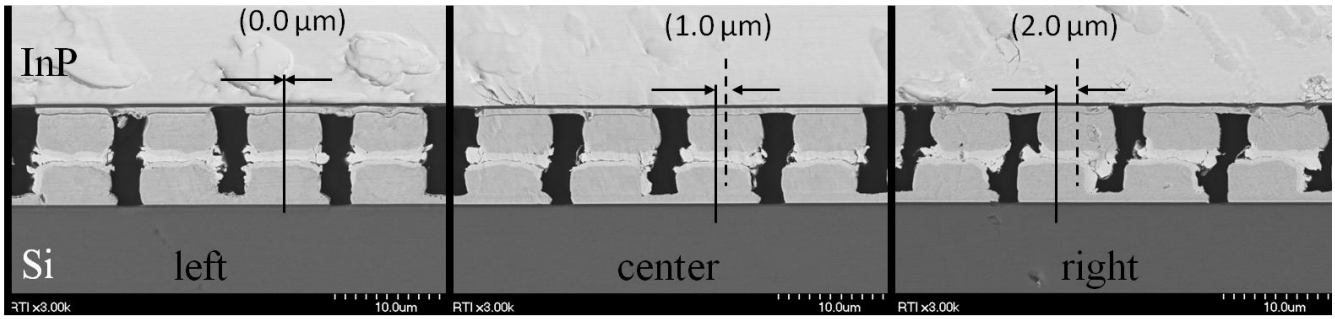

Fig. 8. Cross section SEM images taken from the left, center, and right side of a Cu/Sn bonded InP – Si die pair. The difference in CTE between the Si and InP die results in varying bump-to-bump alignment across the die.

along the original bond interface. The cracks seen in the bump pairs become more severe as the DNP increases. It is surmised that these cracks are the failure mechanism causing the decrease in electrically yielding channels near the die edges.

Fig. 8 shows a series of SEM images taken from an underfilled InP-Si die pair after thermal cycling. The bondline has slight voids similar to those seen in the Si-Si samples and does not exhibit the cracking seen in the non-underfilled InP-Si die pair. Unlike the Si-Si die pair, the bump to bump alignment shifts across the die. From the left side to the right side of the die, a 2 µm shift in the alignment is seen with the bumps on the InP die exhibiting an outward shift. This shift is expected because of the larger CTE of the InP die compared to the Si die. For a 6.4 mm × 5.12 mm array, the edge bumps of the InP array would be expected to shift outward at the bond temperature of 250 °C by 1.5 µm in x and 1.2 µm in y (2 µm in radially outward expansion), see Figure 1. Because the free Sn reacts with Cu and solidifies at 250 °C into Cu_6Sn_5 and then Cu_3Sn, the expansion of the die becomes locked in place at the bond temperature. From the SEM images, a shift of approximately 2 µm in x is seen in the alignment of the bumps across the array from left to right, compared to the 3 µm expected from the CTE calculation.

As mentioned before, as the bonded die pair cools down to room temperature, shear strain develops in the bonds. The crack generation observed in corner bumps in non-underfilled die after thermal cycling testifies to the presence of the stress that increases with the increasing DNP. When the die are underfilled with epoxy, the shear strain decreases as the epoxy locks the structure in place, distributes stresses more uniformly and adds mechanical strength.

IV. Conclusions

Large 640 x 512 area arrays of 10 µm pitch Cu/Sn bumps on InP die have been bonded to corresponding arrays of Cu bumps on Si substrates. Operability of the array was determined by electrical testing of long daisy-chains of bumps. The average channel yield was approximately 97% for both InP-Si and Si-Si die pairs translating into the array operability greater than 99.99%. The reliability of InP-Si and Si-Si die pairs was compared after 500 thermal cycles of -40 °C to 125 °C. No significant change in yield was seen for the homogeneous Si-Si die pairs. The InP-Si die pairs were underfilled using an experimental unfilled epoxy exhibited a 2.8% decrease in channel yield while those die pairs that were not underfilled saw a 13.9% decrease in channel yield. In the latter, the channels that failed in thermal cycling were predominately located near the edges of the die pairs indicating that the bump failures were due to the difference in thermal expansion between InP and Si. Cross sectional SEM images taken from the edge areas of both underfilled and non-underfilled InP-Si die pairs correlated well with the electrical results. The non-underfilled InP-Si die pairs showed evidence of cracks in the original bond interface that became larger as the DNP increased. SEM images taken from a similar location in underfilled InP-Si die pairs seem to indicate that the use of underfill was successful in preventing cracks.

The results described in this work indicate that Cu/Sn microbumps can be successfully and reliably used for the integration of InP and Si die in large area array format. Future work will focus on the generation of larger sample sets and longer term thermal cycling to further prove out the use of this metal system for heterogeneous 3D integration.

References

[1] A. Gutierrez-Aitken, *et. al., "*Advanced heterogeneous integration of InP HBT and CMOS Si technologies for high performance mixed signal applications," *IEEE Microwave Symposium Tech Dig*, pp. 1109-1112, 2009.

[2] M. R. Lueck, J. D. Reed, C. W. Gregory, A. Huffman, J. M. Lannon, & D. S. Temple. High Density Large Area Array Interconnects Formed by Low Temperature Cu/Sn-Cu Bonding for 3-D Integrated Circuits. *IEEE Transactions on Electron Devices*, *59*(7), pp. 1941–1947, 2012.

[3] J. D. Reed, M. R. Lueck, C. W. Gregory, A. Huffman, J. M. Lannon, & D. S. Temple. High Density Interconnect at 10µm pitch with Mechanically Keyed Cu/Sn-Cu and Cu-Cu Bonding for 3-D Integration. *Proc. of the 60th Electronic Components and Technology Conference*, pp. 500–507, 2010.

[4] M. Cohen and G. Olsen "Room-temperature InGaAs camera for NIR imaging", *Proc. SPIE* 1946, Infrared Detectors and Instrumentation, 436 (October 20, 1993); doi:10.1117/12.158695.

[5] N. Koopman and S. Nangalia, "Fluxless Flip Chip Solder Joining," in *Proc. NEPCON West*, 1995.

[6] US D. of Defense, "MIL-STD-883G, Department Of Defense Test Method Standard: Microcircuits," Section *2019.7*, 2006.

[7] R. Labie, P. Limaye, K.W. Lee, C.J. Berry, E. Beyne and I. De Wolf, "Reliability testing of Cu-Sn intermetallic micro-bump interconnections for 3D-device stacking", *Proc. of the* 3rd *Electronic System Integration Technology Conference*, pp. 1-5, 2010.