INTERCONNECT STRUCTURE FOR ROOM TEMPERATURE 3D-IC STACKING EMPLOYING BINARY ALLOYING FOR HIGH TEMPERATURE STABILITY

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ABSTRACT
Numerous metal contact stacks have been proposed for 3D-IC chip stack assembly. Copper is a popular choice for standoff posts since it is well-characterized and in regular production today. However, since direct Cu-Cu bonding is problematic due to planarity and oxidation issues, many development groups employ a Sn or SnAg solder cap on top of the Cu post, sometimes with a Ni diffusion barrier, to provide bondline compliance and to reduce bonding force and temperature. But this structure still requires reflow bonding temperatures around 250C or thermo-compression bonds around 185C. These thermal excursions consume energy and time, and will induce CTE-driven misalignment and stresses when bonding devices comprised of heterogeneous materials such as InGaAs, InP, or Si. Indium has been proposed as a replacement for Sn to allow room-temperature "cold-welding", but elemental indium melts at 156C and is not compatible with subsequent solder reflow assembly processes.

We propose depositing Ni\In onto the Cu post on one side of the bond interface, and Ni\Ag to the other side to create a metallurgical system which can be bonded at room temperature to create robust mechanical and electrical interconnects. An Atmospheric Plasma process is used to de-oxidize and passivate the In and Ag surfaces, followed by room temperature compression bonding of the In to Ag. Subsequent chip layers can be stacked in the same manner at room temperature without requiring thermal excursions for melting and solidification. Following completion and test of the stacked assembly, solid-state annealing will alloy the In and Ag layers, raising the melt temperature of the In/Ag alloy to above standard solder assembly temperatures.

We present details on device fabrication, pre-bond surface preparation, bonding profiles, interconnect yield and preliminary reliability testing for this promising interconnect structure.

Key words: 3DIC, Interconnect, Binary, Alloy, Atmospheric Plasma.

INTRODUCTION
Use of the vertical dimension – 3D – has received a great deal of emphasis and attention in the race to enhance electronic functionality while reducing footprint and cost. While using this vertical dimension may take many forms or employ several methodologies, this paper will focus on interconnect schemes to connect multiple chips directly to each other by means of micro-bumps, Through-Silicon-Vias (TSV's) and/or interposers, creating ultra-short, ultra-fast and low-loss signal paths between chips. These methodologies employing micro-bumps and TSV's in the vertical dimension may include 2.5D stacking, 3DIC, or 3D heterogeneous integration.

There is widespread effort into these various methodologies at a wide spectrum of universities, institutes and industrial chipmakers worldwide [1-6]. Several potential or realized applications for 2.5 or 3D are shown in Figure 1.

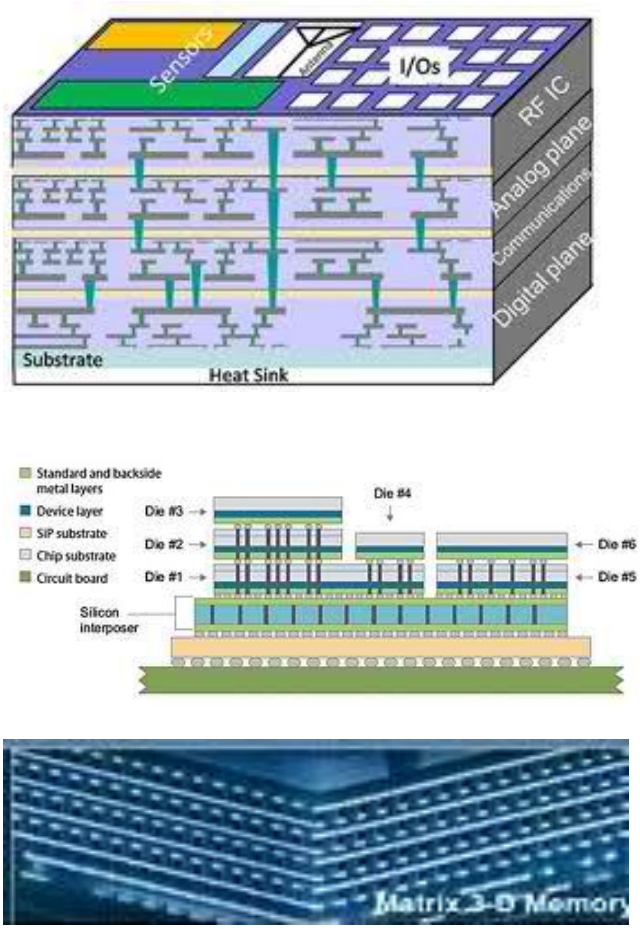

Figure 1, Examples of 2.5 and 3D structures

To meet performance and cost targets, feature sizes of the chips and interconnects must be carefully minimized in X, Y and Z. Thus, circuit designers will apply design rules with aggressive dimensions, increasing the need for high-performance interconnections due to reduced contact areas.

Many metallurgies have been proposed to meet the aggressive requirements of advanced interconnect. The familiar Pb/Sn and other alloys used widely in early consumer applications do not meet the needs of 2.5 or 3D, so copper has received a great deal of attention, largely due to its electrical and thermal performance as well as its widespread use in industry [4, 5, 7, 8]. Despite the many attractive properties of Cu, it readily forms oxides in many environments which inhibit either the bond quality of the initial joint or the long-term reliability of the Cu-Cu bond. Also, the mid-range modulus of copper requires considerable force-per-unit-area and elevated temperature to achieve the amount of physical deformation necessary to accommodate die flatness and surface morphology imperfections. In an effort to overcome these challenges, many development groups are employing solder caps on top of the copper posts to reduce bond time and temperature, and to provide some mechanical compliance to overcome flatness and morphology issues. Among the materials and solders under investigation to use a copper-based bonding scheme are Sn, SnAg and Ni. The many combinations and options often involve a copper post or bump capped with a compliant solder material and then bonded to an opposing copper-based bump or pad.

When the bumps on a chip have been formed, regardless of material, they must be aligned and joined to the opposing structure to form a bond with high mechanical and electrical integrity. Two of the primary methods of joining materials are reflow and thermocompression. The former has been widely used since IBM and Delco launched the C4 process, and entails heating the two parts until one or more of the bump materials reaches its melting point. At this point, the material begins to flow and to join itself to the opposing structure.

At relatively large dimensions and for single-stack processes, the reflow process works very well, producing many parallel bonds at high throughput and high yield. But as bump dimensions shrink, alignment tolerances grow tighter, and the fluid nature of the solder above its melting point cannot maintain sufficient XY alignment to ensure proper electrical and mechanical performance of the bond. Additionally, in multiple-stack methodology common to 3D integration, reflow of layer N may disrupt the bond quality achieved at layer N-1 or N-2. Another concern with applying reflow bonding to 3D Integration is that chips used in the stack may use substrate materials with widely disparate coefficients of thermal expansion (CTE); this can lead to unacceptable misalignments when joining large chips with small bump pitch at higher temperatures.

Thermocompression bonding, wherein force, rather than temperature is the primary driver of the bonding process, has also been employed for many applications. Thermocompression (TC) bonding, depicted schematically in Figure 2, provides some advantages over reflow. For

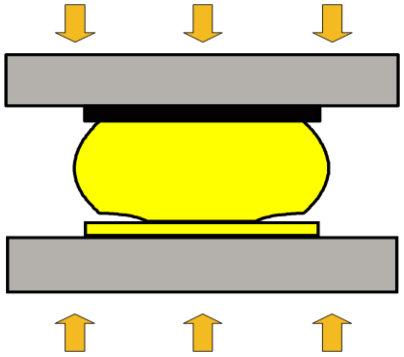

Figure 2, Thermocompression bonding

starters, the elevated temperatures required to reflow many common solders are not required, reducing the runout due to CTE mismatch [9]. Furthermore, bonding many chips in succession at/near room temperature to form a vertical stack does not degrade the alignment achieved with previous bonds. Joints formed by TC bonding show very good mechanical stability, and are thus able to maintain alignment through many bonding cycles. Thermocompression bonding also lends itself very well to very dense connections, because the joint is formed at very low temperatures, preventing the solder from flowing to neighboring bonds and creating electrical shorts.

One more important consideration must be made, however. Even if the 3D-IC stack can be fabricated at temperatures below the melting point of the solders utilized, the final assembly still has to stand up to subsequent reflow processes during "next-higher-assembly". Re-melting of the 3D-IC connections (after subcomponent test) introduces significant risk to the operability and/or reliability of the final product, therefore the 3D-IC stacking bond should remain solid at standard reflow temperatures (>260C).

So, an ideal interconnect design and process must contain the following attributes:

- Production-compatible (plate-able) bump metallurgy.
- Good thermal, mechanical, and electrical properties and reliability.
- Mechanical compliance to reduce bond force and temperature.
- Thermo-compression bond-ability at low temperature and in room ambient conditions.
- Above-normal melting point to survive next higher assembly.

We propose here just such a design and process.

METHODOLOGY:

We propose a metal interconnect scheme in Figure 3. Copper posts on the lower chip are capped with nickel (as a diffusion barrier) and then silver. Copper posts on the opposing chip are capped with nickel (as a diffusion barrier) and then indium. Following normal dicing, demount, and cleanup, Atmospheric Plasma is used on both chips with reducing chemistry to remove oxidation from the Ag and In contact surfaces, and then atomically passivate the dangling bonds on those surfaces to inhibit re-oxidation. The prepared chips are then thermo-compression bonded at low temperature, utilizing the low-modulus compressibility of the indium to form a void-free compression bond to the silver of the lower bump. Elimination of oxidation from the bumps before bonding enables a stable, strong "cold-weld" bond between the In and Ag, even at room temperature.

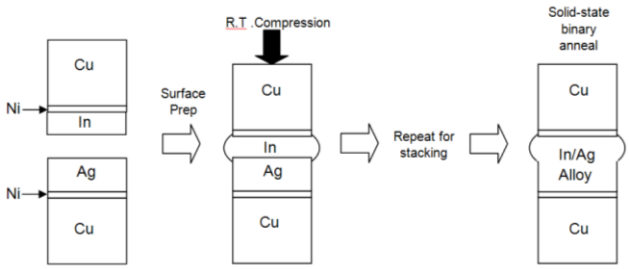

Figure 3, Proposed interconnect design and process.

Subsequent chips can be stacked onto this bonded pair immediately to form the 3D-IC stacked structure. At this point, the 3D stack can be tested for interconnect functionality, even though there is still indium in the stack that would melt if raised above 156C. However, by increasing the temperature of the assembly (but remaining below 156C), a solid-state diffusion of indium into silver and silver into indium will create an alloy composition (nominally Ag_2In) that readily withstands temperatures above 650C [10]. This fulfills the important criterion of being able to undergo subsequent standard reflow assembly processes without re-melting.

To test this concept, chip pairs were designed and fabricated with the bump stack described above. The chip designs utilized a copper interconnect layer to form "daisy-chain" interconnect test structures for resistance, interconnect yield, and shear testing.

TEST VEHICLE FABRICATION

To generate die for the interconnect bonding experiments, we fabricated "top die" and "bottom die" routing metal patterns on Si wafers. The routing metal connects the 640 x 512 array of microbumps on a 10 µm pitch into electrically testable channels. The "top die" patterns were formed on 75 mm Si wafers, while the "bottom die" patterns were fabricated on 200 mm Si wafers. The bottom die are slightly larger than top die to accommodate probe pads for each channel. Each channel consists of 1280 bonds connected in series for two wire resistance measurement. In this layout, a single nonfunctional bond renders the channel electrically open. The routing pattern is illustrated in Figure 4. The Si wafers were test grade, (100) orientation, and were either 725 µm thick for 200 mm wafers or 380 µm thick for 75 mm wafers.

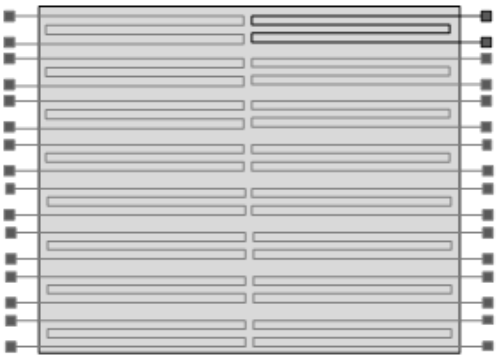

Figure 4, Schematic diagram of the testing structure in plan view showing the layout of the individual test channels. Each die contains 128 channels on each side and each test channel contains 1280 microbumps connected in series.

The process flow used to fabricate the routing layers and microbumps on the Si wafers is shown in Fig. 5. Routing metal was deposited by e-beam evaporation and patterned by metal lift-off.

The metal was 0.5 µm thick Cu with an adhesion underlayer of Ti. A plating seed layer consisting of another Ti adhesion layer and a 0.15 µm thick layer of Cu was sputtered on all wafers. Next, an 8 µm thick layer of AZ9260 positive photoresist (AZ Electronic Chemicals) was spun on both sets of wafers and patterned using contact lithography to form a plating template for the arrays of microbumps. On the "top die" wafers, the microbumps were plated with 1.2 µm of Ni then 2 µm of In.

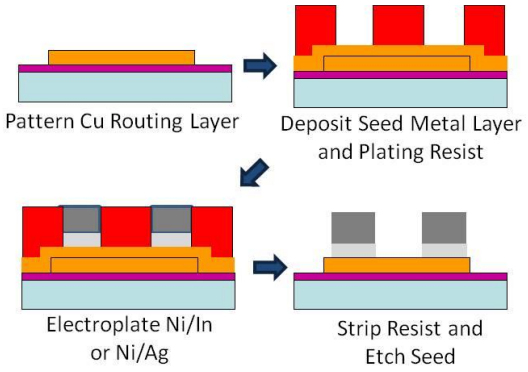

Figure 5, Diagram of process used to form routing metal and 10 µm pitch Ni/In or Ni/Ag microbumps.

The Ni was plated using a nickel sulfamate plating bath from Technic, Inc. The In was plated from an indium sulfamate bath from Indium Corp. The "bottom die" wafers were plated with 1.2 µm of nickel and 4 µm of Ag. Here the Ni plating step was followed with a Wood's nickel strike to improve adhesion of the subsequent Ag plating. The Ag was

plated using a cyanide-free silver bath, Techni Silver Cyless II from Technic Inc. Cyanide-based silver baths are reported to have good adhesion to bright nickel without requiring a Wood's nickel strike step. [11]

The ratio of the Ag bump height to the In bump height was intended to be 2:1 in order to form a Ag_2In alloy after bonding.

Ion milling was used to remove the seed layer from between the routing metal links. For the indium-bumped wafers, ion milling was found to remove an excessive amount of indium, so for these wafers, wet etching was used to remove the copper and titanium seed layer. Electrical testing was used to verify electrical isolation between adjacent bumps and the routing metal.

DIE BONDING AND ALLOYING EXPERIMENTS

All die-to-die bonding experiments were performed using an SET FC150 precision bonder with split optics, allowing for alignment in "cold placement" with accuracy of ±1 µm.

The treated dice were tack-bonded at room temperature at room temperature using a force of 32Kg (0.1 grams per bump). The bond force was held for a duration of 15 to 30 seconds. The hybrid was then annealed at various time-temperature-force profiles to interdiffuse the indium and silver layers.

Table 1 shows interdiffusion times and temperatures as well as average electrical resistance per bump, daisy chain channel yield, and shear strength measurements.

Anneal Temp	Ramp up time	Hold Time	Avg. Ω/bump	Yield to opens	Yield to shorts	Shear/ mil spec
135C	20 sec	600 Sec	0.248	98%	98%	242%
190C	60 sec	90 sec	0.108	93%	96%	172%
190C	240 sec	90 sec	0.084	100%	98%	no test

Table 1, Anneal conditions and test results.

RESULTS AND DISCUSSION

The bonded dice were electrically tested to determine channel resistance, channel yield to opens (defined as the number of fully connected channels divided by the total number of channels on each die) and channel yield to shorts (defined as the number of non-shorted channels divided by the total number of channels on each die). All 256 channels of each die were tested for electrical continuity in a 2-wire resistance measurement. Channels measuring above 15 kΩ were designated as opens and channels measuring below 60 Ω were designated as shorted. The results of the initial electrical testing are shown in Table 1.

Bonded pairs were shear-tested in accordance with MIL-STD-883 which specifies die shear strength for this size die as 5.0 kg. Although shear data (see table 1) is limited, shear strengths on all samples measured did easily exceed the MIL-STD requirement. More data is required for statistical validation, however, the current data suggest that this bond scheme is capable of robust mechanical performance.

After electrical testing to determine bond yield, cross-section samples were prepared using a Focused Ion Beam technique. Energy-Dispersive X-ray Spectroscopy (EDS) was performed on the cross-sectioned samples to determine the extent of inter-diffusion between indium and silver. Figure 6 shows such a cross-section

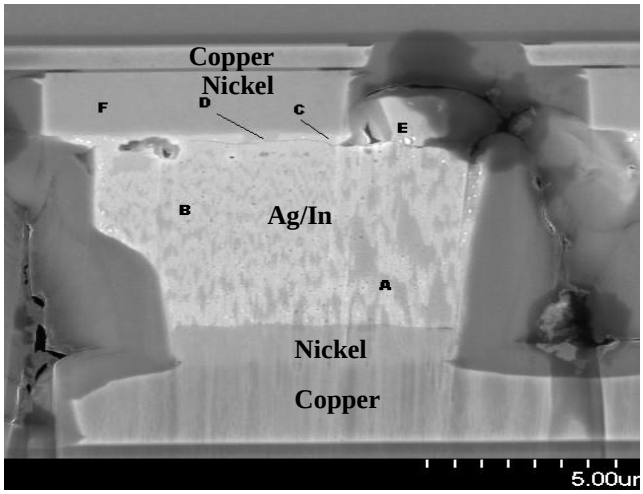

Figure 6, Bond cross-section showing EDS locations

The cross-section is labeled to show the locations of the EDS measurements (A through F), as well as the main components of the metal stack. Table 2 shows the EDS composition results.

	A	B	C	D	E	F
Ag	95.7%	67.6%	58.8%	25.1%	33.0%	0.0%
In	4.3%	32.4%	37.9%	65.1%	59.0%	0.0%
Ni	-	-	-	-	-	100.0%
Cu	0.0%	0.0%	3.3%	9.8%	7.2%	0.0%

Table 2, EDS composition in the regions labeled in Fig, 6

In Region B the expected Ag_2In ratio has been achieved. However, Region A has only a small portion of diffused indium. This could indicate either (1) there was insufficient time/temperature to complete the diffusion process, or (2) the free indium has been consumed in Region B and is not available to diffuse further into the silver bump. Regions C, D, and E show some copper in the EDS analysis. We speculate that there was some Cu on the top surface of the Ag bump before bonding, due to the ion milling used earlier to remove the plating seed layer. This Cu could also be responsible for some voids which appear in the bond interface region. The next round of tests will revise the process to ensure that there is no Cu in this region.

CONCLUSIONS

Preliminary results are encouraging, though additional investigation is needed. Reasonable values for bump resistance, and reasonable short/open yields can be obtained in extended daisy-chain strings with the proposed interconnect structure. Additionally, shear strength of the bonds (without underfill) is capable of exceeding MIL-STD die shear requirements. We plan to refine our processes to optimize silver/indium interdiffusion and to characterize shear strength with a broader sampling. We also plan to verify the mechanical and electrical stability of the structure at typical solder reflow temperatures to ensure that the structure can withstand subsequent assembly by standard industrial solder reflow techniques.

REFERENCES:

1. D. Malta, et al., "Characterization of thermo-mechanical stress and reliability issues for Cu-filled TSV's," *Proc 61st Electronic Components and Technology Conf*, Orlando, FL, May 2011, pp. 1815-1821.
2. P. Andry, et al, "Low-Profile 3D Silicon-on-Silicon Multi-chip Assembly," *Proc 61st Electronic Components and Technology Conf*, May 2011, pp. 553-559.
3. J. Maria, et al., "3D Chip Stacking with 50um Pitch Lead-Free Micro-C4 Interconnections," *Proc 61st Electronic Components Technology Conf*, May 2011, pp. 268-273.
4. K. Hummler, et al., "TSV and Cu-Cu direct bond wafer wafer and package reliability," *Proc 63nd Electronic and Component Technology Conf*, June 2013, pp. 41-48
5. M. Farooq, et al., "3D Copper TSV integration, testing and reliability, *Proc IEDM Conference*, Session 7.1, 2011
6. J.H. Lau, et al., "Feasibility study of a 3DIC integration system-in-package (SiP) from a 300mm multi-project wafer (MPW)," *Journal of Microelectronics and Electronic Packaging*, vol. 8, no. 4, pp. 171-178, 2011.
7. R. Agarwal, et al., "High Density Cu-Sn TLP Bonding for 3D Integration, *Proc 59th Electronic Components and Technology Conf*, 2009.
8. J. Lannon Jr., et al. "High Density Cu-Cu Interconnect Bonding for 3D Integration" *Proc 59th Electronic Components Technology Conf*, May 2009.
9. M. Lueck, et al., "High Density Interconnect Bonding of Heterogeneous Materials Using Non-Collapsible Microbumps at 10 μm Pitch," *Proc 4th IEEE 3DIC Conference*, San Francisco, CA, October 2013.
10. R. W. Chuang and C. C. Lee. "Silver-indium joints produced at low temperature for high temperature devices." *IEEE Transactions on Components and Packaging Technologies* (2002), pp. 453-458.
11. Chicago Metal Finishers Institute. (2002). *Non-Cyanide Silver As a Substitute For Cyanide Processes.* Champaign, IL: Illinois Waste Management and Research Center. Retrieved from http://www.istc.illinois.edu/info/library_docs/rr/RR-94.pdf