High Accuracy Chip-to-Chip or Chip-to-Wafer Bonding methods for 3D-IC integration

Gilbert Lecarpentier
SET S.A.S. (Smart Equipment Technology), 131 Impasse Barteudet, 74490 Saint Jeoire, France

Abstract

3-Dimensional interconnection of high density integrated circuits enables building devices with greater functionality with higher performances in a smaller space. The high density Through-Silicon-Via (TSV) with diameter down to five microns and below, together with the larger chip size increase the placement and bonding accuracy requirements. Die-to-Die and Die-to-wafer bonding are attractive and promising high yield methods thank to the benefit of the known good die concept. Chips from one wafer are diced and then joined to another die or to a wafer; thus, only good dice are joined together and dissimilar technologies can be assembled. There are several bonding processes that can apply to 3D-IC integration, In-situ bonding method (reflow or thermo-compression) which may require oxide removal to guarantee good and reliability bonding. Oxide removal using formic acid vapor is a solution, but it is time consuming. In order to meet the throughput requirements in a production environment, a two-step approach where all chips are accurately placed and secured onto the wafer prior to moving to another machine or station where a global bonding will be performed is a preferable method. This paper explores the chip-to-chip and chip-to-wafer alignment schemes and the associated bonding techniques, including in-situ reflow or thermo-compression with a local oxide reduction which contributes to higher yield together with reduction of the force or temperature requirements. Solutions for maintaining the chip in place adapted to the two steps placement and bonding approach are explored; it includes placement using polymer for pre-attachment and direct metallic bonding which can be performed at room temperature and low force.

1. Introduction

The Moore's law [1] has shown for decades density increase by 2D scaling. 3D interconnection enables the continuation of the Moore's law by using the third dimension. Wafer bonding techniques have been used for decades in various areas of microelectronics. It implies that chip dimension are identical for all layers and the yield decreased dramatically with the number of layers [2]. Die-to-wafer bonding is an attractive and promising method, in which chips from one wafer are diced and then joined to another die or to a wafer [3]. Only good die are joined together and dissimilar technologies can be joined. With the introduction of high density Through-Silicon-Via (TSV) with diameter down to 5µm and below, together with the chip size increase, the Chip-to-Wafer Post Bond alignment accuracy becomes more stringent. Not only lateral positioning is important, but the parallelism of the die with respect to the wafer becomes a critical parameter.

2. Chip-to-Chip and Chip-to-Wafer Bonding

Chip Stacking and Chip-to-Wafer (C2W) bonding approaches suffer of a potentially lower throughput when compared to Wafer-to-Wafer Bonding (W2W). With chip stacking, each die is placed individually; however, solutions are being investigated to enable global bonding after chip placement. The lower throughput is balanced by the benefit of bonding known good die to known good bonding site of the wafer, increasing the yield significantly. Chip-to-Wafer (C2W) assembly method enables mixing heterogeneous technologies, side by side or stacked. Chip-to-Wafer bonding is also used for wafer reconstruction, chip resizing and connection redistribution to achieve 3D Die-stack of different technologies [4].

In situ bonding enbles high accuracy placement because the position die positionning is controlled by the bonder during the whole bonding sequnce. Most bonding techniques used for die-attach or flip-chip bonding (fig. 1) can be applied:

- Reflow soldering,
- Thermo-compression including Cu-Cu bonding [5],
- Insertion bonding [6],
- Thermo Sonic bonding,
- Adhesive Joining
- Fusion Bonding (heterogeneous integration) [7].

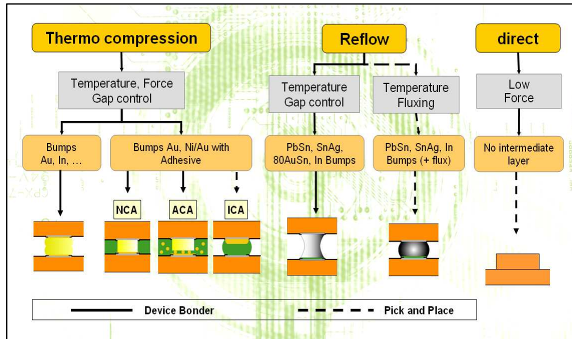

Fig. 1: Flip Chip processes

Collective bonding techniques enable higher throughput; however maintaining the initial placement during the final bond is challenging and is putting more constraints on material selection.

3. Collective bonding approaches.

In-situ die bonding performed on high precision bonder like the SET-FC300 enables accurate placement. The throughput is limited by the bonding time. This sequential bonding technique well adapted to Die-to-Die bonding results in multiple temperature cycles for the landing wafer.

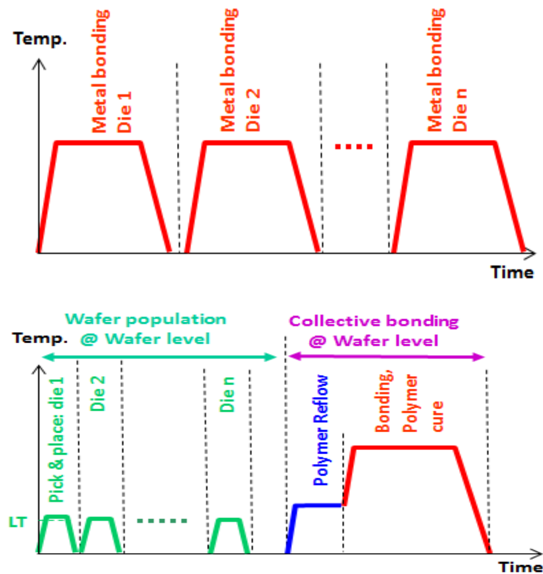

Fig. 2: Thermal cycles seen by landing wafer: In-Situ (sequential) bonding vs. Collective Bonding

Collective die-to-wafer bonding is time efficient and the landing wafer sees only one temperature cycle. The accuracy depends upon pre-attachment method and global bonder capability to maintain the relative placement of the dice on the landing wafer.

4. Die-to-wafer techniques with 2-Step approach

Several placements methods securing the die in place during global bonding are being investigated.

a. insertion approach

The “insertion” technique [8, 9] is a flip-chip technique using micro-tubes (fig. 3) and solder lands (fig. 4) to aim at achieving ultra fine pitch (< 10 µm) and high bumps count (4.10^6) connections.

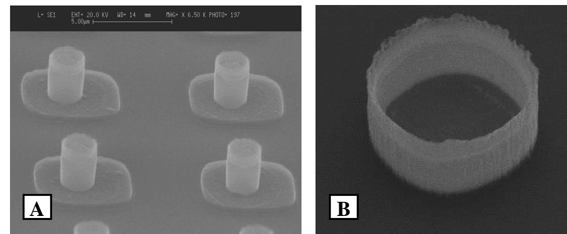

Fig.3: µtubes fabrication results - Top Views

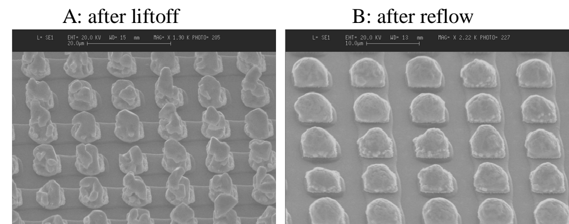

Fig. 4: SEM images of 10µm indium solder bumps made by lift-off technique

b. Tacking by adhesive

Cost effective processing by segmentation of 3D assembly (fig. 5) has been demonstrated using a photo-patterned polymer [10] to secure the dice after accurate placement performed on the SET-FC300.

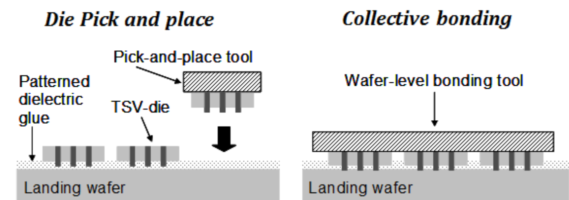

Fig. 5: 2-Step 3D-Assembly using photo-patterned adhesive

The Collective Bonding is performed on a Wafer Bonder; force and temperature are increased and the Polymer is reflowed. It is a critical step as die shifting might occur.

An alternative to photo-patterned adhesive which requires additional photolithography steps is the utilization of a photo-decomposable adhesive [11] (fig. 6).

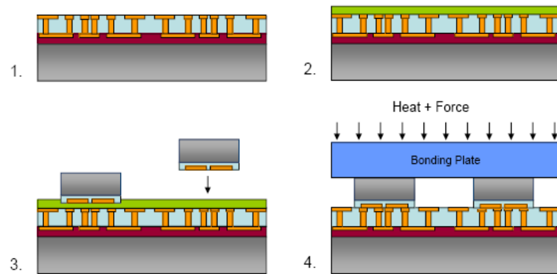

Fig. 6: -Step 3D-Assembly using photo-decomposable adhesive

The adhesive is spin coated onto the landing wafer. Dice are placed sequentially using high accuracy die bonder, then the wafer is moved to a wafer bonder where force and heat is applied forcing the decomposition of the adhesive and bonding all dice in parallel.

c. Direct metallic bonding

Direct metallic bonding (fig. 7) is performed at room temperature, atmospheric pressure and low force. It provides high mechanical and electrical integrity.

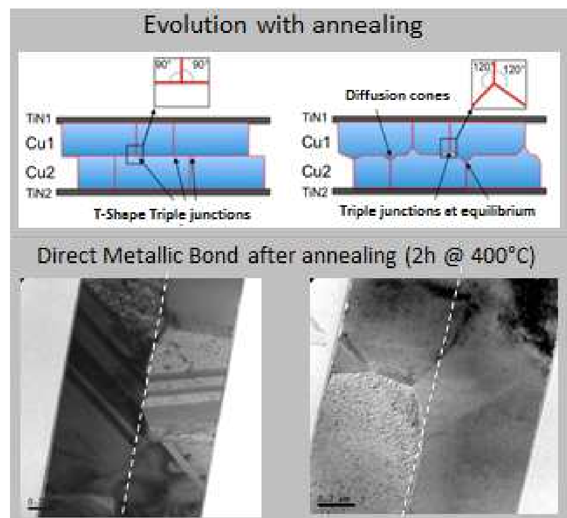

Fig. 7: Direct metallic bonding (Cu-Cu)

Unlike the eutectic solder assembly, the direct bonding interface is void-free, resulting in lower electrical resistance, higher strength, and better reliability.

The FC300 (fig. 8) used for this direct metallic bonding experiment features 0.5µm placement accuracy. Final bonding is performed by annealing and as no impact on the initial placement accuracy.

Fig. 8: Die bonder SET-FC300, modified to reach the level of particle contamination enabling direct metallic bonding

5. Oxide removal prior to Cu-Cu bonding

Because of its excellent electrical properties, copper is used more and more in die interconnection. Oxide that appears at standard temperature and pressure must be removed for successful bonding.

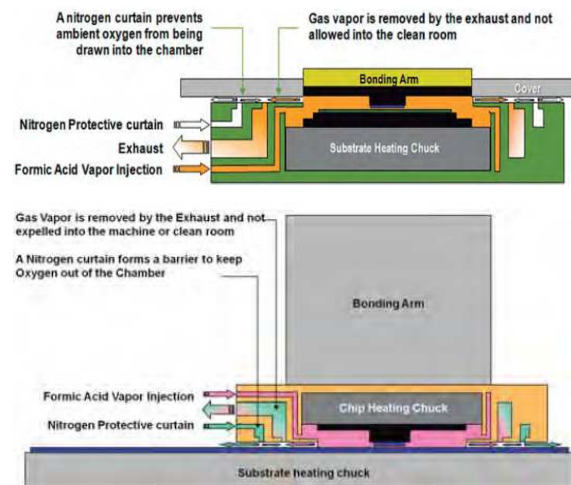

Fig. 9: Localized confinement chamber (C2C/C2W versions)

Local confinement chamber (fig. 9) built into the bonding tool uses reducing gasses, such as forming gas or formic acid vapor, to safely reduce the oxides immediately prior to bonding.

The chamber is created by using a non-contact virtual seal between the bonding head and the substrate chuck, ensuring gas collection and preventing oxygen intrusion.

6. Conclusions

High density 3D-IC integration is now moving to production. Die-to-Wafer with a 2-Step bonding approach is a cost effective, high yield and flexible solution for 3D-IC assembly. A variety of bonding technologies enable high volume manufacturing implementation of the various 3D bonding schemes using D2D or D2W approaches.

7. References

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