High Accuracy Chip-to-Chip or Chip-to-Wafer Bonding methods for 3D-IC integration

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OUTLINE

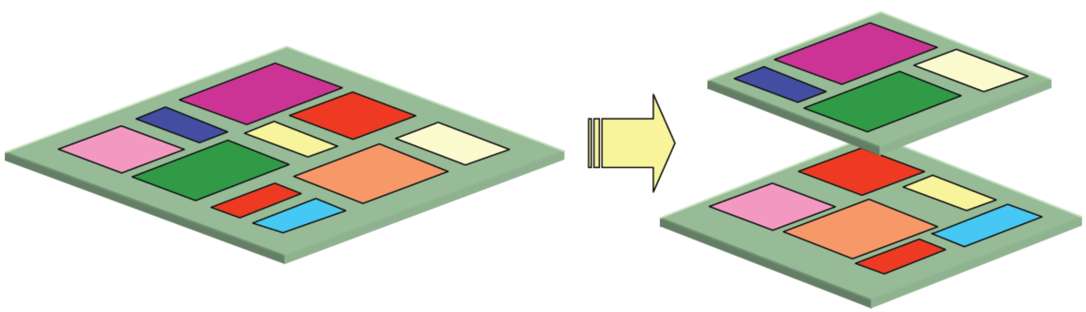
- Introduction
- Placement schemes
- Bonding schemes
- Oxide reduction
- Summary

INTRODUCTION
3D ASSEMBLY BY CHIP OR WAFER STACKING

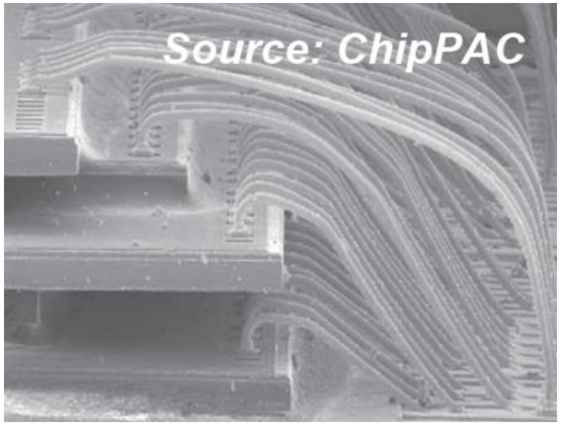
- Multifunction Devices (heterogeneous integration)
- Higher Packaging Miniaturization

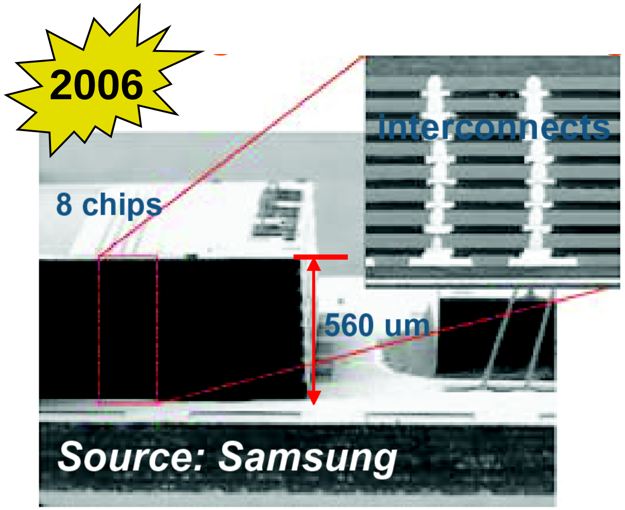
Repartitioning

- Reduces area of individual chips (Yield improvement)
- Reduces number of mask levels per die (Cost reduction)
- Results in much shorter global interconnect lines for better performances



INTRODUCTION





- Established 3D Packaging Technology

  Stacked Dice interconnected using Wire bonding technology is widely used

  - Peripheral, Long wire bonds
  - Low-density interconnects

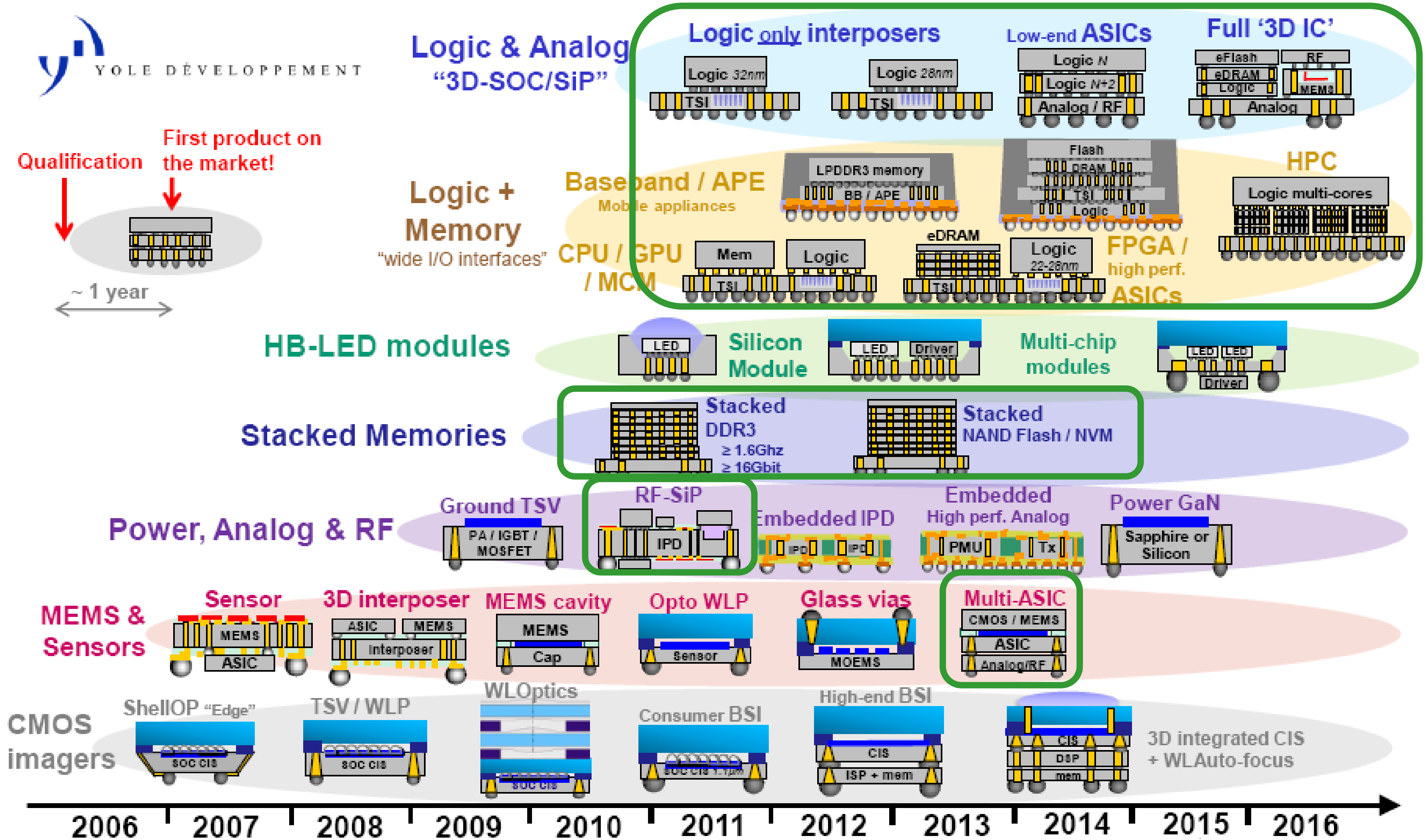
- 3D-Integration, Memory stack with TSV

  - Higher 3D-Interconnect density
  - Increased performance

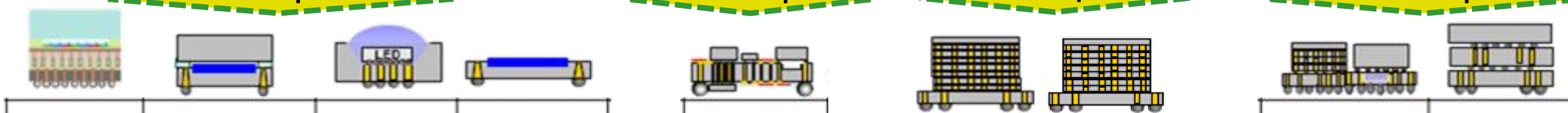
    Shorter connection

    Lower Capacitance and Inductance

GLOBAL ROADMAP FOR 3D-IC WITH TSV (2009)



3D TSV PACKAGING APPLICATIONS / PLAYERS



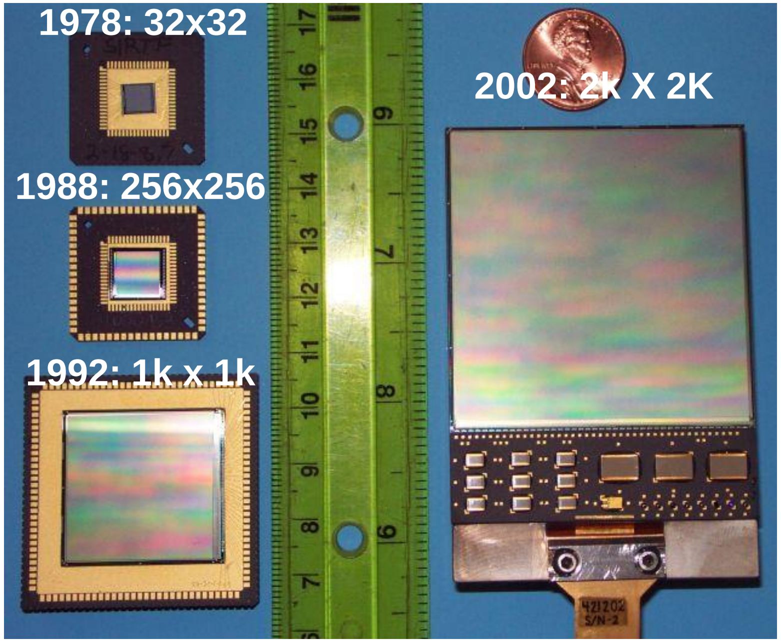
	> 10 µm				3 ~ 10 µm	2 ~ 5 µm		0.5 ~ 1 µm	
Application	CMOS image sensors	MEMS & Sensors	HB-LED Modules	Power & Analog components	Wireless SiP	Stacked DRAM modules	Stacked NAND Flash packages	'Logic + Memory' SiP modules	Logic / Analog / eMem 3D-SOCs
Description	WLP CIS, BSI sensors, WLAuto-focus	Interposer and caps for gyroscopes, accelerometers, microphones, pressure sensors, RF-MEMS (FBAR, resonnators, switches…), microfluidic, micro-probes, optical (opto sensors, micro-mirrors, laser, VCSELs) and display (OLED) applications…	Silicon interposer WLP modules	PA, MOSFET, IGBT, DC/DC converters, interface ICs…	RF IPD and interposers for tunable radio FEM, WLAN, Bluetooth, UWB, MMICs…	mem+mem stacking in BGA/PoP modules only	interposers and mem+mem stacking in BGA / TSOP / PoP modules only	Digital interposers and stacked memories (DRAM, Flash) for Baseband/DSP, FPGA, GPU, CPU…	Basebands, DVB / DAB modules, low-end ASICs, high perf ASICs, MCU, eRAM, SRAM, NVM…
Players	Tessera, Aptina, ST, Tezzaron, IBM, Dalsa, SMIC, JLCSP, jcap, Xintec, AWLP, Panasonic, UMC, Sony, Dongbu, Samsung, SMIC, Hynix, Sharp, ZyCube, Toshiba	imt, Dalsa, Panasonic, Silex, Avago, Alien, Chartered, Epcos, Epson, Texas Instruments, Freescale, IBM, ST, VTI, Sensonor, UMC, Omron, Hamamatsu, SMIC, Nepes, ae, DNP, Sony, tsmc, Samsung, apm, Sony, JLCSP, AWLP, Xintec	tsmc, Hymite, Texas Instruments, LG Innotek, ChipMOS, Micron, apm, Shinko, imt, Avago, ST, ipdia, Toshiba	Avago, National Semiconductor, Texas Instruments, ST, NXP, Amkor, IBM, Vishay, IOR, Panasonic	ipdia, Silex, ST, ON, TriQuint, Avago, Panasonic, apm, STATSChipPAC, IBM, tsmc, Texas Instruments, Infineon, Vishay, muRata, DNP, imt	Samsung, Hynix, Micron, Elpida, Nanya, Toshiba, VCI, Tessera, ChipMOS	Samsung, Hynix, Micron, Toshiba, DNP, IBM, SanDisk, Seagate, VCI, Tessera, STATSChipPAC	Samsung, IBM, Xilinx, LSI, Altera, Dongbu, Qualcomm, Texas Instruments, Infineon, ST Ericsson, NEC, UMC, Fujitsu, tsmc, Intel, Avago, Amkor, Sony, Nepes, Freescale, STATSChipPAC, TAC, Shinko, Toshiba, Chartered, SPIL, Broadcom	IBM, Infineon, Renesas, Qualcomm, Texas Instruments, Infineon, ST Ericsson, NEC, UMC, tsmc, Intel, Avago, Amkor, Nepes, Freescale, STATSChipPAC, TAC, Shinko, Chartered, SPIL, Broadcom
Market size in million wafer/year (2015)						~1.0	~1.8	~4.3	~1.0

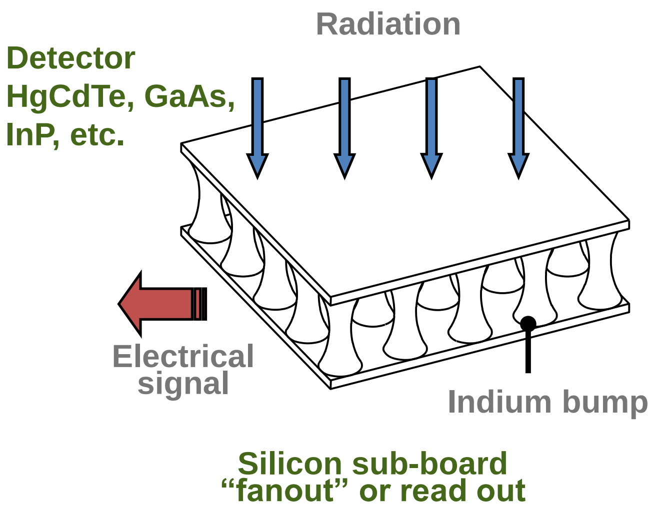
MAIN SET DEVICE BONDERS APPLICATIONS
PIXEL DETECTORS (IR, UV, X-RAY)

IR FPAs CAN NEVER HAVE TOO MANY PIXELS!

- Small bumps (< 5 µm)
- Fine Pitch (< 10 µm)

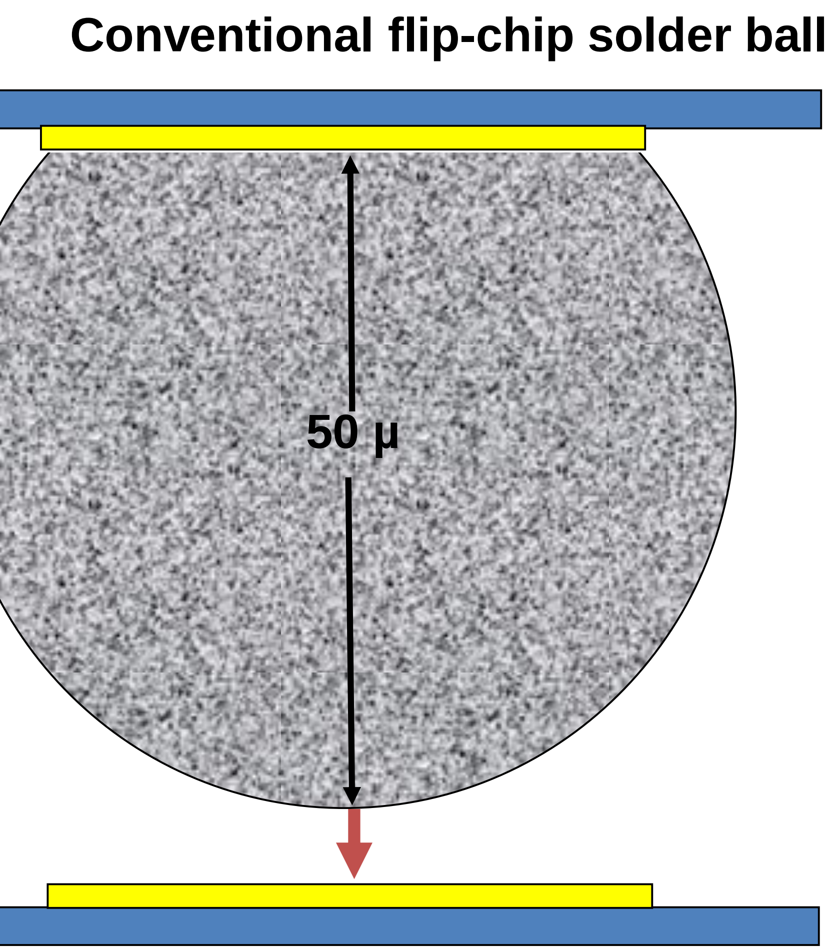
→ High Accuracy Placement and Tight Parallelism Control

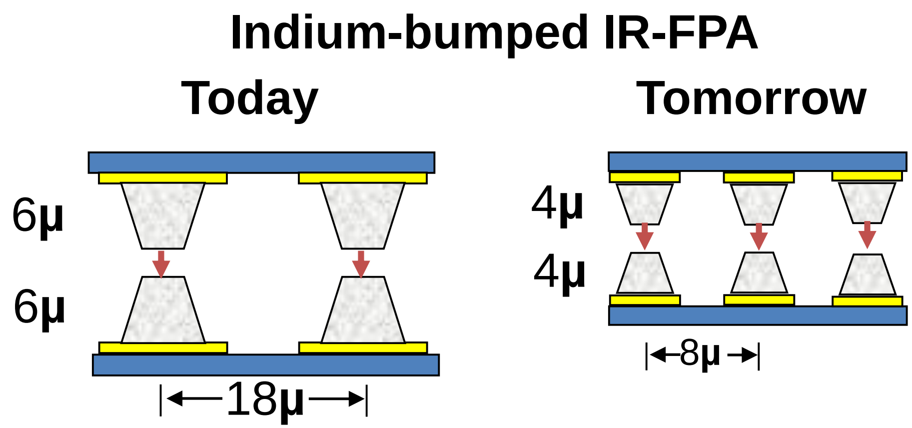




Requirements for assembly of 3D Interconnect using High Density TSV technology converge with those of IR-FPA assembly which have demonstrated for decades, successful Heterogeneous Integration of Low Pitch devices.

IR-FPA CHALLENGES: SMALLER PIXEL/BUMP SIZE → SIMILAR TO 3D-IC REQUIREMENTS





- High Accuracy Parallelism and Alignment, Process Flexibility and Heterogeneous Integration are available
- High Throughput Required for 3D-IC adoption, still need to be addressed

PLACEMENT AND BONDING SCHEMES

PLACEMENT

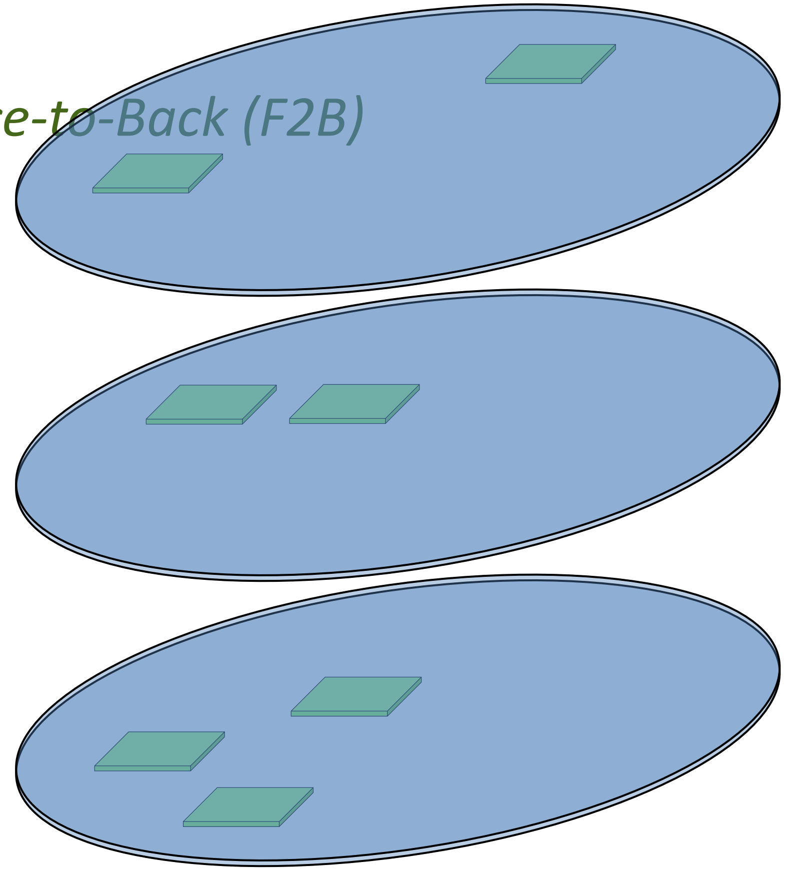
- Wafer-to-Wafer Bonding (W2W)
- Die-to-Die (D2D / C2C); Die-to-Wafer Bonding (D2W / C2W)

BONDING

- In situ Bonding
  - Thermocompression
  - In-Situ Reflow
- Sequential placement followed by gang bonding

WAFER TO WAFER (W2W) BONDING

Wafers are bonded Face-to-Face (F2F) Face-to-Back (F2B)



- ☺ High Throughput

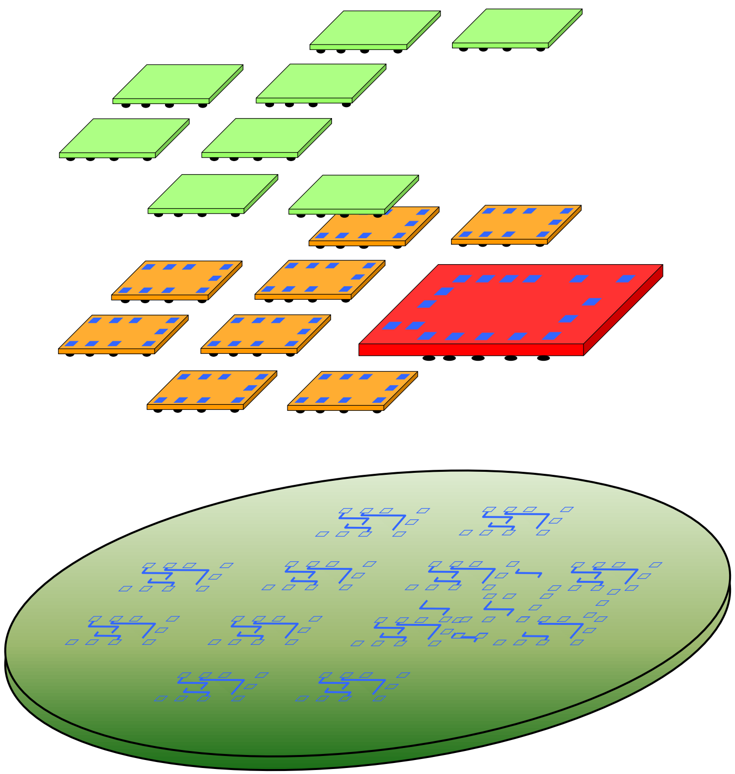
- ☹ Chip and wafer size must be identical
- ☹ Yield Issues
- ☹ Overlay very challenging

Failed Stacks

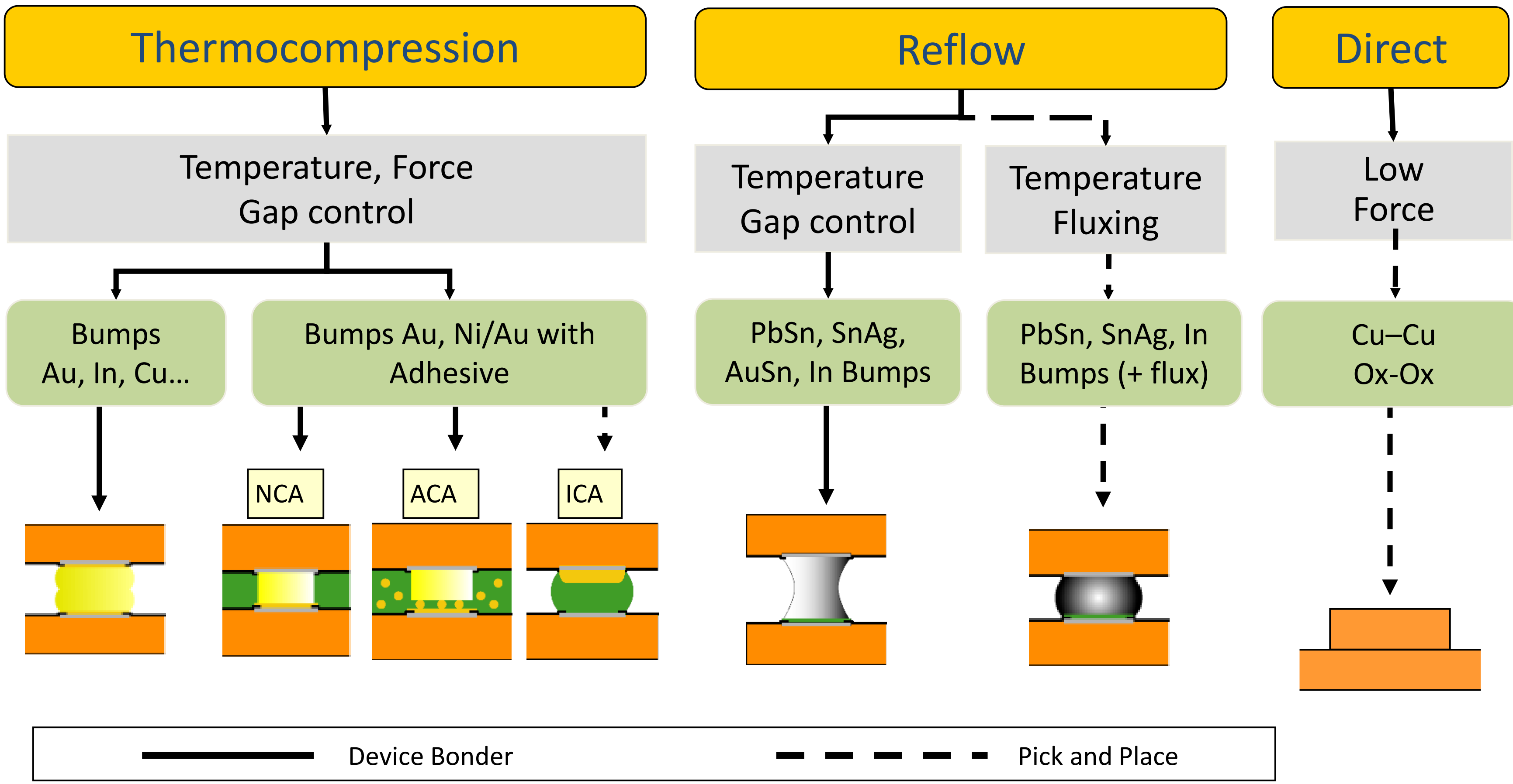
DIE TO WAFER (D2W) BONDING

Dice are bonded Face-to-Face (F2F) or Face-to-Back (F2B)

- ☹ Lower Throughput
  - \- Single Chip Placement
- ☺ High Yield
  - \- Known Good Die
  - \- Good Overlay
- ☺ Flexibility
  - \- Component and wafer sizes
- ☺ **Heterogeneity !**
  - \- Different Technologies
  - \- Different suppliers, …



DIE-TO-WAFER BONDING
IN-SITU BONDING PROCESSES



DIE-TO-WAFER BONDING
IN-SITU BONDING PROCESSES

Reflow Soldering

- T > Solder Melting Point
- CTE Mismatch makes Alignment more and more difficult as Pitch decreases and chip size increases
- Oxide protection or removal is required
- Die Warp and Smaller Bumps make Self Alignment reflow impossible

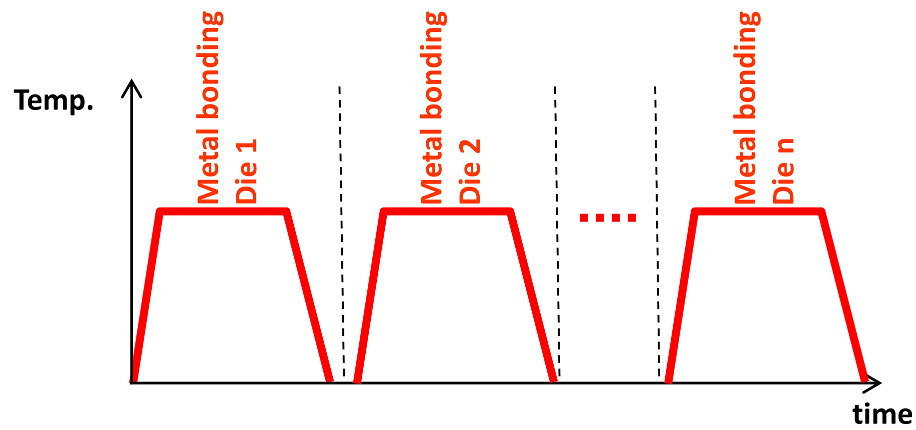
Thermo Compression Bonding

- T < Solder Melting Point
- Force increases with the number of interconnections

DIE-TO-WAFER BONDING
IN-SITU Vs COLLECTIVE, TEMPERATURE PROFILE

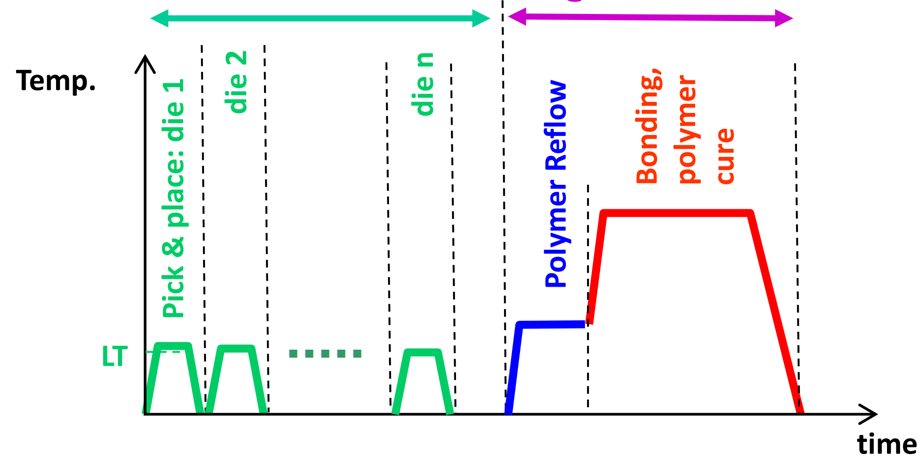
Sequential D2W bonding

- ☺ High Accuracy capability, controlled by the bonder
- ☹ Time consuming
- ☹ Landing wafer sees several bonding T-cycles



Collective D2W bonding

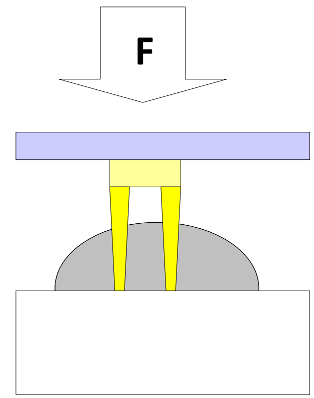
- ☺ Time efficiency
- ☺ Landing wafer sees only one temperature cycle
- ☹ Accuracy depends upon pre-attachment method and global bonder



Micro/Nano-Electronics Packaging and Assembly, Design and Manufacturing Forum
Conference & "interconex" Exhibition
MiNaPAD Forum 2011
MINATEC
3, Parvis Louis Neel
Grenoble, France
May 11-12, 2011

2-STEP APPROACH D2W BONDIN
THERMOCOMPRESSION – MICRO INSERTS

- Flip Chip Technique
  Using micro-tubes and solder pads
- Ultrafine Pitch < 10 µm
- High Bumps Count (2000 x 2000)
- Adapted to heterogeneous imaging arrays fabrication

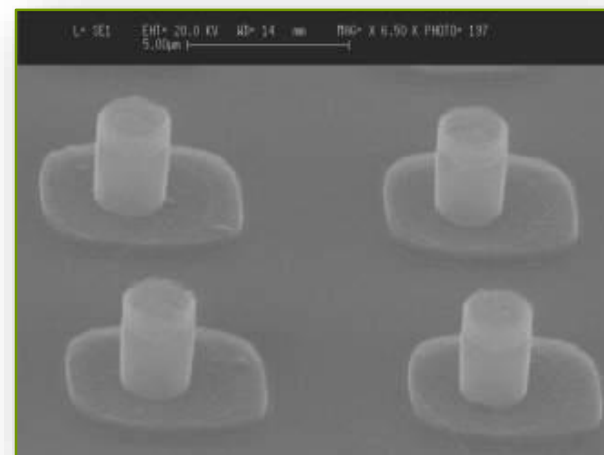


SET paper
DP 2009

Demonstrator IR-FPA (Indium Bumps)

- **4-million µtubes Array @ 10µm pitch**
- **Aligned on 6 x 6 µm² metallic pads**
- **Micro-tubes height: 2.5 ~ 2.8 µm**

→ Die-to-Wafer Parallelism is critical to successful insertion and bonding yield



2-STEP APPROACH D2W BONDING THERMOCOMPRESSION – MICRO INSERTS

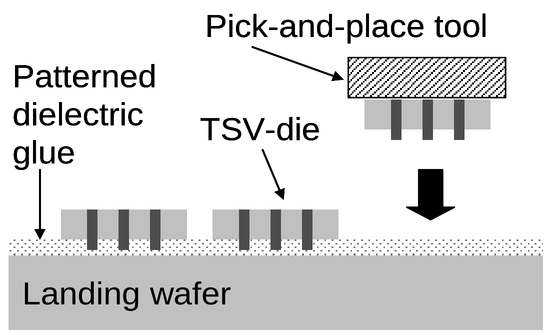
- Flux Less
  - Gold plated µtubes break the native solder oxide establishing electrical contact
  - No flux cleaning is required
- Low Pressure
  - Sharp µtubes geometry and indium solder ductility, enable insertion at low force (< 0.5 mN / connection)
  - Can be handled by conventional FC Bonding equipment even for high very pin counts (i.e. > **4 millions** connections)
- Room Temperature
  - No CTE mismatch issues
  - Bonding step can be completed by solid-solid diffusion

2-STEP APPROACH D2W BONDING
PHOTO PATTERNED DIELECTRIC GLUE

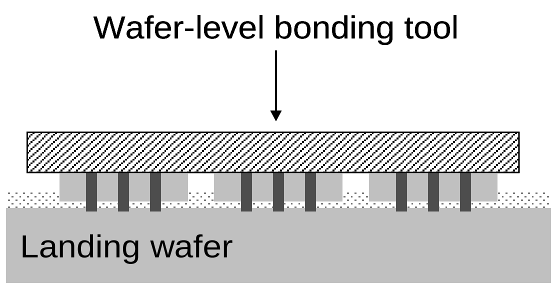
- **Cost effective processing by segmentation of 3D assembly**

SET paper DP 2010

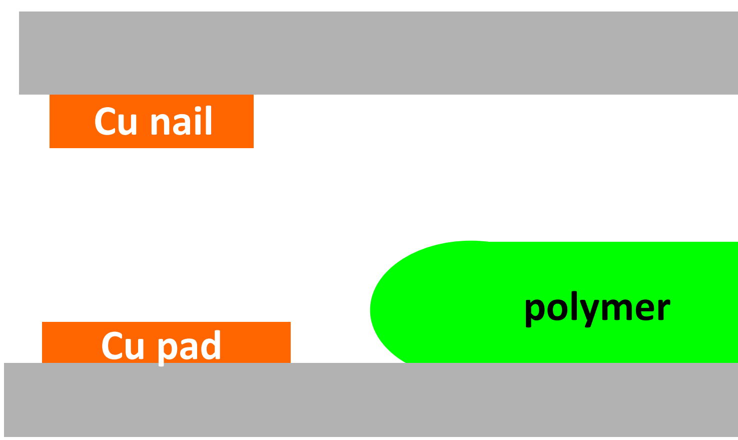
Die Pick and place



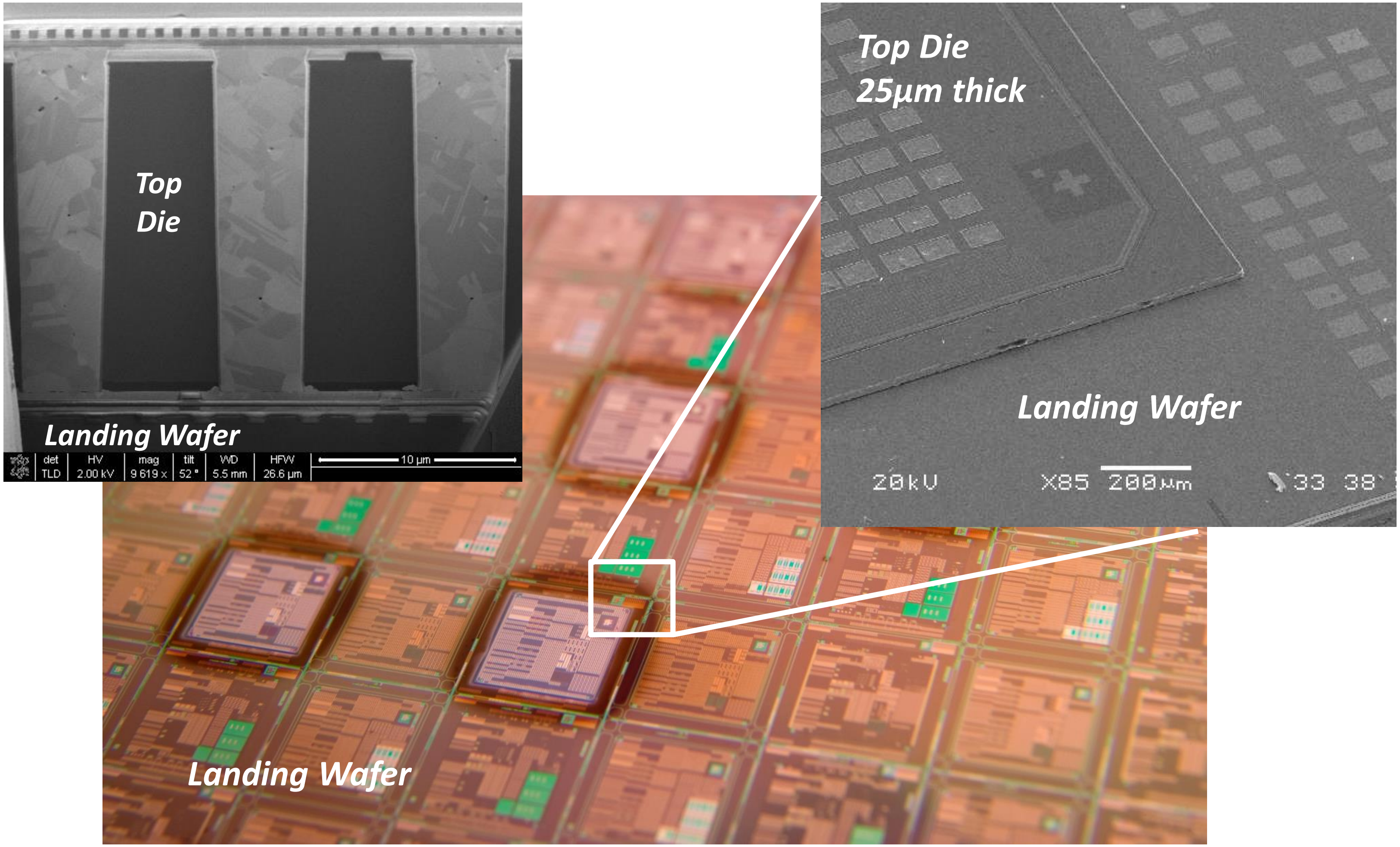
Collective bonding



- **Die placement (SET-FC300)**
  - Die is picked, aligned and Placed
  - It is secured by the Patterned Polymer
- **Collective Bonding (Wafer Bonder)**
  - Force and temperature are increased
  - The Polymer is reflowed
  - Critical step: die shifting might occur

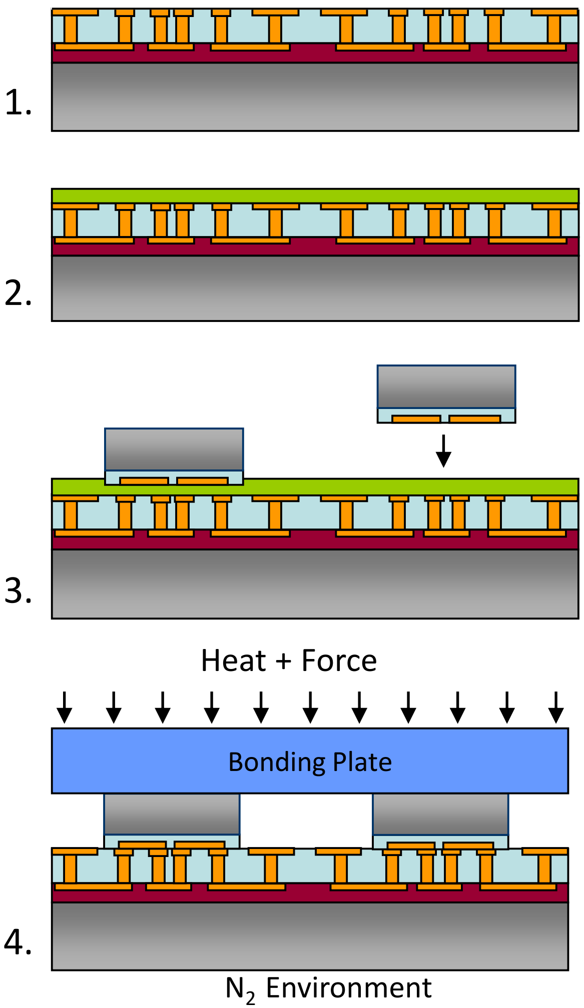


2-STEP APPROACH D2W BONDING
PHOTO PATTERNED DIELECTRIC GLUE

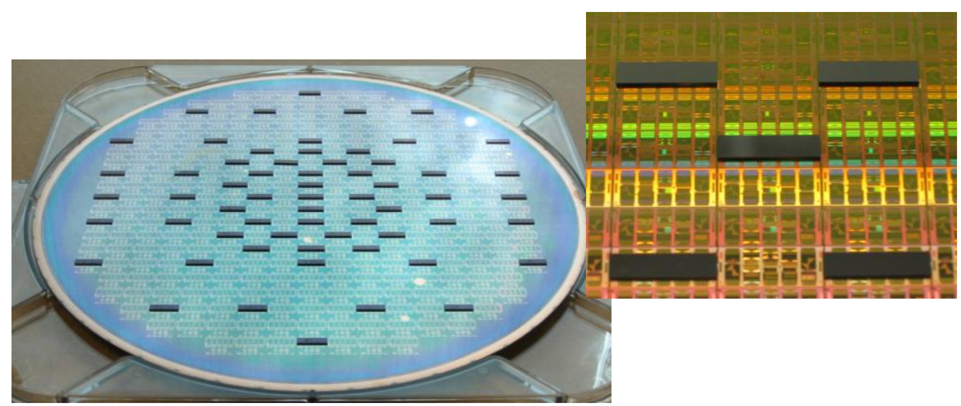


2-STEP APPROACH D2W BONDING THERMO DECOMPOSABLE ADHESIVE

SEMATECH



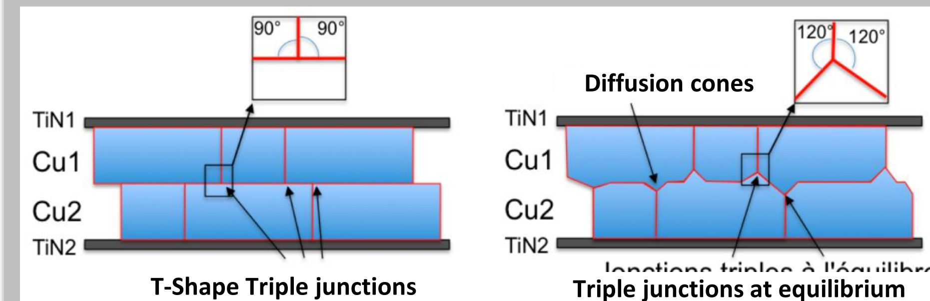
1. TSV wafer with bond and probe pads.
2. Spin coat thin layer of sacrificial adhesive.
3. Die Bonder →Tack dice sequentially
4. Wafer Bonder → Apply heat/force to decompose the adhesive and bond all dice in parallel.



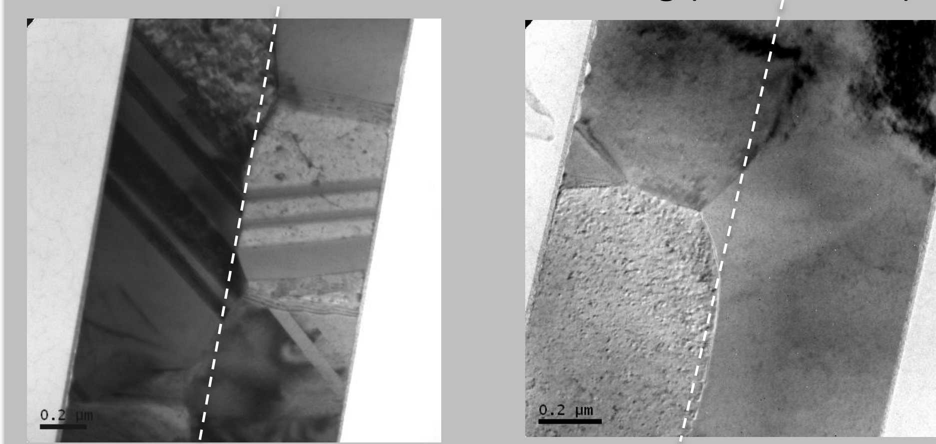
2-STEP APPROACH D2W BONDING
DIRECT METALLIC BOND

- Advantages
  - Low force and room temperature attachment process
  - High strength attachment at placement, no risk of shifting at collective bond step
- Challenges
  - Ultra clean equipment (SET-FC300, special design)
  - High planarity and clean surfaces with low roughness

Evolution with annealing



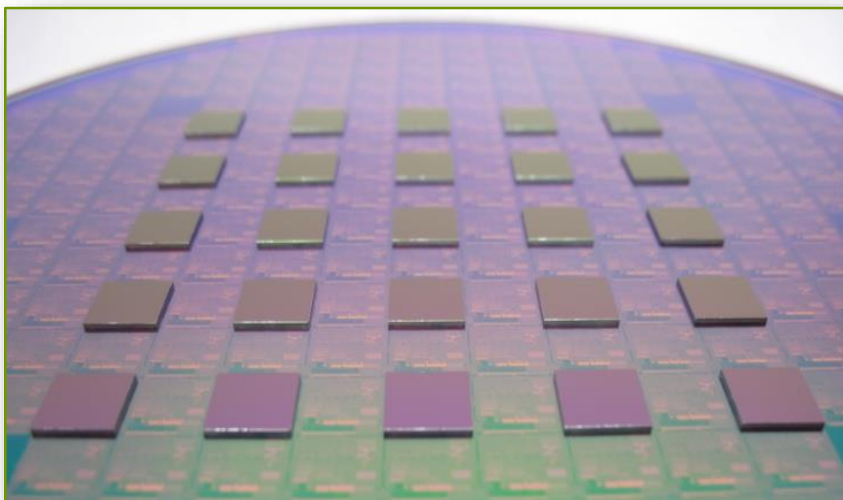
Direct Metallic Bond after annealing (2h @ 400°C)



2-STEP APPROACH D2W BONDING
USING PICK & PLACE USING DIRECT METALLIC BOND

- Multi-partner project partially financed by the French Ministry of the Industry to develop equipment and process for direct metallic bonding

  (FUI, FEDER, Region Rhone Alpes and Aquitaine)



COPPER PADS / PILLARS
REMOVAL OF OXIDE PRIOR TO BONDING

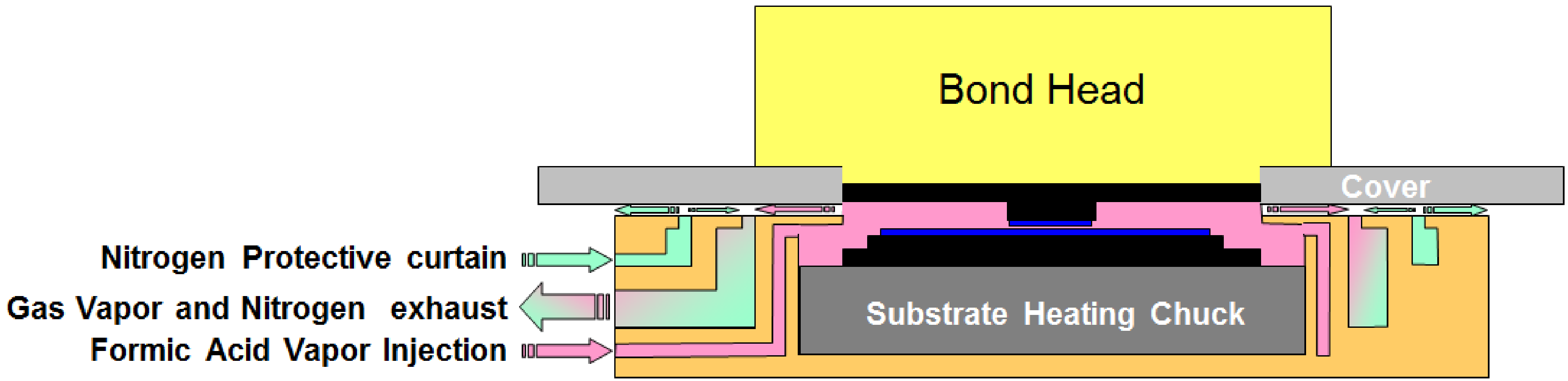
Problem with Copper → OXIDATION

- Cu oxidizes at STP, oxidizes rapidly at elevated temperatures
- Metal oxides inhibit mechanical and electrical integrity
- Oxides must be prevented, removed, or circumvented

Requirements for Oxide Removal Process

- Rapid and effective
- Inert to surrounding materials
- Minimal or no residue
- EHS Compliant
- Long-lasting
- Low-cost

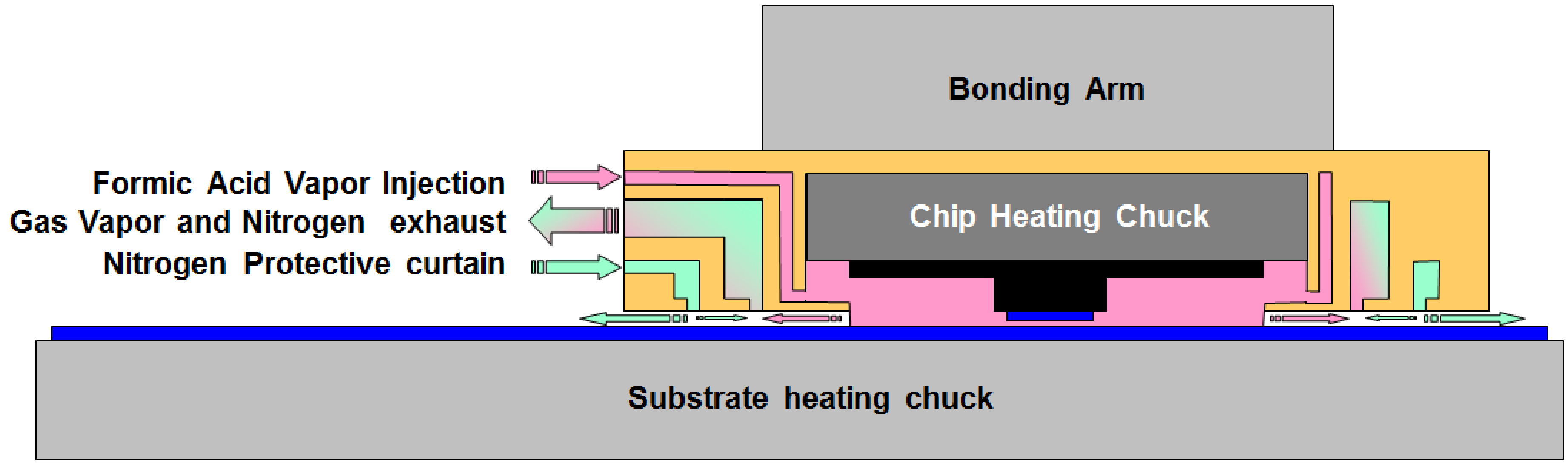
REMOVAL OF OXIDE PRIOR TO BONDING IN-SITU CONFINEMENT CHAMBER (D2D VERSION)



- Initially design for Die-To-Die bonding
- The Semi-Open Confinement includes two parts
  - The Chamber itself and a Contactless Cover Plate attached to the Bond Head
  - Formic Acid Vapor is injected towards the components

    Gap between components is programmable
  - The Exhaust Ring prevents process gas dissemination in the environment
  - External Nitrogen curtain prevents Oxygen introduction in the Confinement Chamber

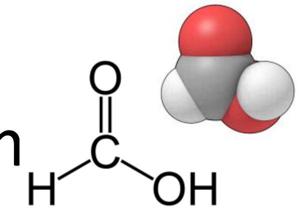
REMOVAL OF OXIDE PRIOR TO BONDING
IN-SITU CONFINEMENT CHAMBER (D2W VERSION)

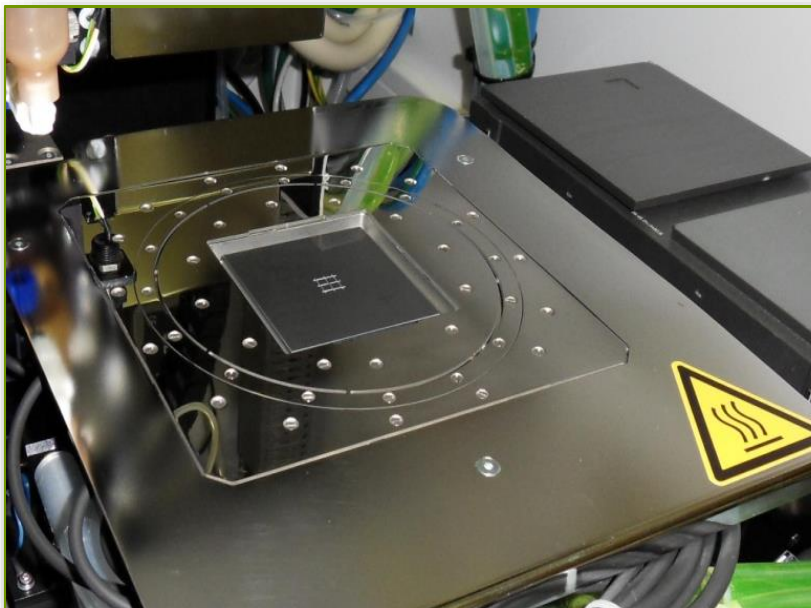


- **In the Die-to-Wafer version of the Confinement Chamber, the chamber part is attached to the bond head, the contact less cover function is performed by the wafer itself**
- **This experimental set up has some challenges**
  - Local areas of the wafer see several gas reduction cycles
  - During wafer population, exposed areas oxidize

REMOVAL OF OXIDE PRIOR TO BONDING
REDUCTION CHAMBER HARDWARE

- Photos of the D2D version of the micro-cham





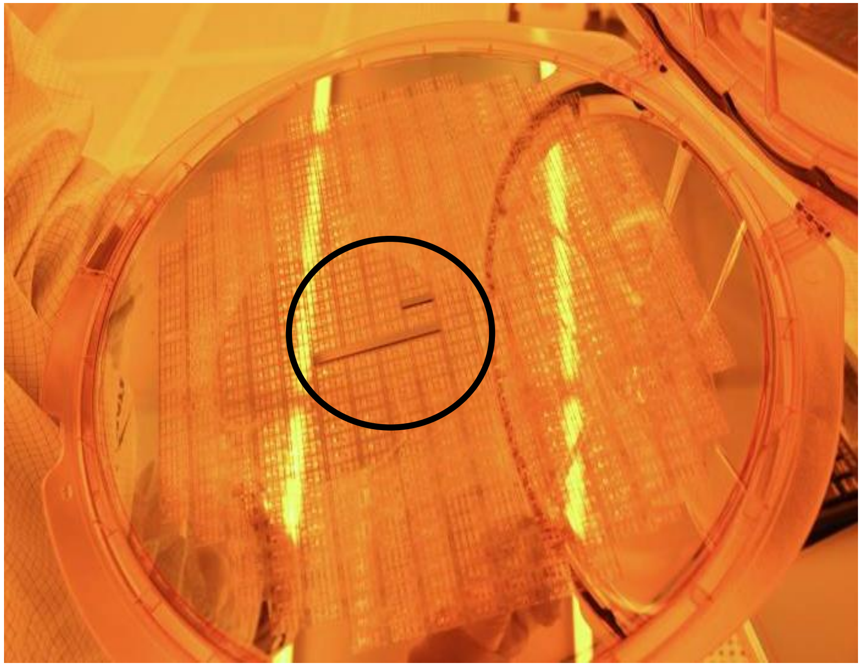
View of Chuck

View of Bond Head

REMOVAL OF OXIDE PRIOR TO BONDING EXPERIMENTAL RESULTS

SEMATECH

- Cu-Cu Bonding Procedure
  - Alignment at process temperature
  - Nitrogen purge and Formic Acid Vapor scrub
  - Bonding
    - Temperature of Bond Head and Chuck: 325 °C/ 300 °C
    - F = 1000 N
    - t = 900 s



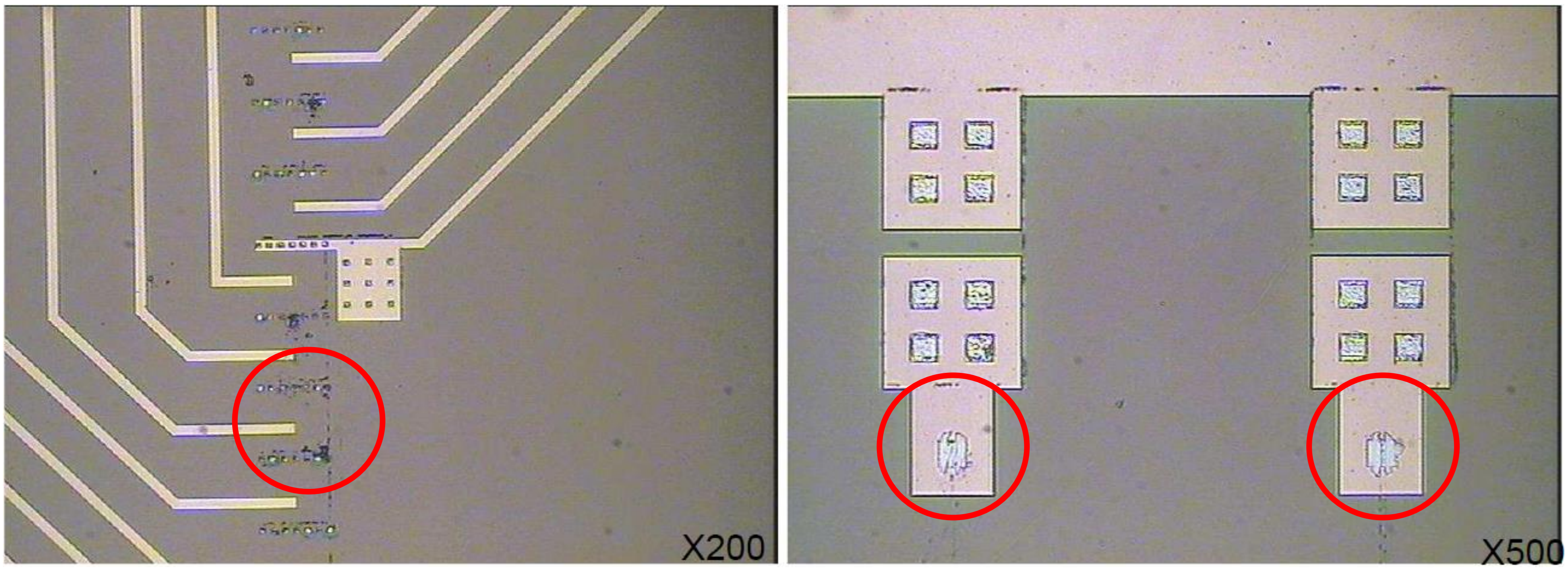
- **Five MM2 die were successfully bonded to an M1V1 wafer**

REMOVAL OF OXIDE PRIOR TO BONDING EXPERIMENTAL RESULTS

SEMATECH

- Evidence of copper transfer between MM2 and M1V structures

  Note: oxidation not seen on M1 lines and pads because the M1 structures are protected by a TEOS layer



SUMMARY

- High density 3D integration is moving to production
- D2W bonding with a 2-Step Hybrid Approach is a cost effective, high yield and flexible solution for 3D-IC assembly
- A variety of bonding technologies exist to enable HVM implementation of 3D schemes using D2D or D2W approaches