Chip-to-Wafer Technologies for High Density 3D Integration

T. Signamarcheix[a], L. Bally[a], S. Verrun[a], R. Taibi[b], G. Lecarpentier[c], A. Farcy[b], B. Descouts[b], M. Legros[d], M. Martinez[d], V. Lelievre[e], L. Di Cioccio[a] and C. Deguet[a],

[a]CEA-Leti, MINATEC Campus, 17 rue des Martyrs 38054 Grenoble, Cedex 9, FRANCE
[b]STMicroelectronics, 850 Rue Jean Monnet, 38926 Crolles, France
[c]SET, 131 impasse Barteudet, 74490, Saint Jeoire, France
[d]CEMES-CNRS, 29 rue Jeanne Marvig, 31055 Toulouse Cedex 4, France
[e]ALES, 8 rue des méridiens, Sud galaxie, 38433 Echirolles, France

Chip-to-Wafer (CtW) technologies are a promising solution for high density 3D integration application to overcome the limitation of Wafer-to-Wafer in terms of stacking yield, alignment accuracy and reproducibility along the wafers. Direct Cu bonding was developed at Leti to enable in situ Chip/Wafer electrical interconnection at low temperature, low pressure and with high bonding throughput [1]. The direct bonding presents the interest to avoid pre or post underfill even for a high interconnection density. We present here the recent advance in Chip-to-Wafer structures made by combination of direct Cu bonding and high alignment accuracy pick&place process.

For direct bonding technologies, extremely low surface contamination is required to ensure the perfect quality of the bonding interfaces. For this purpose, specific developments were realized on an SET-FC300 [2] pick&place equipment to achieve a low particular contamination during the processes. A local microenvironment was created into the equipment to protect the wafer surface during the chip's bonding. Such an optimization allows to significantly decreasing the contamination as it will be presented (Fig.1). As an example, the particle contamination after substrate processing was reduced from 350 particles without optimization to less than 20 particles with the optimization (estimated by automatic surface inspection on the wafer).

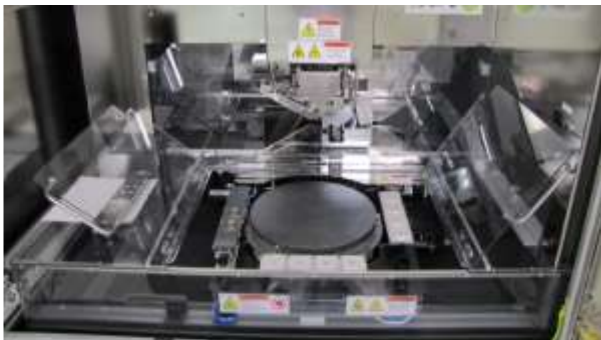

Fig.1: *Illustration of the microenvironment realized by the SET company on a FC300 equipment to limit the particular contamination on the wafer during the chip-to-wafer bonding.*

One Cu level stacks were prepared to define patterned Cu/SiO_2 surfaces for both the chips and the wafer. Optimized damascene like process was employed to obtain a smooth surface and to adapt the topology between the SiO_2 and Cu areas [3]. Surfaces were then subjected to a combination of treatments to enhance the surface hydrophilie. Fig.2 is a Scanning Acoustic Microscopy (SAM) observation of the structure obtained for a non aligned CtW bonding and after a 400°C thermal annealing (2hrs). It demonstrates the excellent bonding quality of the CtW interfaces.

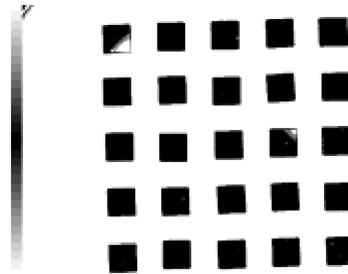

Fig.2: *SAM observation of the non-aligned CtW structure made by direct Cu/SiO_2 bonding after a 400°C annealing (2hrs). Dark areas represent bonded areas.*

Aligned CtW bonding was also ensured in the optimized pick&place equipment. Characterization of the structures by mean of Scanning Acoustic Microscopy (SAM), InfraRed (IR) misalignment alignment, Scanning Electron Microscopy (SEM) and electrical test will be presented and discussed as a validation of both, the direct bonding technology as well as the equipment optimization and capability.

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References

[1] P.Gueguen et al, IITC 2008, proc. p 61 (2008)
[2] http://www.set-sas.fr/en/mpg1-175538--FC300-High-Force-Die---Flip-Chip-Bonder.html
[3] P.Gueguen et al. Conference Information: 18th European Workshop on Materials for Advanced Metallization, MAR 08-11, 2009 Grenoble, FRANCE