3D-IC Integration using C2C or C2W Alignment Schemes together with Local Oxide Reduction

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Abstract:

3-Dimensional interconnection of high density integrated circuits enables building devices with greater functionality with higher performances in a smaller space. This paper explores the chip-to-chip and chip-to-wafer alignment and the associated bonding techniques such as in-situ reflow or thermocompression with a local oxide reduction which contributes to higher yield together with reduction of the force or temperature requirements.

Extended Abstract:

To realize 3-Dimensional Integration (3DI) for practical applications, a number of technical challenges must be addressed. This paper will highlight two major challenges in the bonding realm, namely the issue of bonding methodology and the issue of removing surface oxides before bonding. These two will be explored to define the problem as well as their technical and economic impact on the device performance and manufacturing process.

In a typical 3DI process flow, Through-Silicon-Vias (TSV's) are created in the wafer, creating a connection path which is completed when one substrate is bonded to the other. The advantages of this general scheme have been widely reported and include reduced device footprint, higher performance and speed, as well as reduced cost. Furthermore, 3DI provides the distinctive of combining devices of different design rules, application types, or even substrate materials into one package, in a word, heterogeneous integration.

Choice of Bonding Methodology

Bonding of chips and wafers has been employed in many segments of the semiconductor world, typically used in higher-end devices. The methodologies can be roughly divided into 3 general types: Wafer-to-Wafer (W2W), Chip-to-Chip (C2C) or Chip-to-Wafer (C2W). The first of these, W2W bonding, involves the joining of two entire wafers before any singulation has taken place. Developed initially for MEMS applications, this method has found wide usage in the MEMS packaging world such as the encapsulation of accelerometers and various sensor types. Though this method is considered for 3DI, it is limited to bonding substrates with same wafer diameter and same chip dimensions, though it can bond many chips quickly in a parallel process. For this reason and others, W2W will likely play a role primarily in the realm of bonding 3DI wafers to carriers for thin wafer handling.

The second bonding methodology, C2C, has been used widely for high performance devices such as optical imaging devices, stacked memories and other MEMS or photonic devices. A wide variety of joining materials and processes is available for these

applications, as shown in Figure 1. C2C bonding offers the advantage of high accuracy, flexibility and performance, but carries with it limited throughput, since each die must be typically leveled and aligned to its mate before the bonding process begins. Some devices may not require such stringent alignment tolerances, but high performance devices in the 3DI realm typically do. C2C also offers the advantage of bonding only known-good-die (KGD), thus increasing the potential yield dramatically. Furthermore, this method can bond devices of highly disparate application type, chip size or even substrate material to achieve true heterogeneous integration. Various applications and reasons for employing C2C bonding will be reviewed in the presentation.

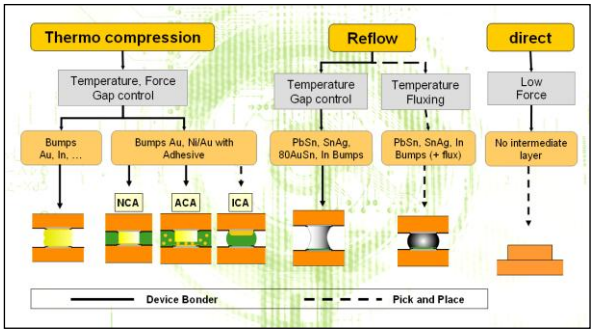

Fig. 1: Flip Chip processes

Chip joining processes are often grouped into 3 types as shown here. For thermocompression bonding, a relatively high force up to many kg's can be applied in conjunction with elevated temperature to create the joint. Reflow processes employ materials such as solders which melt and re-freeze. Direct bonding incorporates very smooth and flat surfaces to bond directly to each other without any intermediate layers.

A novel method of joining chips, insertion of micro-tubes with solder lands, has recently been developed specifically to address the need for high-density interconnects with small bumps. This process is depicted in Figure 2 and will be reviewed.

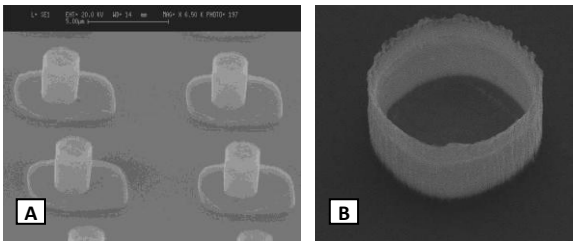

Fig.2: µtubes fabrication results - Top Views

C2W bonding employs the bonding of singulated chips onto un-singulated wafers. Similar to C2C bonding, it uses only KGD, can bond chips of many different types, thicknesses and sources, and has great flexibility in its choice of joining process. Unlike C2C bonding, it is used to bond chips to near or far neighbors on the wafer surface, creating a system with very high functionality within a very small space.

A hybrid method is proposed and explored, whereby the advantages of C2W and W2W bonding are provided. Dubbed "collective hybrid bonding", this approach uses a rapid and straightforward joining method in a C2W bonding flow, followed by a longer bond in W2W fashion to permanently attach all chips to their host wafer. As depicted in Figure 3 and as will be detailed in the presentation, this method preserves the flexibility and accuracy of C2C or C2W bonding, at greater throughput and therefore lower cost. Examples and details of process flows and materials from various groups will be highlighted.

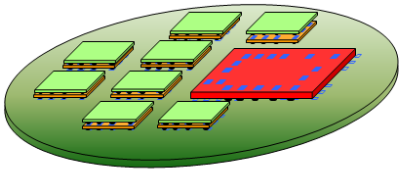

Figure 3: C2W bonding of various sizes

Reduction of Oxides

Since many 3DI process and bonding methods include metals such as copper as the joining material, the challenge of surface oxidation must also be addressed. Oxides can form on the outer surface of these metals, either due to elevated process temperatures or even as native oxides at ambient conditions. These metal oxides may hinder the joining process, expressing themselves as either insulating surfaces which inhibit the electrical performance, or as mechanical barriers which inhibit the bonding strength.

A new method of removing oxides is proposed and explored, wherein a confinement chamber is formed around the bonding region, then a reducing gas is introduced into this area just prior to the actual joining process. The confinement chamber is created by using a near-contact virtual seal between the bonding head (holding the chip) and the substrate chuck; this set-up ensures integrity and concentration of the gas while preventing oxygen intrusion. The hardware is shown schematically in Figure 4 and enables the rapid and safe removal of oxides under a controlled atmosphere immediately prior to bonding. Configurations for both C2C or C2W bonding have been delivered; C2W confinement chamber is depicted here. Since there is no physical contact between bonding head and substrate chuck, key requirements of bonding such as alignment quality and force control are unaffected by the chamber.

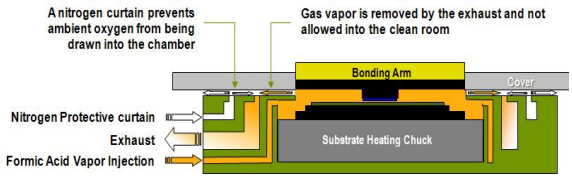

Figure 4. Schematic of local confinement chamber.

As noted in Figure 4, the process gas is injected through horizontal nozzles towards the device being bonded; an exhaust ring removes the process gas from the confined area and sends it into the gas exhaust line, preserving the integrity of the machine and the cleanroom environment. A nitrogen curtain is formed around the exhaust, ensuring that ambient air is not entrained into the micro-chamber by the Venturi effect, while a cover attached to the bond head creates the confined micro-chamber. This configuration operates with either inert gasses to prevent oxide formation on bonding surfaces during the bonding sequence, or with reducing gasses such as forming gas or formic acid vapor to remove and prevent oxides. Photos of local confinement chamber hardware are shown in Figure 5.

(a) (b)

Figure 5. Photos of the C2C confinement hardware with a view downward at the bonding chuck (a) or upward at the bonding head (b)

To qualitatively gauge the confinement chamber's performance, a copper coupon with test patterns was heated to 350C for 30 seconds in the bonding position while formic acid vapor flowed into the chamber at 8 SLPM; all oxides were presumably removed and the copper surface was accordingly highly reflective. Next, formic acid vapor flow was terminated, and the copper surfaces oxidized rapidly at 350C with ambient air, producing a mottled and unreflective surface in a few seconds. Following this, the formic acid vapor was reinstated and the copper quickly returned to its reflective state, indicating that oxide

removal was effective and rapid. Quantitative tests with electrical and/or bonding data are ongoing and are very positive, showing effective removal of oxides at 250-350C. Figure 6 indicates the testing of the copper coupon as described.

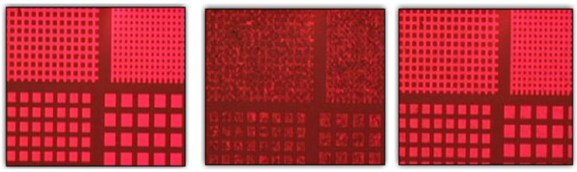

Figure 6. Copper patterns on test chip (a) after 30 seconds of formic acid vapor, (b) after a few seconds of atmospheric ambient, and (c) after formic acid flow is reinstated, showing the rapid reduction of the oxides.

Conclusions:

Two key challenges of 3DI have been explored and solutions detailed, namely in the area of collective hybrid bonding to optimize bonding accuracy and throughput, and in the area of reducing metal oxides prior to bonding by means of a confinement chamber. The two have been implemented on a commercially available device bonder to help to enable true heterogeneous integration for commercial applications.