PROCESS AND EQUIPMENT ENHANCEMENTS FOR C2W BONDING IN A 3D INTEGRATION SCHEME

Keith A. Cooper, Michael D. Stead
SET North America
Chester, NH, USA
kcooper@set-na.com

Daniel Pascual
CNSE Assignee to Sematech
Albany, NY, USA

Eric F. Schulte
Process Consultant
Santa Barbara, CA, USA

Gilbert Lecarpentier, Jean-Stephane Mottet
SET SAS
St. Jeoire, France

ABSTRACT

Of the various methodologies under consideration for 3D integration, chip-to-wafer (C2W) bonding is a leading candidate due to its inherent flexibility and potentially high yields, all leading to a highly integrated, multifunctional, cost-effective device with a small footprint. C2W bonding can enable true heterogeneous integration by using dice from differing substrate materials, manufacturers, die sizes or even wafer diameters while maintaining high yields due to selecting only known-good dice (KGD).

Due to the feature sizes and therefore the alignment and registration tolerances for advanced devices, each die is sequentially selected, leveled, aligned and then bonded to a host wafer. Though the results are high quality, the process can be time consuming due to the materials and bonding processes typically used for vertically integrating these chips. Furthermore, the Cu bonding surfaces often used are prone to oxidation at elevated bonding temperatures or even at room temperature, and particulates on the surfaces or in the local environment can limit the accuracy and electrical integrity of the bonds.

This paper will review 3 major areas of process or equipment development surrounding the above problems, namely the issue of in-situ or prior removal and prevention of surface oxides at the bonding interface, the issue of local environmental control to reduce particulates and other airborne contaminants, and the issue of throughput enhancement by using a sacrificial adhesive to temporarily tack the dice before collective bonding. Each of these 3 will be explored with hardware solutions proposed, along with process results on test vehicles or functional devices.

INTRODUCTION

Since the advent of semiconductors and integrated circuitry, manufacturers have raced to produce the next chip which would be faster, cheaper, better. [1] A recent effort has focused on packaging present or future chip generations more densely by using the third dimension – height - in chip packaging and integration. Referred to as 3D Packaging and 3D Integration, the effort focuses on the need to conserve footprint in the semiconductor material and in the final package by building the circuit or the package upward instead of outward.

In a typical 3DI process flow, Through-Silicon-Vias (TSV's) are created in the wafer, creating a connection path which is completed when one substrate is bonded to the other. The advantages of this general scheme have been widely reported and include reduced device footprint, higher performance and speed, as well as reduced cost. [2-7] Furthermore, 3DI provides the distinction of combining devices of different design rules, application types, or even substrate materials into one package, in a word, heterogeneous integration. A schematic showing the potential buildup of many disparate chips into one compact unit is depicted in Figure 1. Despite the obvious attractions of 3D integrated circuits, they must be manufactured within market-defined cost constraints. [8].
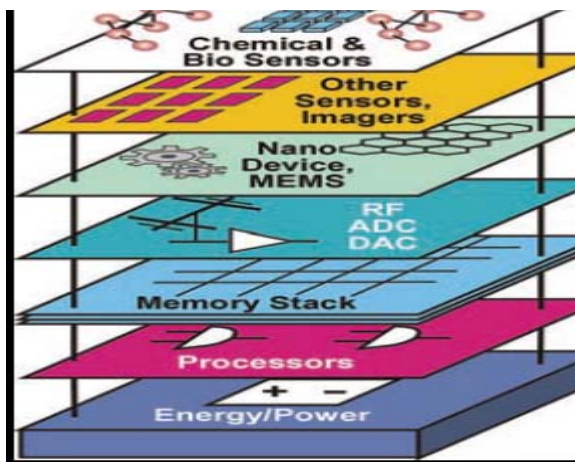
Figure 1. 3D Integration for heterogeneous systems [9]

Among the challenges which 3DI must address to enable widespread adoption are the costs associated with the throughput and yields of such a complex scheme. This paper will address 3 areas of key concern, including yield enhancement by in-situ or prior removal of surface oxides at the bond interface, yield enhancement by local particulate control and hardware optimization, and throughput enhancement by collective bonding with a sacrificial adhesive.

IN-SITU OXIDE REMOVAL
In a typical process flow for 3D Integration, TSV's are etched into the substrate, then filled with various conductive or dielectric materials. Cu has become a major focus as an interconnect material for 3D integration due to its relative ease of processing, mechanical and electrical characteristics, and its scalability [4-7]. A representative TSV structure for 3D chip stacking is shown in Figure 2.
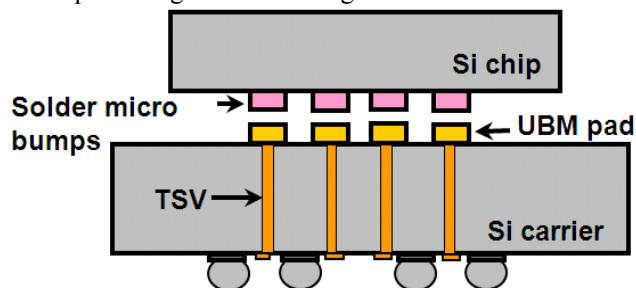
Figure 2. Schematic drawing of 3D stacking of the Si chip/Si carrier with TSV (not to scale). Image courtesy of A. Yu of IME Singapore.

The surfaces of the Cu or other bonding materials likely have oxides present which compromise the thermocompression bonding results. Oxidation of metal surfaces is a persistent problem in device bonding. Because oxides generally adhere poorly to other metals or oxides, the bonding force must penetrate the oxide, literally breaking through to achieve metal-to-metal cohesion. Not only does this increase the required bonding force, but the oxides may also raise the electrical resistance of the joint. Even after the device has been bonded, residual oxides may provide a

convenient site for further oxidation, leading to reliability and performance problems [6]. The requirements for an oxide removal process have been previously outlined [10] and include:

- Fast, effective removal of oxides
- Inert to other surfaces
- Minimal or non-existent residue
- EHS compliant
- Sufficient duration of effect
- Cost-effective

Historical methods for removing oxides have included mechanical scrubbing during the bonding process, using an acid dip prior to bonding, or using oxide-reducing flux. Though these methods have worked for larger feature sizes, they can create misalignments, add processing steps, or in the case of flux, can lead to reliability or performance problems if flux residues are not completely removed.

A new method to remove oxides has been developed, wherein a local confinement chamber is formed by the bonding tool at the bond interface which uses reducing gasses such as forming gas or formic acid vapor to safely reduce the oxides immediately prior to and during bonding. The confinement chamber has been described previously [10] and is depicted in Figure 3.
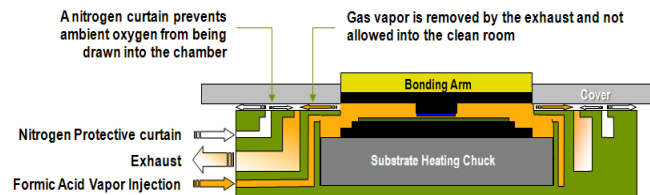
Figure 3. Schematic of local confinement chamber.

As noted in Figure 3, the process gas is injected through horizontal nozzles towards the device being bonded; an exhaust ring removes the process gas from the micro-chamber and sends it into the gas exhaust line, keeping the gas out of the machine and the clean room. A nitrogen curtain is formed around the exhaust, ensuring that ambient air is not entrained into the micro-chamber by the Venturi effect, while a cover attached to the bond head creates the confined micro-chamber. This configuration operates with either inert gasses to prevent oxide formation on bonding surfaces during the bonding sequence, or with reducing gasses such as forming gas to remove and prevent oxides. Photos of local confinement chamber hardware are shown in Figure 4.
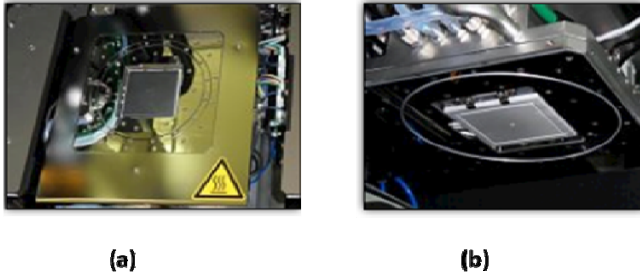
Figure 4. Photos of the confinement hardware looking down at the bonding chuck (a) or up at the bonding head (b)

The chamber's effectiveness has been examined and proven both with mechanical samples and with test devices. [10, 11, 13]. The use of this chamber in a C2W bonding scheme would involve the repeated reduction of oxides for the present bonding site and its neighboring sites, so the impact of repeated oxide removal and reflow steps on the bonding metallurgy would have to be properly explored and managed. [12].

EX-SITU REMOVAL OF OXIDES

To reduce sequential-bond cycle time, an ex-situ removal of oxides prior to bonding is also under development. To counter the undesirable effects of re-oxidation before or during bonding, the freshly de-oxidized surface is protected with a few monolayers of passivation which inhibits re-oxidation at elevated temperatures and/or extended periods of time. Since the passivation layer is only a few atomic layers thick, it is easily frangible upon bonding contact and therefore does not need to be removed prior to bonding. Additionally, the process is completely dry, contaminant-free, takes only a few seconds to perform, and is done in atmospheric ambient conditions with non-hazardous chemistry. These features enable a continuous flow of die into the bonding process and eliminate the need for the confinement chambers, exhausting any reducing gasses, and the process overhead to reduce oxides at each bonding site.

The process was originally developed for indium bump bonded infrared focal planes (IRFPAs), as indium oxide is particularly difficult to penetrate during thermo-compression bonding. Application of this method to IRFPAs and other indium bump bonded assemblies has led to a significant reduction in required bonding force (less bump deformation), reduced slip mis-registration, and a shortened compression cycle; while at the same time increasing pixel yield and thermal cycle reliability. The process has been proven to have no deleterious effect on sensitive CMOS circuitry or ultra-sensitive infrared detector material.

Analytical characterization of the process is carried out on small specular coupons of indium-on-silicon using laser ellipsometry. The measure of change in the polarization of the reflected laser beam (raw Delta value) is inversely related to the depth of thin surface films such as oxidation. Figure 5 shows a progression of ellipsometer delta (Δ) of an indium surface with respect to time before, during, and after surface treatment.
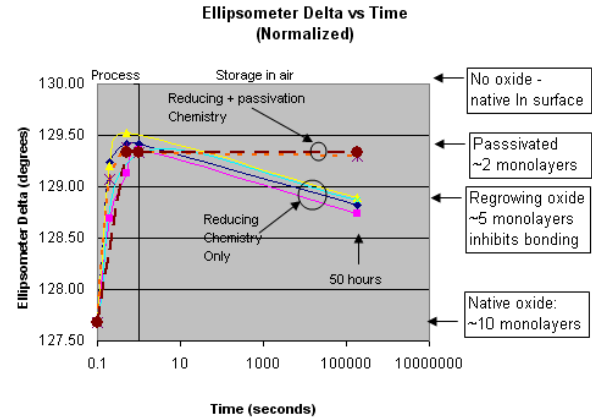
Figure 5. Ellipsometer delta reading shows de-oxidation of the indium surface followed by 50 hours soak in air. Note regrowth of oxide on unpassivated samples vs. stability of passivated samples.

A lower reading on the Δ axis indicates a thicker oxide. Native indium oxide lies at ~127.7, whereas a perfect non-oxidized surface would be at ~130.00. Treatment by the proprietary process raises Δ to around 129.4. Without passivation, the native oxide begins to re-grow immediately, and will eventually relax to native oxide saturation. However, with the passivation, Δ stays essentially unchanged after 50 hours of soak in atmosphere at room temperature. Since IRFPAs are typically bonded at room temperature, this passivation appears highly suitable for practical IRFPA production applications, and indeed, IRFPAs bonded 24 hours after treatment had the same adhesion and tensile rupture as freshly treated die. In order to test the limits of the passivation, indium/Si coupons were treated, measured, and then placed on a 150C hotplate in air for 5 minutes. The Δ dropped ~0.2 degrees, and remained there after an additional 5 and 10 minutes back on the hotplate. Bonding tests with bumped chips after hotplate soaks have not yet been attempted, but ellipsometer readings would predict success.

Figure 6 depicts the IRFPA indium bumps after room-temperature indium-to-indium bonding and subsequent pull-apart.
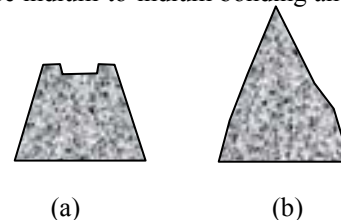
Figure 6. Comparison of indium-to-indium adhesion of IRFPA bumps after pull-apart: (a) without surface treatment; (b) with pre-bond surface treatment.

Portion (a) is from an untreated FPA and shows no indication of indium-to-indium adhesion, merely an indentation where the bumps compressed together but were

inhibited from fusing by native oxidation. Portion (b) is from a pre-bond treated FPA, bonded under identical conditions and shows ideal tensile rupture of the indium indicating that the opposing bumps were fused into a single column. IRFPAs bonded with this method were subsequently completed and tested, and showed comparable (actually slightly better) performance and pixel yield.

Other metal contact combinations are currently being tested and early ellipsometer results are encouraging. Bonding tests with these alternate contact metals are currently in progress.

PARTICULATE STUDY OF FC300

Since the bond methodology for 3DI often includes Cu and its alloys, flatness and cleanliness of bond surfaces is critical to achieving initial contact; without initial contact, the bond cannot propagate and the electrical resistance will be unacceptable.

In a study funded by French and European sources (PROCEED and FEDER, respectively) particle counts were conducted on an SET FC300 bonder configured for 3DI at the CEA LETI facility in Grenoble. Using settling wafers and the KLA Tencor SP2 surface particle counter with 90 nm detection threshold, the FC300 tool was systematically studied to identify prime sources of particulate matter [13].

Air flow within the alignment section of the bonder was found to be adding particles to the wafer on the alignment stage, as were several mechanical motions of either the alignment optics or the bonding head itself. After a detailed analysis of the particle counts and of the materials used in the respective machine assemblies, changes were identified and carried out on numerous portions of the motors, bearing surfaces and cabling channels. In some cases, subassemblies were equipped with containment chambers to either encapsulate or exhaust generated particles, as shown in Figures 7 and 8. Particulate counts in critical areas of the bonder were reduced about 2 orders of magnitude, as shown in Figure 9, leading to improved yields and therefore decreased costs at the bonding step.
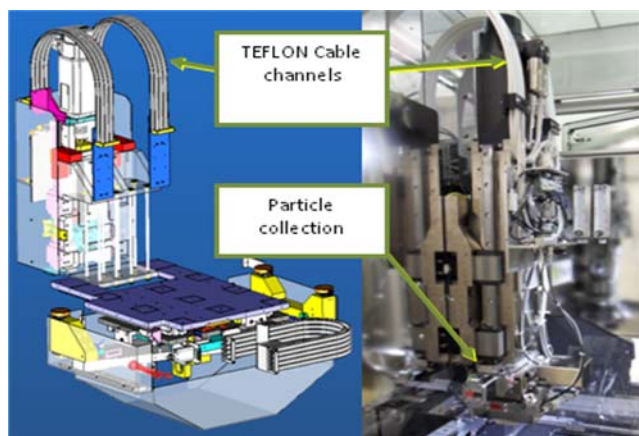
Figure 7. Bond Arm Improvements
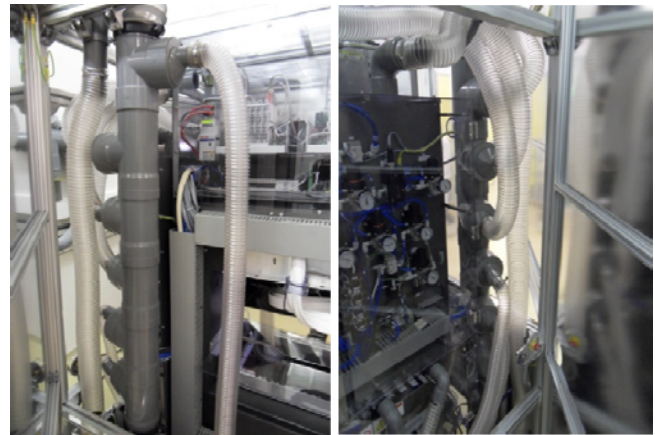
**Figure 8.** Various electrical and pneumatic components contained and exhausted.
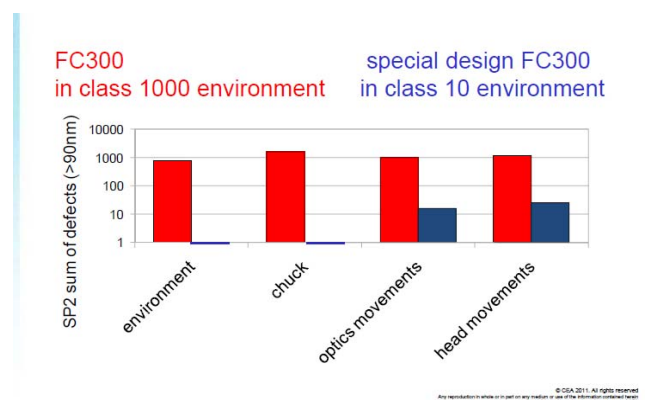
Figure 9. Improvements of particle counts after machine improvements described

THERMO-DECOMPOSABLE ADHESIVE

A new method has been explored in which singulated dice are initially bonded or tacked to a wafer in Chip-to-wafer (C2W) fashion, then the bonding process is completed in a wafer bonder tool. Intended to address the issues of CTE mismatch and bonding known-good-die (KGD) of various sizes and types, yet with the cost effectiveness and throughput of a wafer-to-wafer (W2W) scheme, this method has been referred to as collective hybrid bonding and been described and employed previously [9-11].

Using a high-accuracy die bonder, individual dice are aligned and tacked, one-at-a-time, onto a wafer coated with a thermo-decomposable adhesive layer. The low-temperature tacking process avoids oxidation of the Cu bonding surfaces, minimizes thermal cycling times, and increases throughput significantly. Once the wafer is populated, it is further processed in a closed-chamber wafer-bonding tool in an oxygen-free environment. All of the dice are gang-bonded using a high-temperature Cu-Cu bonding process to globally apply the required heat and force. Once the adhesive is heated past its critical decomposition temperature, it cleanly vaporizes away and the Cu-Cu bonds are formed. A process summary is depicted in Figure 10.
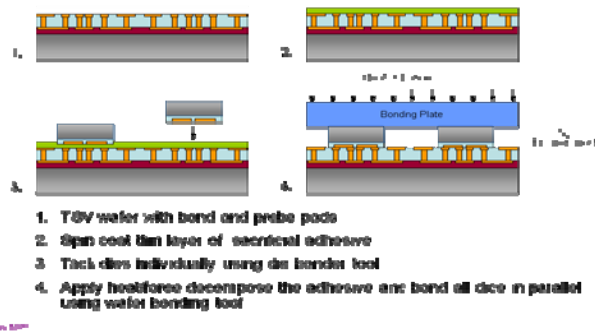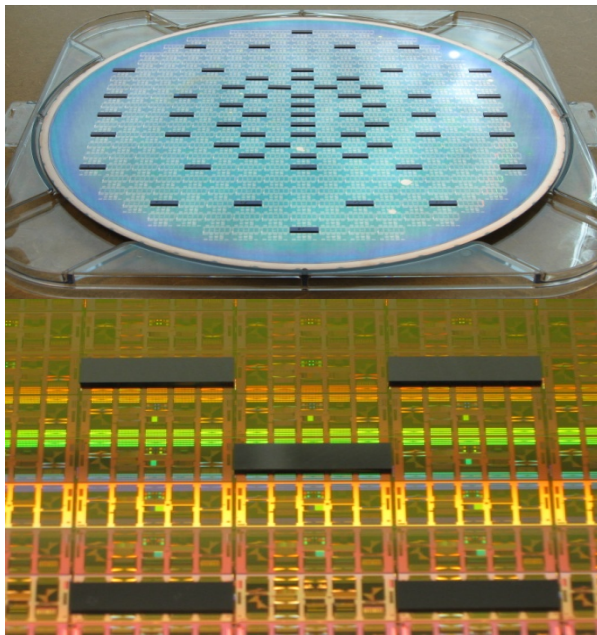
**Figure 10.** Tack/Collective bonding process overview. 1) 50um thick TSV wafer containing bonding and probing pads on its top surface and backside metallization for electrical chains. The TSV wafer is attached to a 300mm Si handle wafer (gray) using an adhesive (red layer). 2) A 0.8um thick layer of thermo-decomposable adhesive (green) is coated on top of TSV wafer. 3) Multiple dice are tacked onto the TSV wafer one-at-a -time using short, low-temperature cycles in a high-accuracy die bonder. 4) All dice are bonded simultaneously using a high-temperature bonding cycle in a closed-chamber wafer bonder. During collective bonding, the adhesive vaporizes away followed by diffusion bonding of the Cu bond pads.

Multiple dice were bonded to a 300mm TSV wafer platform using the tack/collective bonding process described above. Figure11 below shows photographs of the populated wafer and a close-up of several dice.

Figure 11. Above: Multiple dice bonded to 300mm TSV wafer using the tack/collective bonding process. Below: Close-up of bonded Dice.

Electrical chains are composed of 5um diameter TSVs, backside metallization, and the metal patterns of the bonded die. Each chain contains a total of 3,552 links with taps at every 296 links. The chain resistance is plotted against chain length in Figure 1212 below. Note that these measurements also include the resistance of the electrical leads, which contribute to the overall measured resistance. A Kelvin test structure was used to separate out lead resistance. The resulting four-point resistance of a single TSV and a bonded connection is 75mΩ. This value is consistent with separate measurements of just the TSV alone, which suggests that the resistance of the Cu-Cu bonding interface is negligible compared to the TSV resistance. Analysis by FIB-SEM confirmed that the thermo-decomposable adhesive does not interfere with Cu bonding [14].
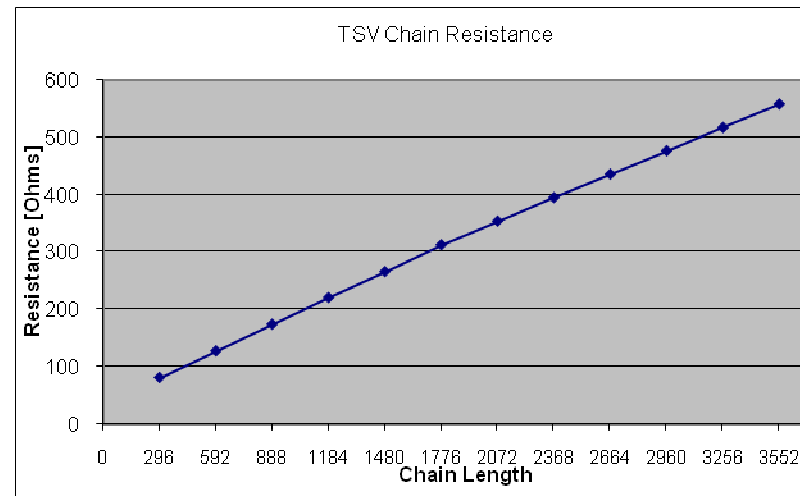
Figure 12. Resistance of TSV chains containing up to 3,552 links. Electrical chains are completed by each TSV, backside metallization, and the metal patterns of the bonded die.

CONCLUSIONS AND RECOMMENDATIONS
To address some of the cost concerns concerning 3D Integration, three specific areas of C2W bonding were explored with a view to increasing throughput, quality and yield. The first topic explored the use of in-situ or ex-situ hardware and processes to remove and/or prevent oxidation on metal bonding surfaces. Both methods proved to be effective, as indicated by test coupons or actual devices.

Secondly, a bonding tool configured for 3D Integration of chips onto wafers was systematically investigated as to particulate counts on settling wafers. Numerous hardware improvements were identified and implemented, resulting in more than a twofold improvement in particle counts in key areas.

Finally, a novel tack/collective chip-to-wafer bonding process was demonstrated, wherein a polymer coating enabled chips to be tacked to a wafer, followed by a Cu thermo compression bond to vaporize the polymer adhesive and complete the bonding of all dice simultaneously.

Electrical testing indicated excellent performance with low-resistance contacts.

All three areas showed significant improvement over current methods, with each to be implemented and further characterized on test vehicles and functional devices. Process costs, yields and throughputs are improved by each of these three investigations and will lower the cost of implementing 3D Integration for a variety of device types.

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