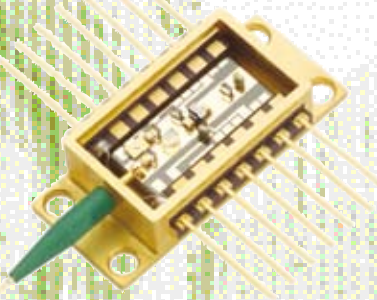
SET Technical Bulletin

DIE BONDING APPLICATIONS



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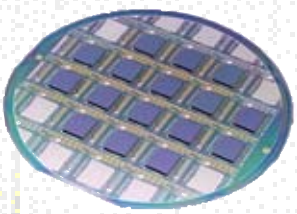

ACKNOWLEDGMENTS

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The material in the SET Technical Bulletin has clearly been derived from many sources including individuals, companies and organizations. We have attempted to acknowledge in the appropriate parts of the bulletin the assistance that has been given. We would like to extend a special thank you to several professional societies for permitting us to reproduce some of their illustrations and information in this SET Technical Bulletin. These include the **Electronic Components and Technology Conference (ECTC)**, the **IEEE International Conference on 3D System Integration (3D IC)** and the **Institute of Electrical and Electronic Engineers (IEEE)**.

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Since the advent of photolithography in electronics in the early sixties, and for decades, most new technology developments for the semiconductor industry have aimed at downsizing the transistors so as to make more integrated, more powerful, faster and even cheaper Integrated Circuits (ICs). Since a few years, this industry has changed and this in turn shifted the paradigm of technology innovation for semiconductors: a consensus is rising within the community of process experts and scientists that further downsizing of the transistors will not only become more difficult because new geometries tend to the physical limit of atom sizes, but it will also come along with lower performance side-effects such as higher parasitic coupling, higher current leakage and thermal issues. From an investors' perspective, the math is simple: in order to reach the next CMOS technology node, huge investments are needed, and the expected benefits are still unclear.

In parallel, electronic applications are being thought differently and processing power is now less seen as an end than as a means to develop and build user-friendly communicating personal devices and appliances. You do not only want a game console with bright and fast high resolution graphics. You now want to interact with it: it can feel and sense you in every possible way, by means of motion and video sensors. Patients with cardiac rhythm malfunctions want to enjoy their lives as they did before being equipped with a pacemaker: continuous monitoring is now made possible as the pacemaker device measures the heart beats and directly sends relevant information via the patients cell phone to his physician without requiring any formal examination at the doctor's. As a consequence, there is rising awareness that integrated circuits are increasingly interacting with the real world by receiving, processing and transmitting more information than ever before. The focus is shifting from the transistors constituting the integrated circuits to their external interfaces, from processors to sensors and actuators, from circuits to systems: the value of semiconductors is shifting from ICs to IC and system packaging.

But the challenges remain the same ones as 50 years ago: how to make high performance, fast, low consumption and

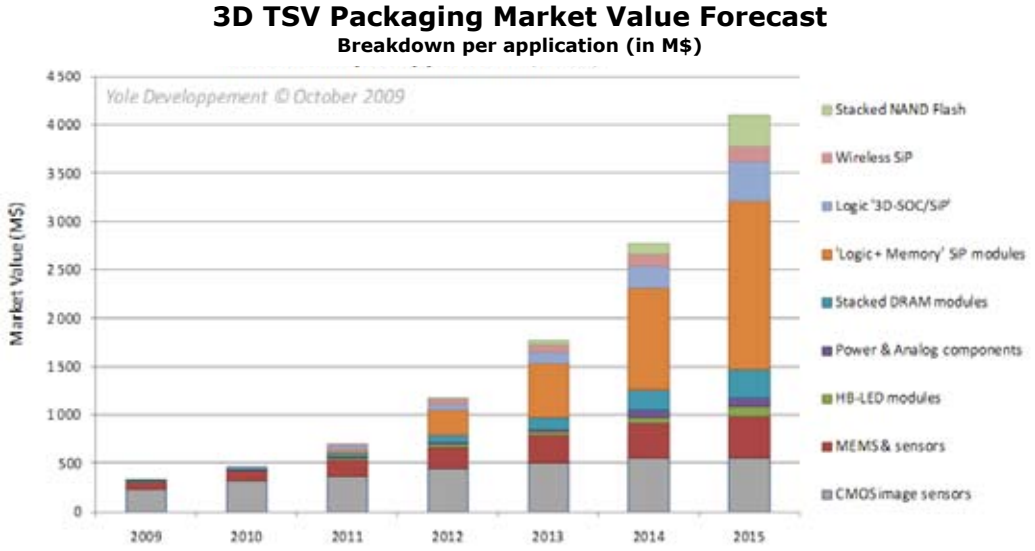

Figure 1 - 3D TSV Packaging Market Value Forecast: Breakdown per application (in M$).

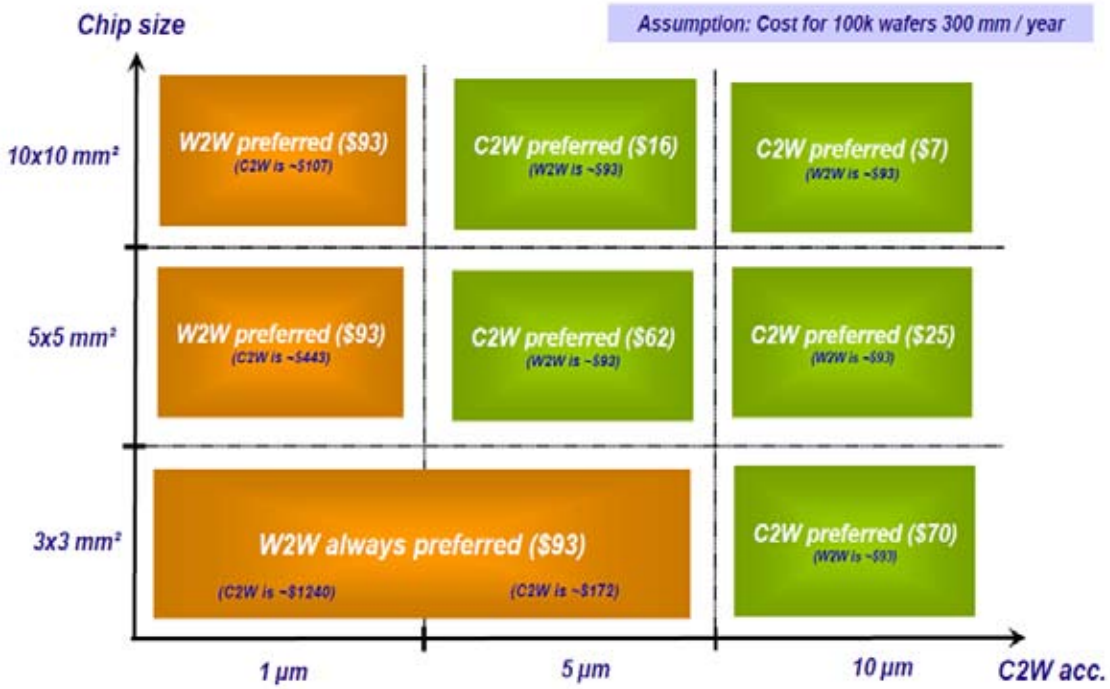

Figure 2 - Cost effectiveness of bonding scenarii function of die size and needed placement accuracy.

cheap highly integrated electronic systems? What is changing is how this is now increasingly being addressed. And the answer stands in a few keywords: mid-end, wafer-level packaging, 3D integration. The whole idea is to pack more electronic function per volume unit (instead of surface area) and to extend the photolithography techniques beyond the making of ICs to their packaging and their integration in a system. And this is a heavy trend: Yole forecasts that from slightly less than M$ 500 in 2010, the market of 3D integration using through silicon vias (TSV) will grow to more than B$ 4 in 2015 (figure 1), addressing a wide variety of advanced systems! Packaging of MEMS and sensors using wafer-level techniques will become mainstream in just a few years as we forecast a compound annual growth rate of 85% over the 2009-2013 time period!

Ahead of time of the other players in the value chain of the semiconductor industry, equipment manufacturers are bound to play an important role so as to tackle the technology challenges and seize the opportunities offered by this paradigm shift. SET demonstrated throughout this technical bulletin their active involvement in each and every area of technology innovation resulting from this industry trend. All the technical articles in this bulletin either deal with 3D integration of integrated circuits or packaging of MEMS and sensors using wafer level techniques, and all of them demonstrate how the SET bonders can be adequately used with varying process parameters: die to die bonding or die to wafer bonding, copper tin or gold tin or solder alloys, with flux or flux-less, with a wide range of die and wafer thicknesses, within front-end or back-end factory environments.

Thanks to the equipment flexibility, recipes combining the right placement accuracy, compression duration, force and temperature can be defined to meet the requirements of bonding strength and reliability with high industrial throughput. Moreover, SET is well-positioned on the die to die (or chip to chip) and especially on the die to wafer (or chip to wafer) bonders which represent the favorite solution for a vast majority of industrials. Indeed, the chip to wafer bonding technique already allows better costs than "chip to chip" as it enables batch processing at the wafer level. On the other hand, it offers more integration flexibility than wafer to wafer as different size ICs using heterogeneous wafer processes can be stacked using chip to wafer. It is also clear that by choosing the chip to wafer bonding option, the bonded chips can be pre-tested, and only good ICs are reported on the host wafer allowing for much higher stack yields than when using wafer to wafer. This accounts for the cost competitiveness of the chip to wafer bonding technique served by SET versus the wafer to wafer bonding technique for many given configurations of die sizes and required placement accuracies as illustrated in figure 2.

SET clearly appears to be well positioned and prepared and with the right focus to address any new opportunity offered by the high growth mid-end semiconductor market of 3D system integration.

An Innovative Die to Wafer 3D Integration Scheme: Die to Wafer Oxide or Copper Direct Bonding with Planarised Oxide Inter-Die Filling

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ABSTRACT

An innovative die to wafer stacking is proposed for 3D devices. Known good-dice are bonded on a processed wafer thanks to direct bonding. Oxide layers or patterned oxide/copper layers are used as the bonding medium. After a first thinning, a low stress high deposition rate oxide is deposited to embed the dice. A final thinning is then done to recover a flat and smooth surface before the through silicon vias.

INTRODUCTION

Combining packaging and system on chip technologies, 3D integration is now seen as an alternative solution to the Moore's law. This technique consists in stacking functional components, interconnected by through silicon via (TSV), and thus maintaining or improving the performances of the final circuit at lower manufacturing cost than similar 2D-IC. Direct oxide bonding is a way to address high density TSV integration. Feasibility demonstrations were already achieved at the wafer level using this bonding method (1). While memory stacking is addressed by a wafer to wafer approach, the die to wafer stacking is more suitable for 3D heterogeneous integration, requesting the bonding of various dies sizes coming from different technological nodes or from different substrate material. A die to wafer stack is also the way to answer yield problems by stacking only known good dice. At CEA Leti Minatec, we are implementing an innovative die to wafer 3D integration scheme based on direct bonding and inter-die filling oxide planarisation. The main specification guide line for this new integration is to allow post processes like TSV without any impact on both the direct bonding and the inter-die oxide (meaning no new technology development to be done or any electrical performances degradation of TSV with respect to those obtained on wafer to wafer bonding).

3D INTEGRATION SCHEME

The integration scheme is the following: on a processed wafer, known good dies are bonded by face to face direct bonding in a pick and place tool either with silicon oxide layers or patterned Cu/SiO_2. The dice are then thinned to the wanted thickness. A low stress high deposition rate oxide is deposited all over the structure as an inter-die filling. This oxide is thinned down to the die backside to recover a flat surface before the whole via process is done. Each step of this scheme will be detailed in the following sections. The advantages of this technology are first that direct bonding allows the thinning of the stack down to only a few microns, then since no polymer is used for the bonding or the inter-die filling, thermal strain is reduced and reliability enhanced, finally post processes are not limited by the bonding layers stability with temperature.

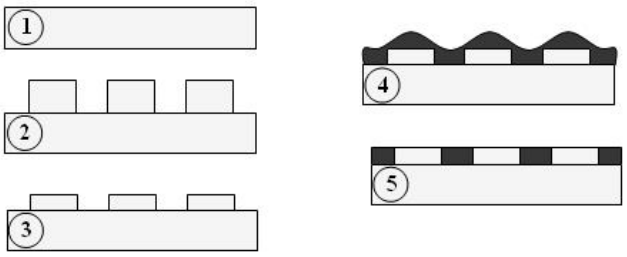

Figure 1 - On a processed wafer (1), known good dies are bonded by direct bonding (2). After a first thinning of the dice (3), a low stress high deposition rate oxide is used as an inter die filling (4). A final planarization is done to allow the via post process (5).

DIE TO WAFER BONDING WITH OXIDE LAYERS

Both die and wafer present continuous surface oxide layer, with buried copper metallization for electrical tests. Surfaces are prepared for direct bonding by mean of mechanical steps (polishing) and chemical steps to achieve high hydrophilic degree. With this preparation a bonding energy G of 1.4 J/m^2 was measured by the double cantilever beam technique on wafer to wafer bonding. Aligned chip-to-Wafer (DtW) structures are realized in an **FC300** equipment from SET to obtain the sub-micrometers alignment required for 3D high interconnection density. Pick&place is then achieved using low pressure (<500mg), at room temperature (~25°C) and for very short contact delay (<20sec). Figure 2 shows an optical microscopy observation of 25 dies bonded on a processed wafer after such a pick&place bonding and a 400°C annealing. After the 400°C annealing, a few non bonded areas are observed. Such defects are attributed to particle contamination of the wafer that occurs during the pick&place sequences. DtW alignment was controlled using Infra-Red microscopy. A misalignment below 1µm was achieved for all the structures. This indicates that high alignment quality DtW structures could be made using direct bonding and pick&place.

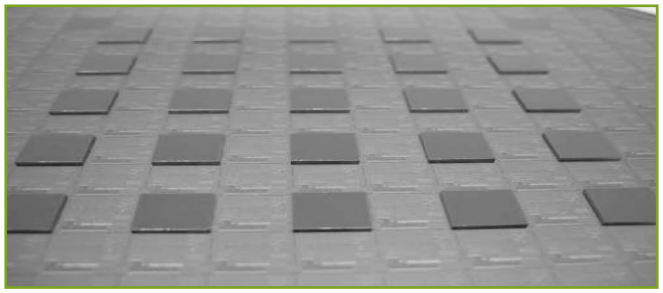

Figure 2 - Optical observation of 25 dies bonded on a processed wafer. The whole structures was annealing at 400°C during 2hrs.

DIE TO WAFER BONDING WITH PATTERNED COPPER/OXIDE LAYERS

Using copper at the bonding interface level is an interesting way to provide both vertical conduction and reliable mechanical toughness (2). To address 3D-ICs applications, an ambient air, atmospheric pressure, room temperature Cu/SiO_2 patterned direct bonding technology has been implemented at the die to wafer level. Low surface roughness, free contamination and flat pattern profile engineering are mandatory to enable high bonding quality (2).

Prior to the dicing, dies are prepared by a CMP process at wafer level to monitor surface adequacy with pattern direct bonding. Since dicing induces huge particle contamination, a die cleaning process is mandatory before bonding. Die to wafer alignment and bonding are then carried out in a SET FC 150 tool. Bonding quality is characterized by Scanning Acoustic Microscopy (SAM) after 200°C/30minutes annealing step. Few non bonded areas are recorded at the patterned bonding interface induced again by particle contamination (Fig. 2). The bonding was effective with copper density of 20% (pad structure and 2% (Kelvin structure). Anyway one as to note that depending of the copper density the bonding energy will range at 200°C from 1.4 J/m² to undebondable structures.

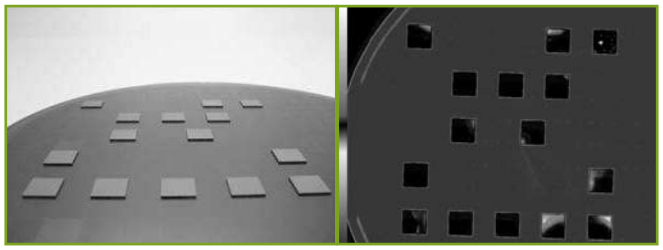

Figure 2 a et b - (left) Optical view of die to wafer SiO_2/Cu patterned direct bonding, (right) Scanning Acoustic Microscopy of the same structure.

The alignment was measured on each die, thanks to cross in box, and ranges from few microns down to 0.5 µm for the best case. The obtained alignment is limited by the capacity of the equipment with our used conditions. Die to wafer SiO_2/Cu patterned direct bonding has been performed with Kelvin structures to allow fine electrical characterization of the bonding interface (Fig. 3). Kelvin structures are obtained by bonding dies on wafers having both a 10 µm branch of the Kelvin structures. The copper to copper contact area is though 10x10µm². The silicon substrates of the dies are removed down to oxide first mechanically and finally with a TMAH wet etch. The silicon oxide is finally dry etched down to the bonding interface to enable probes to connect copper pads (Fig. 4).

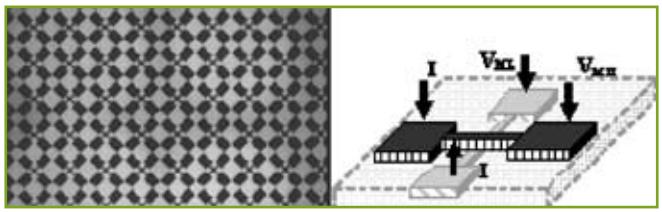

Figure 3 - (left) Infra Red view of Kelvin test structure at the bonding interface before thinning, (right) Principle of the Kelvin structure test.

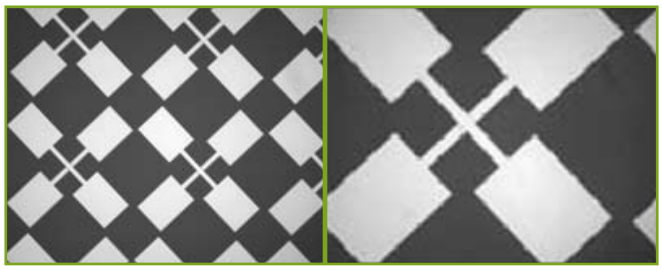

Figure 4 - Optical microscopy of the copper bonding Kelvin structure after silicon and silicon oxide etching. The pads are 95µm large and the bonded zone is 10x10 µm².

Electrical characterization was performed on 400°C/30mn annealed samples. The I(V) curve has a perfect ohmic behaviour (Fig. 5). With four point electrical characterization on Kelvin structures, one can calculate the contact resistance of the copper to copper bonding interface and its specific resistance:

$$R_C = \frac{V_{MH} - V_{ML}}{I}$$

$$\rho_C = R_C \times A_C$$

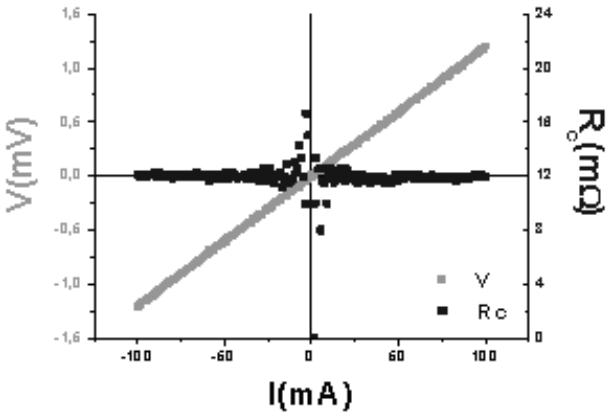

Figure 5 - V(I) and Rc(I) curve on the 10x10 µm² contact area of the Kelvin structure.

With A_c the copper to copper bonded area, V_{MH} the upper

layer electrical potential, V_{ML} the lower layer electrical potential and I the input current. Contact Resistance R_c is 12mΩ for 10x10µm² contact area and the specific contact resistance is 1.2Ω.µm².

This value is in good agreement with wafer to wafer bonding contact resistance measured on similar Kelvin structures (2). Furthermore, this resistance is negligible compare to that of TSV resistance used in 3D IC schemes (1).

INTER DIE FILING AND PLANARISATION

To allow the recovering of a planar surface an inter-die filling must be deposited. For industrial requirements, the filling material must be deposited with an high thickness deposition rate, not be degraded by post process steps (like a 400°C anneal for example), enable an optical alignment through the thick layer and induce a low residual stress. The chosen filling material is a high deposition rate oxide layer with residual low stress. A thickness near 30µm was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) at 400°C. Depending on the deposition conditions, the deposition rate ranges from 1.8 to 3µm/mn and the stress in the film as low as 15 MPa.

The stress induced in the dies was simulated with ANSYS software. The stack is described in figure 6, homogeneous anisotropic mechanical properties of interconnects is used.

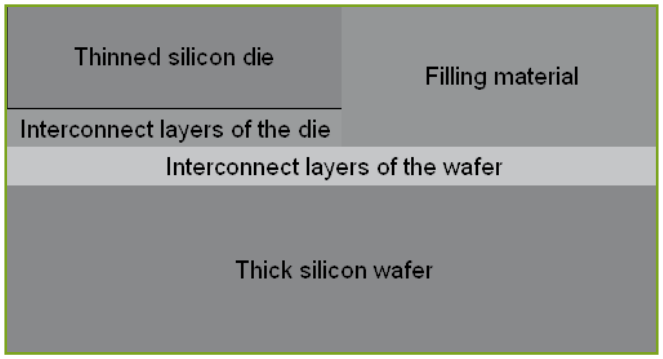

Figure 6 - Simulated area using symmetries of the stack.

Preliminary results show a maximum stress at the edges off the silicon dies of 20 MPa, This stress does not propagate more than a few microns at the edges of the dies.

Figure 7: die to wafer structure after oxide interfiling.

Devices won't be affected by such a stress. Figure 7 is a picture of a wafer after a 30µm thick filling oxide deposition. A recess effect at the edges of the dies appeared after the deposition (Fig. 8). This phenomenon was attributed to a geometric effect and was easily reduced down to 1.4 µm (Fig. 9a).

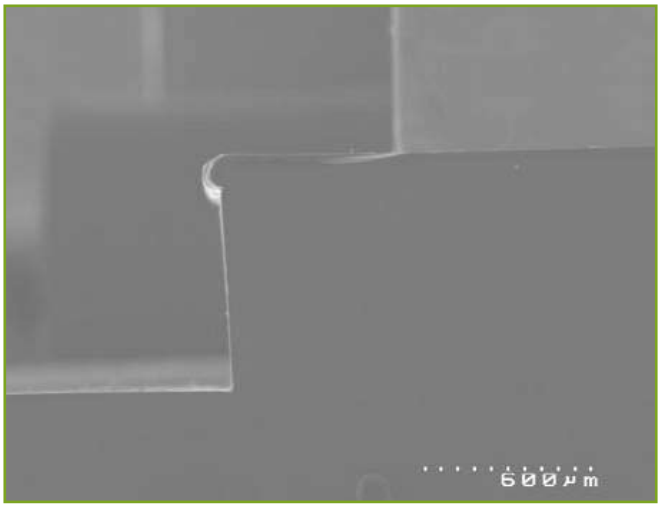

Figure 8 - MEB observation of the oxide deposition on a die, a masking effect is clearly seen at the upper corner of the die.

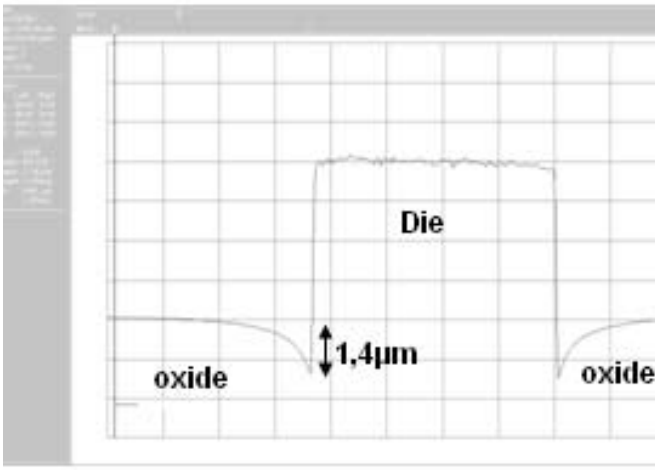

Figure 9a - Oxide recess after deposition measured by profilometry.

In order to recover a flat surface that would allow further technological steps involved in 3D integration processes such as lithography, TSV process or stacking of a second dies level, a planarization stage was developed.

In this process, the oxide layer over the dies is thinned using grinding tools until the recess was removed. Since oxide grinding is very unusual, wheels dedicated to hard material were used. Then, a polishing step is performed to remove the remaining oxide down to the silicon backside, a non selective (Si/SiO_2) specific slurry was used in order to prevent fences creation at the edges of the dies. The targeted final thickness was 15 µm. We obtained a "flat" mixed surface (Si/SiO_2) with a protusion of the silicon dies smaller than 150nm homogeneously on the wafer (figure 9b).

The measured surfaces roughnesses (RMS) are 4nm and 50nm for the silicon and the oxide, respectively. Improvements of this process are still under progress.

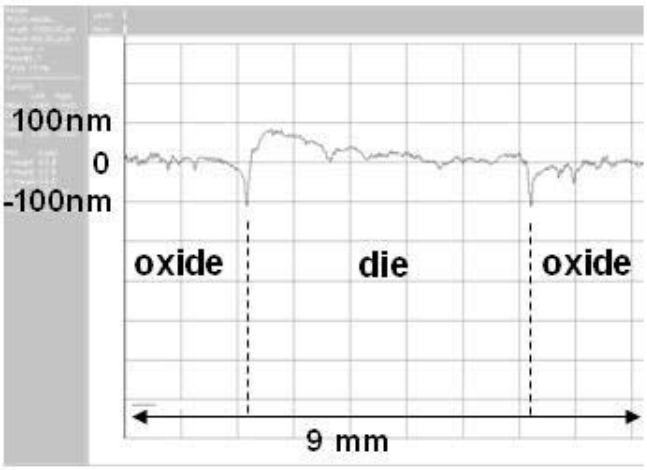

Figure 9b - mechanical profilometer scan of a mixed surface after planrization.

FINAL DEMONSTRATOR

All the described steps were done on processed dies and wafers at a low temperature (< 400°C or < 200°C) to ensure the integrity of the FEOL and BEOL processes already done on the dice or the wafers (Fig. 10). A TSV process described elsewhere (1) was then applied on these wafers without any process adaptation (Fig. 11). The electrical results as for example the measured 3µm TSV resistance of 170mΩ is in good accordance with the values measured for the same structures on bonded wafer to wafer stack. Thus, the feasibility of this innovative 3D integration scheme is demonstrated, improvements are under progress.

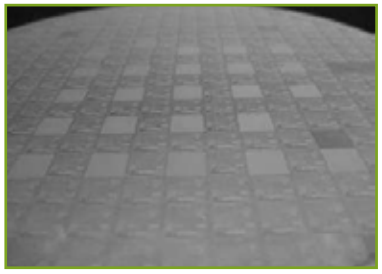

Figure 10: Optical observation of the fully planarised wafer prior to TSV process.

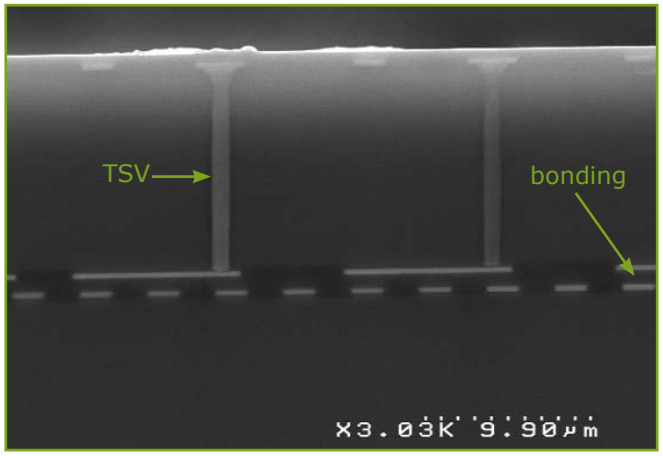

Figure 11 - Cross sectionof the final stack after the TSV process.

CONCLUSION

Each technological step of an innovative 3D die to wafer integration scheme was developed such as: die to wafer bonding with oxide or mixed copper/oxide layer, oxide filling and planarization. and validated in an electrical demonstrator. The obtained results on the first tests are very encouraging. And this technology will be implemented.

REFERENCES

(1) P. Leduc, L. Di cioccio et al, VLSI 2008, "Enabling technologies for 3D chip stacking "proc. p.76-78 (2008).

(2) P. Gueguen, L. Di cioccio et al. 3D "Vertical interconnects by Copper Direct Bonding", MRS fall (2008).

(3) L. Di Cioccio et al. Enabling "3D Interconnects with Metal Direct Bonding" extended abstract IITC (2009).

(4) P. Leduc, L. Di Cioccio et al. " Innovative 3D die to wafer integration scheme based on oxide or copper direct bonding and oxide die inter filling planarization", this conference.

RF MEMS and Flip-Chip for Space Flight Demonstrator

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The next generation of telecommunication satellites payloads will require higher performances and higher functionality for multimedia applications with still stronger constraints on cost and size. That means higher operating frequencies (Ka band), higher flexibility, (reconfigurability, on board processing...) and further miniaturization.

In such a context, RF MEMS – Micro Electro Mechanical Systems – offer new degrees of freedom for the realization of integrated filters, tunable LC circuits, and reconfigurable antennas… They could replace solid-state components thanks to their good microwave performances and even create new functions due to their electromechanical behavior and small size.

An example of an expected redundancy function is showed on the following figure.

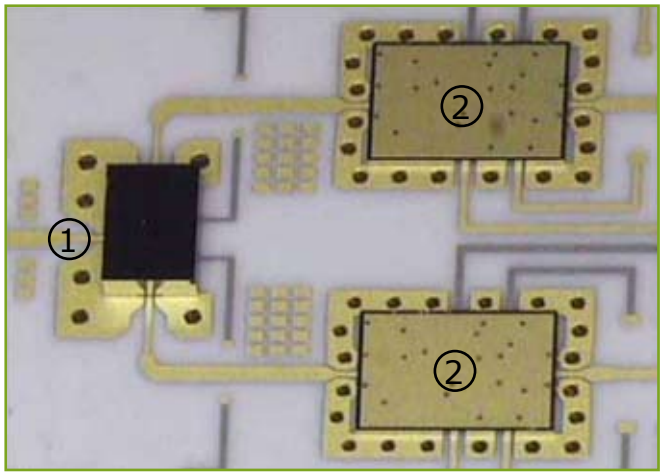


Figure 1 - Example of future trends: self redounded Ka-Band LNA with MEMS:

① Flip-Chipped MEMS Switch (self-packaged),
② Flip-Chipped MMIC LNA.

RELIABILITY IN ORBIT

For RF MEMS switches, one of the main problems to be addressed is the reliability for missions more than fifteen years and the capability to survive at the space environment. A flight demonstration could allow:

- to have the visibility of the new technology for new internal or external customers,
- to go from mid to high TRL (Technology Readiness Level) i.e. to move from «Component and/or breadboard validation in laboratory environment» status to «prototype demonstration in a space environment»,
- to enhance the know-how of such a technology and the associated risk assessment.

A space flight equipment has been defined to demonstrate, in flight condition, RF MEMS capability. This demonstrator has been designed to be full independent and to preserve the payload immunity.

The aim of this experience is to assess the failure modes for RF switches based on ohmic contact technology, which are dealing with the stiction metal-metal at the contact level, the creep for the membrane and the dielectric charging effect due to the electrostatic activation. This will be done through DC measurements using advanced RF switch intrinsic characteristics: the contact resistance Rc during On position and the Vp (pull down voltage).

Twenty MEMS will be used for covering three functioning modes :

- 4 switches with rapid cycle 1 switching per second,
- 4 switches with medium cycle 1 switching per day,
- 4 switches with long cycle 1 switching per year,
- 4 switches will be actuated by remote control from Ground, after 10 years,
- 4 switches where pull-in voltage is monitored to estimate their eventual degradation.

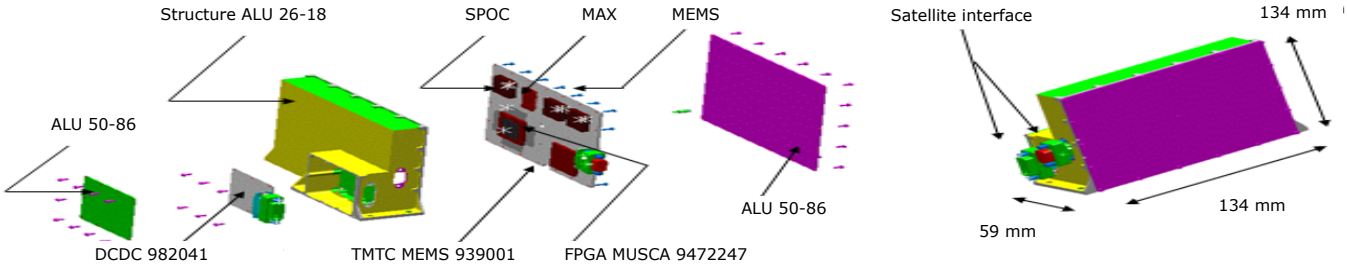
The concept of the demonstrator is illustrated on the figure 2. The RF switches are very small components that require connections as short as possible to preserve all the RF characteristics. So, flip-chip has been selected for assembling and connecting the RF switches. As the objective of this demonstrator is to measure and follow, in flight, the reliability of the RF MEMS switches, those devices will not be measured at the RF performances level. However, the use of flip-chip bonding has been confirmed to be as close as possible to the real application.

This paper focuses on the assembly of the RF switches and the associated hybrid; so, we are first going to discuss about flip-chip based on stud bumps and thermocompression assembly.

STUD BUMPS AND FLIP-CHIP ASSEMBLY

The principle of stud bumps is described on figure 3.

Figure 2 - Concept of the flight demonstrator.



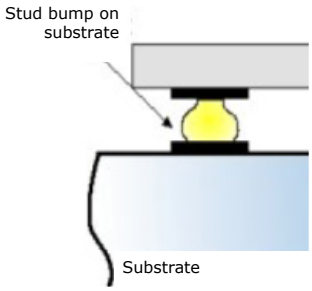


Figure 3
Principle of flip-chip with stud bumps and thermo-compression.

The choice of using stud bumps is driven by several reasons: shortest connections, the use of "standard" device (i.e. with only gold pads for bonding), the capability to make those bumps on any type of substrates, including in the openings of multilayer structures. From a high frequency point of view, the size of the bumps,

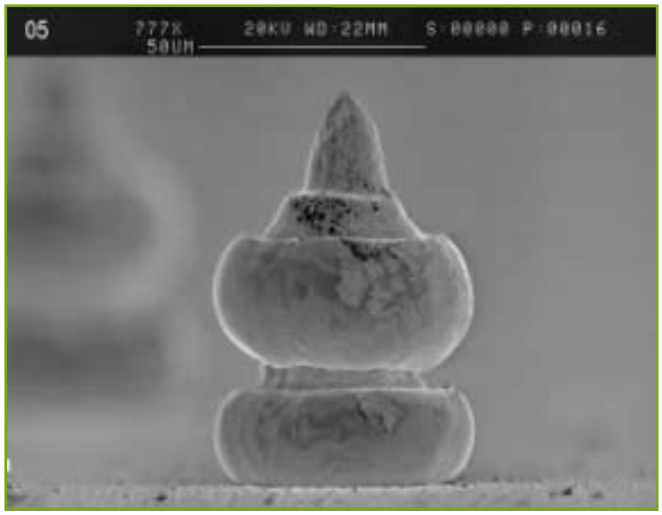
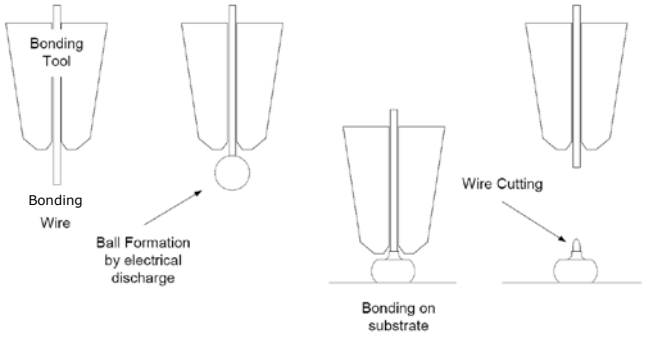


Figure 4 - Double stud bump (Ø 50 µm - hbase = 50 µm - htotal = 80 µm).

and specially the diameter, is compatible of the electrical performances. The capability to make double even triple bumps is also a key point to manage the gap between the component and the substrate. For microwave, the proximity of the substrate with the active face of a device could influence the electrical performances.

The stud bumps are made on a standard ball-bonder, with a modification of the software to allow the break of the wire at the ball level. The wire is doped with palladium to make it more brittle. The different steps are described on the figure 5. The size and geometry for a bump is detailed on the figure 6. One could note than the visible diameter (Dv) is smaller than the diameter (De) of the contact at the substrate level.

Figure 5 - Principle for stud bump manufacturing.



For the specification application described in this paper, we need to have higher bumps to be compliant with the thickness of the caps for the MEMS.
The sizes of those bumps and the die shear have been tested for two different lots.

For information, the minimum required by JEDEC and MIL-STD_883D is a force of 5g/bump.

	1st lot	2nd lot
High (µm)	87	76
Diameter DV (µm)	61	57
Force (g)	21.3 g	26.6 g

A DoE (Design of Experiment) has been implemented to characterize the limits of the main parameters, which are: chip and substrate temperatures, force per bump and time of pressure. The retained criteria's are the electrical performances, the holding of the dice (including the type of break).

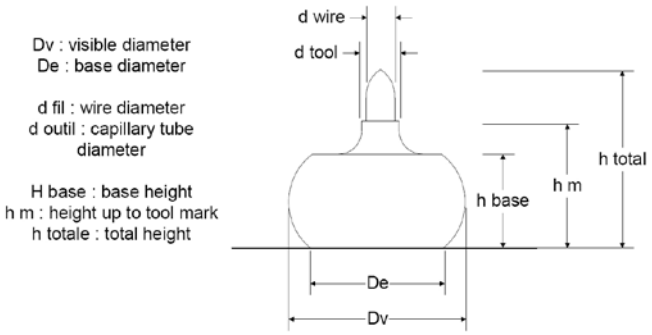


Figure 6 - Stud bump characterization.

Figure 7:
Triple stud bump.

FLIP-CHIP ASSEMBLY OF THE RF MEMS SWITCHES

20 RF-MEMS switches, from CEA-LETI, have to be assembled in hermetic packages.

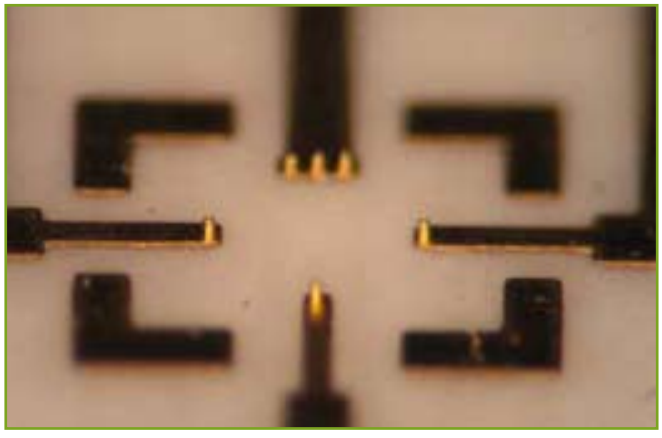


Figure 8 - Stud bumps at the substrate level.

The stud bumps are implemented on ceramic substrates (figure 8).

Figure 9 - SET FC 150 Automated Die/Flip-Chip Bonder.

Then, a **SET FC 150 Automated Die/Flip-Chip Bonder** (figure 9) is used to make the thermocompression bonding on the substrate.

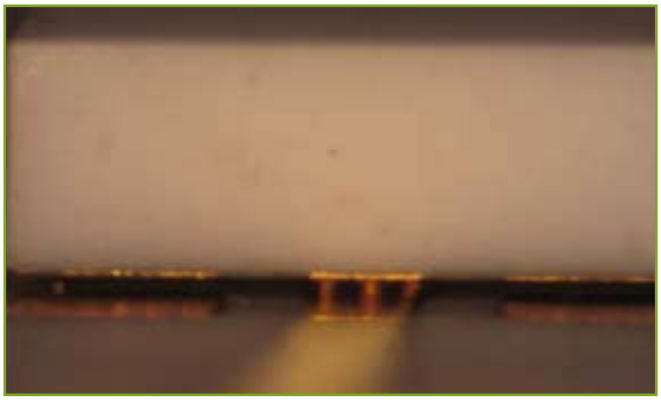


Figure 10 - Bumps under the device.

The good accuracy of this bonder allowed to use very small pads and, as a consequence, to minimize the desadaptation of the RF signal in a real application. The substrate with the device is then bonded into a metallic package, which will be hermetically sealed under nitrogen.

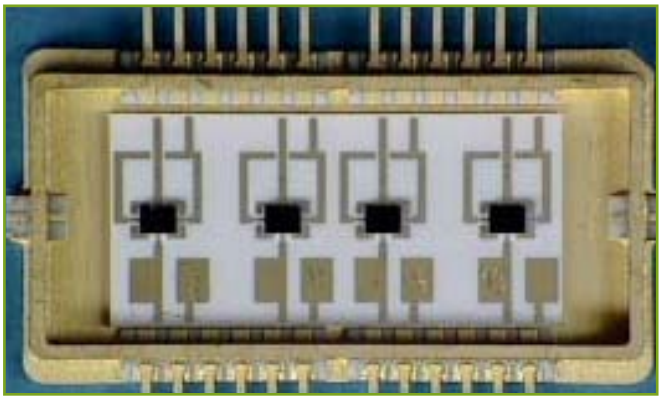


Figure 11 - Hybrid package.

CONCLUSION

A new equipment has been developed aiming at prove in-orbit operation for new RF MEMS switches. This equipment is using an autonomous flight proven interface to the platform and is compatible of GEO telecom satellite working at 36000km.

The use of flip-chip for the connection of the RF MEMS has reduced the length of the RF/microwave connection so that all the intrinsic characteristics are presserved.

The functionality of the electrical model is validated and passed all the standard procedure applied to commercial satellite equipment (EMC, thermal vacuum, vibrations and mechanical shocks).

The fly model is produced, waiting the end of the RF MEMS qualification.

Electrically Yielding Collective Hybrid Bonding for 3D Stacking of ICs

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ABSTRACT

The production of non-monolithic 3D-systems by stacking and interconnecting components through substrate vias (TSVs) is intrinsically limited to the stacking of thin dies, typically ranging from 100µm down to 15µm. Since dies or wafers of such thickness are no longer rigid, it is an important requirement that the bond guarantees mechanical stability and rigidity to the thin stacked die or wafer. The route followed here combines the fixation of a thin wafer or die by means of a dielectric adhesive with the formation of a metallic interconnect. This process is called **Hybrid Bonding**. The introduction of a tacky polymer as an intermediate glue layer in the direct bonding scheme offers the possibility for die-to-wafer throughput optimization: the opportunity lies in the separation of die pick-and-place and bonding operations. This process is called **Collective Hybrid Bonding**. Two polymers have been selected (so called polymer A and polymer B) according to their reflowing and bonding properties, and a die pick and place procedure has been defined and optimized for each of them, allowing a fast and reliable operation. Moreover, electrical measurements of daisy chains showed a comparable and reproducible yield of 80% working chains up to 1000 TSVs.

INTRODUCTION

The restriction in thin die stacking not only stems from the desire to shrink system height, but is also imposed by the limited capabilities of TSV processing. Depending on the type of TSV technology employed, the final wafer or die thickness typically ranges from 100µm down to 15µm. Since dies or wafers of such thickness are no longer rigid, it is an important requirement that the bond guarantees mechanical stability and rigidity to the thin stacked die or wafer. Pure dielectric bonding guarantees such stability simply by the fact that the thin die or wafer is bonded over its entire surface. This method, however, limits the options for electrical interconnection to a via-last approach enhancing the risk of system yield loss during via processing. A very recent approach combines fixation of a thin wafer or die by means of a dielectric adhesive with the formation of a metallic interconnect. This is typically the route followed by IMEC and is so called 3D-Stacked IC (3D-SIC) [1,2]. An illustration of this 3D concept is shown in Fig.1. In this approach, standard single damascene techniques are combined with extreme wafer thinning and direct Cu-Cu thermo-compression bonding.

In this integration scheme, a die-to-wafer stacking approach is preferred: indeed, as compared to wafer-to-wafer bonding, it may be of more interest for the fabrication of heterogeneously integrated systems as it does not impose the requirement of equal die size. The method is also compatible with the selection of Known Good Die prior to stacking and, therefore, is of interest in cases where one of the components in the stacked system is a product with limited yield.

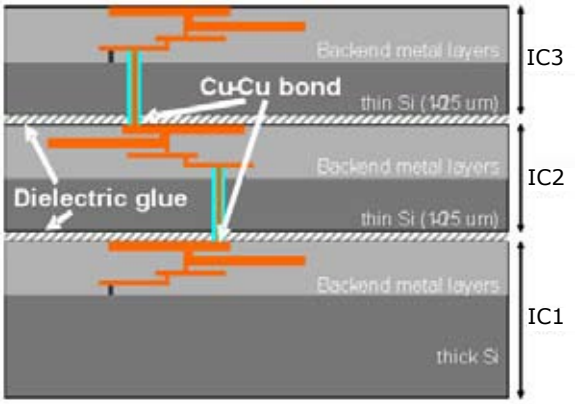

Figure 1 - Illustration of the 3D-SIC concept: dies are separated by a thin dielectric glue layer, and interconnected through Si Cu vias (TSVs).

The cost of die-to-die or die-to-wafer stacking for most bonding methods is limited by the throughput of the process, especially when heat needs to be applied to achieve the bond, which is a lengthy process. The introduction of a tacky polymer as an intermediate glue layer in the direct bonding scheme now offers the possibility for die-to-wafer throughput optimization. This process is called **Hybrid Bonding**. The opportunity lies in the separation of die pick-and-place and bonding operations. First, the TSV-dies are aligned and placed onto a landing wafer on which the polymer glue layer has been previously processed and patterned (by standard photolithography step). This patterned and tacky dielectric weakly bonds the stacked dies and fixes them during further handling. This operation is performed ideally at low temperature with the pick-and-place process repeated until the full wafer is populated. In a second stage, the fully populated wafer is moved to a wafer-level bonding tool where pressure and heat are applied to all stacked dies at once.

Thus, the dielectric layer reflows and the metallic interconnect bonding is performed for all stacked dies simultaneously. This process is called **Collective Hybrid Bonding** and is illustrated in Fig. 2.

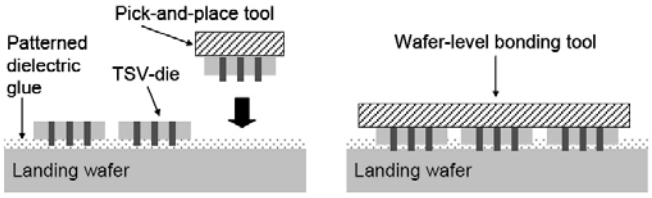

Figure 2 - Illustration of the die pick and place and the collective hybrid bonding process.

The choice of the intermediate glue layer depends not only on its bonding properties that have to be compatible with the Cu-Cu direct bonding process, but also depends on its capability of reflowing and deforming upon application of pressure during the collective bonding process to allow good electrical interconnections between the different top dies and the landing wafer. Two polymers have been selected (so called as **polymer A** and **polymer B**) according to these criteria, and a die pick and place procedure has been defined and optimized for each of them.

DIE PICK AND PLACE AND HYBRID COLLECTIVE BONDING

Different landing wafers were processed by standard photolithography with respectively polymer A and polymer B as glue material. Patterning of the polymer glue layer is required as the collective bonding relies on the reflow and the deformation of the material upon application of temperature and pressure. The patterning of the polymer glue layer results in a uniform distribution of tiny dots across the wafer surface as shown in Fig. 3, except in locations where TSVs will make an electrical contact after bonding.

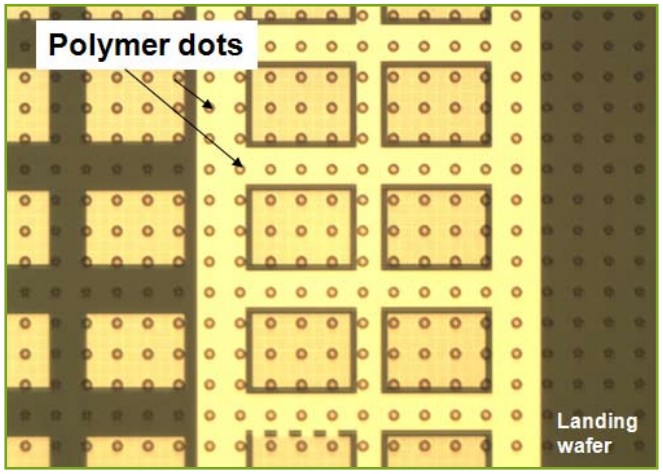

Figure 3 - Optical picture of a landing wafer after dielectric patterning showing a uniform distribution of polymer structures (dots).

The lithography process has been optimized for both polymers to result in a layer thickness slightly higher than the initial TSV hight (typically 0.7µm). The idea of the pick and place procedure is to connect at low temperature the top die to the landing polymer glue layer only, in a fast and reliable operation, leading to a high throughput process. The experimental pick and place operation has been performed at die level (after dicing of the landing wafer) on a flip-chip bonder type **FC150**. Different die attach conditions in pressure, time and temperature have been evaluated.

Figures 4 and 5 show the test conditions as used to determined reliable pick and place conditions both for polymer A and polymer B. Each condition has been tested on 5 samples. The success criteria is defined as 'all 5 samples stay in place'. The experiments clearly show the existence of 2 regions: the first region systematically leads to failure (at least 1 die fell off), and the second determines a safe set of conditions for which a reliable die attach is obtained.

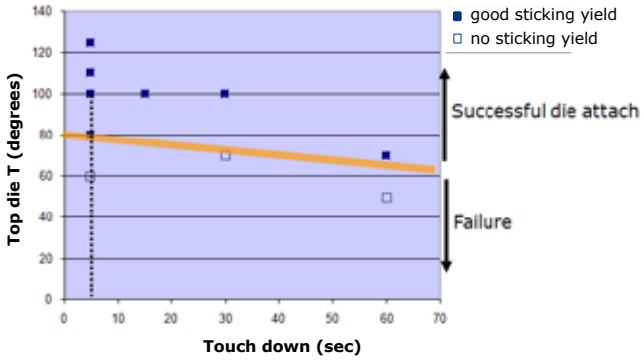

Figure 4 - Die pick and place experimental conditions as function of top die temperature and contact time as used for polymer A.

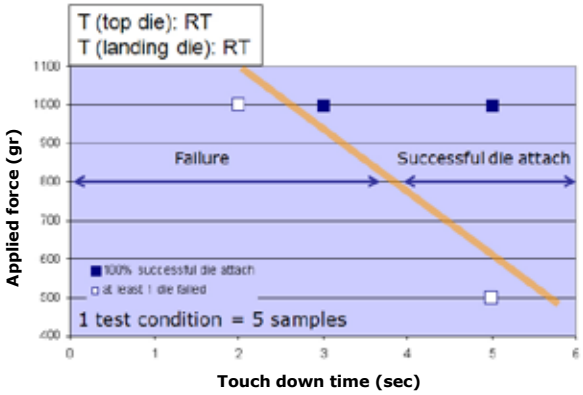

Figure 5 - Die pick and place experimental conditions as function of force and contact time as used for polymer B. Note that both top and bottom dies stay at room temperature.

As shown in Fig. 4 for polymer A, a reliable die attach occurs for top die temperatures above 80°C while the landing die including the polymer layer stays at room temperature. It is an important parameter to keep the bottom die at low temperature to prevent polymer curing during the pick and place operation that would lead to failure. The best conditions have been established for a top die temperature of 100°C, a bottom die at room temperature, a touch down (or contact) time of 5 sec and 10kg force. Lowering the force or further decreasing the touch down time lead to systematic failure (all dies fell off). Concerning polymer B (Fig. 5), both top and bottom dies stayed at room temperature. The variables here are touch down time and contact force. As previously mentioned, the definition of a successful die attach region allows to determine reliable and repeatable bond conditions. As compared to polymer A, a much lower force has to be applied for much shorter times. The best conditions have been

established for a room temperature process, 1kg force and 3sec contact time. With this respect, polymer B is a better candidate than polymer A. A significant reduction in bonding force and contact time makes polymer B an attractive material for die pick and place.

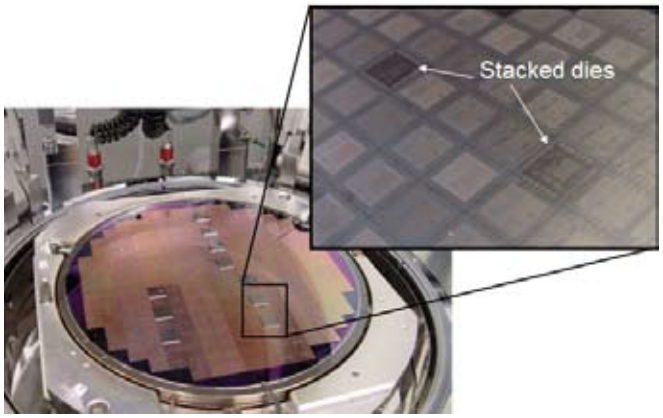

Figure 6 - Picture of a landing wafer after pick and place of 10 TSV dies and collective hybrid bonding.

The next step in 3D stacking is the collective hybrid bonding operation. After populating a landing wafer (including the patterned polymer layer, A or B) with TSV dies and using the best known method as described previously, the landing wafer is transferred in a wafer bonder.

The final bonding process is performed in 2 steps: in the first step at relatively low temperature, the polymer reflows and deforms upon application of a force, putting into contact the Cu TSVs of the top die and the Cu landing pads. In the second step, the temperature is further increased to realize the Cu-Cu direct bonding, and at in the same time the electrical connections between top and bottom Cu layers. A picture of a landing wafer after collective hybrid bonding is shown in Fig. 6. Electrical measurements of daisy chains showed a comparable and reproducible yield of 80% working chains up to 1000 TSVs, both for polymer A and polymer B, as shown in Fig. 7.

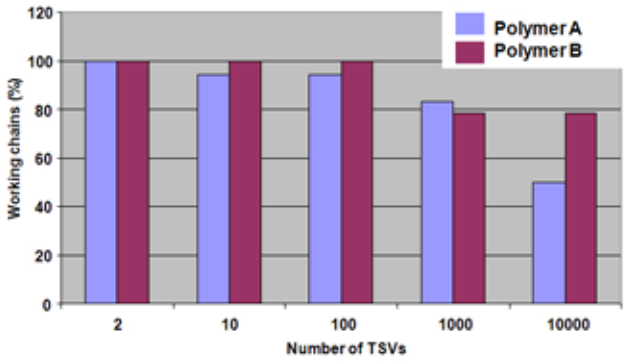

Figure 7 - Electrical yield obtained on 10000TSV daisy chains after collective hybrid bonding with respectively polymer A and polymer B.

CONCLUSION

The 3D stacking approach proposed here relies on the introduction of a tacky polymer as an intermediate glue layer in the direct bonding scheme. It offers the possibility for die-to-wafer throughput optimization. The opportunity lies in the separation of die pick-and-place and bonding operations. Two polymers have been selected according to their reflowing and bonding properties, and a die pick and place procedure has been defined and optimized for each of them. The best known method allows a die pick and place at room temperature, with an indicative throughput of a few seconds per die placement (excluding alignment). After collective hybrid bonding of TSV dies to a landing wafer, electrical measurements of daisy chains showed a comparable and reproducible yield of 80% working chains up to 1000 TSVs.

REFERENCES

[1] A. Jourdain, S. Stoukatch, P. De Moor, W. Ruythooren, S. Pargfrieder, B. Swinnen and E. Beyne,, "Simultaneous Cu-Cu and Compliant Dielectric Bonding for 3D Stacking of ICs", *Proc. IITC Conference, June 4-6, 2007, Burlingame, CA, pp. 207-209.*

[2] B. Swinnen, A. Jourdain, P. De Moor, E. Beyne C. in *"Wafer Level 3-D ICs Process Technology"*; edited by S. Tan, R.J. Gutmann, and L.R. Reif (Eds), Springer, ISBN 978-0-387-76532-7, 2008.

A Fluxless Bonding Process using AuSn or Indium for a Miniaturized Hermetic Package

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ABSTRACT

In the field of high speed data transmissions or in the industrialisation of MEMS devices a hermetic package is often required. However this technological achievement represents an important part of the package price and usually limits the freedom of design and miniaturization. In this paper we propose a localized hermetic sealing method adapted to batch process, that uses either Eutectic AuSn (AuSn20) or pure Indium for the seal ring. A novel fluxless controlled thermocompression process is developed to achieve simultaneously a hermetic bonding and interconnection of I/Os located within the sealing ring through the capping part. Different designs are tested using a standard He aspersion leak test and additionally some reliability tests are performed. Leak rate $<5.10^{-8}$ mbar l/s are obtained with both AuSn20 and In seal rings.

INTRODUCTION

For a long time optoelectronic modules have been dedicated to high added value applications like fiber optic telecommunications. The standard packaging solutions still used in this field are based on multi part optical assemblies hermetically sealed in high cost housings like butterfly packages [1]. More recently, optical links have spread in local loop networks, like Ethernet LANs, Fiber Channel SANs, and Internet switches. These newer applications require high speed high density optical channels at lower cost per data rate. Standard hermetic sealing processes using metallic leads, typically Kovar (Fe-Co-Ni) and local glass solder seals, are very prohibitive and not adapted to these low cost applications. The sealing methods imply either very high temperatures that are above 400°C for glass solder, or resistance welding which is expensive and is limited to a unit process. A batch process which achieves miniaturization of the package is necessary. In the market of MEMS, accelerometers, which are the main industrialized MEMS product used in airbags are typically sealed using a glass frit bonding technology (Bosch). However, as the market tends to go towards miniaturization, metal will prove to be the best choice for hermetic purpose. When reduced to extremely thin wall thickness (10µm) the permeability of metal over glass will hold for much longer (100 years compared to a year). With RF-MEMS device packages, the use of eutectic gold-tin is being investigated [2]. In the optoelectronic package there are today some developments for cheaper and smaller encapsulation using metal seal rings, typically made of AuSn preforms [3]. However the use of AuSn preformed rings has some drawbacks, it is deposited unitarily over the lid or the base and the width of the ring may not be reduced below 400µm for fabrication and handling purposes. Therefore these solutions remain costly and do not properly address the demand for reduced footprint and cost reduction in today's packages.

At LETI, we also have developed a 4-channel high data rate (10 Gbps) small-form factor transceiver [4], shown figure 1. The design of this module is based on an advanced Multi Chip Module technology and embeds optoelectronic devices (laser diode and photodiode arrays) as well as the control electronic ICs (multichannel driver and transimpedance amplifiers respectively).

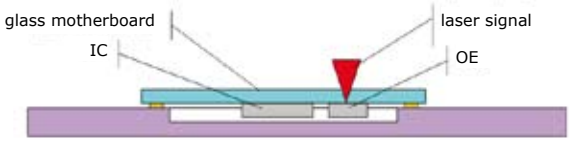


Figure 1 - Schematic of a 4-channel high data rate transceiver.

In order to keep a high degree of reliability required for the application, an original packaging strategy has been developed. The glass motherboard is assembled onto a ceramic package, for example a 44 pad Leadless Chip Carrier with standard dimensions (17x17mm²) made of alumina. The use of a LTCC cofired ceramic package also permits to dramatically reduce cost compared to metallic packages when high quantities are addressed.

On the upper surface of the ceramic package, metalized rings and pads have been designed with the same pattern as on the glass motherboard. The pads are connected to metallic vias that interconnect the electric signal to the pads located on the lower side of the ceramic package. As a result, it is possible to hermetically assemble the glass motherboard onto the ceramic package using solder rings and connecting pads. Hermeticity and electrical connections are simultaneously obtained during the sealing process. Some prototypes were first achieved using non hermetic seals and hermetic seals using AuSn20 preforms.

The development of such packages requires advanced sealing technologies, intended to reduce cost. The remaining of this paper describes the current work on sealing technology for miniaturization.

FABRICATION PROCESS AND SAMPLES DESIGN

To further study such hermetic seals, work on a batch process, optimize the design and solder materials, some test samples are achieved by designing seal rings and connecting pads using sputtering deposition of AuSn20 or evaporation deposition of Indium solder on silicon substrates. Quartz or pyrex chips are used to model the hermetic lid. To achieve the hermetic seal we use AuSn20 and In as the solder material. AuSn20 is already used for fluxless assembly needed in hermetic bonding and leads to stable bonds over time with very high shear strengths. However, its relatively high melting temperature and hardness limits its application where the thermomechanical stress remains low. For this purpose Indium, which has a much lower bonding temperature and which is adapted for the assembly of parts with a CTE mismatch, is also studied. In both cases an evaporation deposition and lift-off process are used to implement and pattern the solder. This technique, in addition of being a batch process, achieves a solder ring with a width well below 100µm, which greatly reduces the footprint of the package. The samples are prepared with ring dimensions of 6mm x 6mm and ring width of 60µm to 105µm for the assembly of quartz on silicon which has a CTE mismatch between 3 and 4 and pyrex on silicon which have matched CTE. With these samples the influence of the thermomechanical stress will be tested over the different solders. Additionally, some connecting pads are implemented within the seal ring to reproduce the I/Os. After deposition the solders are reflown to form smooth ring, ready to be assembled.

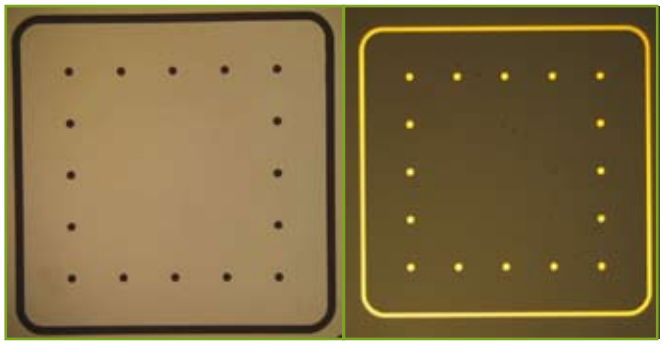


Figure 2 - Test samples: Seals rings and output pads on the silicon substrate and lid.

Different processes are tested for the reflow and lid assembly. Visual observations, cross sections and shear tests are performed to estimate the quality of the bond.

Finally, leak tests before and after thermal shocks are performed to obtain a final qualification of the samples and determines the optimum assembly parameters.

The AuSn20 test samples, shown Figure 2, are fabricated by Reinhartd Microtech in Switzerland [5].The deposition is achieved by alternately sputtering thin layers of gold and tin under vacuum with a total deposition thickness of 4.5µm. 100mm silicon wafers are used to fabricate the substrate and pyrex wafers as well as quartz wafers are used for the lids. The solders are only deposited on the silicon substrates and an Under Bump Metallization (UBM) which consists on an adhesion and diffusion layer as well as a solderable layer is deposited on the pyrex and quartz lids. The top layer is Au which is a good wetting layer, with 0.1µm to 0.2µm thickness not to modify the gold tin ratio after reflow.

The In test samples are fabricated at CEA using the same mask as the AuSn20 samples. 4.5µm of In is deposited using a chemical vapor deposition followed by a lift of process. The same lids are used for the assembly.

SAMPLES DESIGN

The rings are 6mm square with varying widths from 60µm to 105µm and the interconnect pad diameters vary as well from 60µm to 105µm. The substrates and lids have matching design so that the ring and output pads correspond to each other, however, the width of the ring may vary between the two. A schematic of the solder and under layer is shown in figure 3.

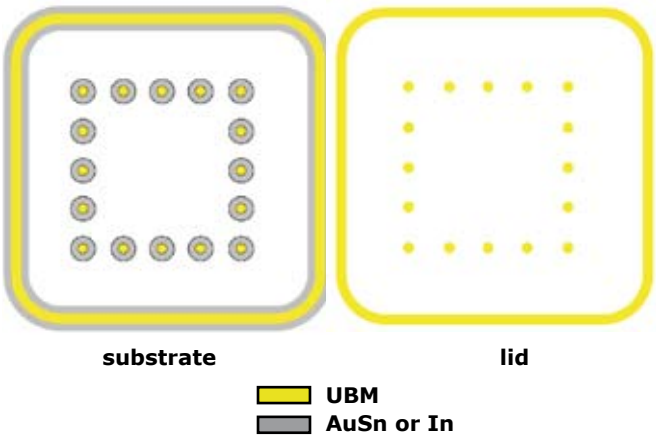


Figure 3 - Rings and bumps designed.

It has been previously observed that the design of the deposition ring and its under layer require special care otherwise there is a risk of local excess of metal upon reflow. Different combinations between the width of the ring, the under metal layer on the substrate and on the lid are therefore tested. These differences achieve different ring height and bump height, the bumps being slightly higher than the ring after reflow. The ring squares have rounded corners and some geometric changes within the under metal layer are also tested to reduce the possibility of metal excess after reflow. A total of 64 configurations are tested.

REFLOW PROCESS

The reflow process is necessary in both cases to obtain the desired geometry before assembly. Upon reflow, smooth rings and bumps with the proper height are obtained and in the case of AuSn20 the eutectic gold tin which consists of a mixture of the Au_5Sn phase and AuSn phase (see figure 4) is generated. For this step a liquid flux or an active atmosphere is possible since it may be followed by a cleaning step. Indium is well known in the field of infrared detector [6] and its reflow process straightforward under flux or active atmosphere.

The reflow process is generally performed for a few minutes at about 15°C higher than the 156°C melting temperature

of In. AuSn20 is generally deposited by electroplating [7], or molded into a preform, but on rare occasions deposited by sputtering as described above.

In all cases a reflow process is necessary. For preform it achieves the mechanical contact between the under layer and the preform and a tacking medium is often used after the placement of the preform. In the other cases the formation of the eutectic phase needs to be achieved. It can be seen from the phase diagram that a slight increase of Sn or Au in the solder changes dramatically the reflow temperature. In addition, if the phases are not carefully controlled the mechanical properties and the intermetallic compounds are modified [8]. So the ratio between Au, Sn and the Au under layer must be carefully chosen and controlled upon deposition. Different techniques are possible to create the eutectic. One process consists of aging the samples in a reflow oven under vacuum for 4h at 200°C [9].

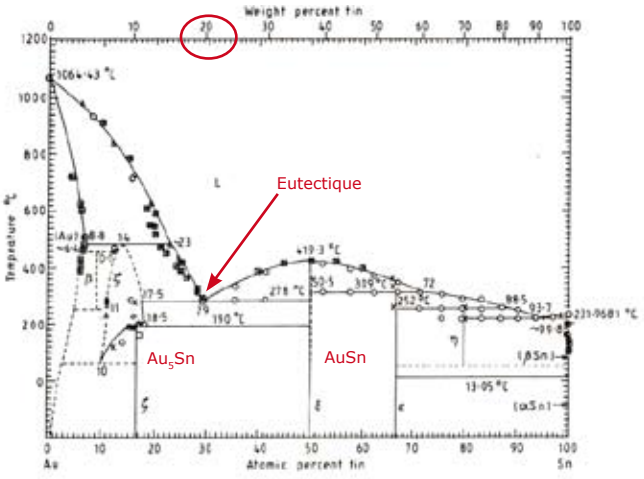


Figure 4: AuSn Phase diagram.

However, it is faster to use a reflow process between 310°C to 320°C under an active atmosphere [9,10] for just a few minutes.

This step is a critical part of the whole assembly process so the AuSn20 behavior is first studied before working with the designed samples. We use some AuSn20 preform on silicon substrate to first qualify the behavior of eutectic gold tin with respect to varying temperature, atmosphere (active or non-active) and observe its wettability as well as its mechanical behavior. The reflow temperature is varied from 300°C to 400°C and the time at peak temperature is varied from 30 sec to 10min.

The results are shown in figure 5:

320°C under N_2H_2 or N_2

400°C under N_2H_2 or N_2

300°C under active atmosphere

Figure 5 - Behavior of AuSn perform upon reflow.

All the preforms are the same size. Since AuSn20 does not wet silicon, the preform should reduce its contact with silicon and form a nice sphere after reflow. All the preforms start melting at 280°C, but only with an active atmosphere does the solder form a nice sphere. Under non-active atmosphere the preform does not de-wet the silicon substrate and the surface tension forces are not strong enough to break an oxide layer that has formed. The temperature has a limited effect compared to the atmosphere activation.

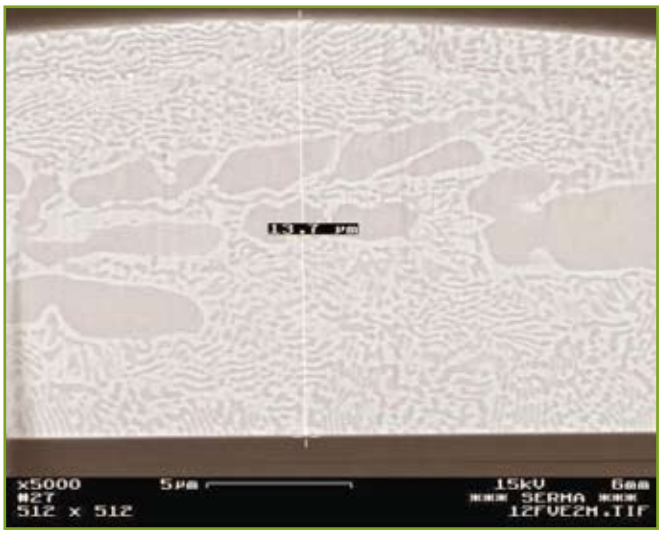


Figure 6 - SEM Image of a reflown sample showing the formation of the Au-Sn eutectic phase.

From these experiments a reflow process with an active atmosphere under 320°C is chosen for our samples. After reflow, not only must the geometry and final surface be perfect to achieve hermetic sealing with the lid, but also the metallurgy of AuSn20 must be carefully controlled. It is therefore necessary to verify that the proper intermetallics are achieved. Some SEM images of cross samples, showing the metallurgy of AuSn20 are seen figure 6. The dark phases represent AuSn and the light phase Au_5Sn. It can be seen that the solder exhibits a nice mixture of both phases with slight local excess of AuSn. Optical observation of the rings can also

be seen in figure 7:

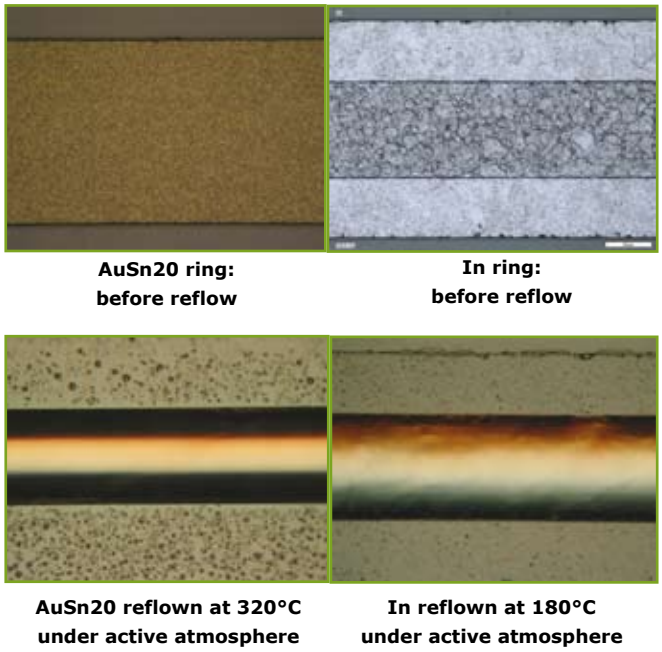


Figure 7 - Reflown samples.

Figure 7 shows the results for both AuSn20 and In rings. The 4.5µm layer deposited changes into a nice smooth 10µm to 20µm high ring. Both processes work very well for this operation however the different design leads to different results. Indeed if the ratio between solder material and under bump layers is not carefully chosen some material excess is locally observed, especially on the ring corner as shown figure 8.

Figure 8 - Local material excess upon reflow.

Finally, this step, which is critical for the rest of the process, is controlled by two major aspects. First, the solder material must be carefully controlled to obtain a good reflow and second, the design must be carefully studied to prevent local defects. If it is rather simple to reflow a sphere, it becomes very challenging to control the solder geometry over an entire ring. Only 14 configurations are finally kept, which lead to ring height from 10 to 20µm. AuSn20 and In lead to the same results so that the same configurations are kept for both solders. This step proves, however, to be easier with In as no eutectic formation is necessary. The mechanical properties and reflow temperature are dependant of the metallurgy and to obtain a good eutectic solder an homogenous mixture of Au_5Sn and AuSn must be achieved. Additionally the sphere height is designed to be slightly higher than the ring's so that the bumps first contact the lid and helps the auto-alignment of the lid over the substrate. Upon assembly the bumps spread over the lid UBM and the ring contacts the lid (see figure 9, patent US6566170B1 1).

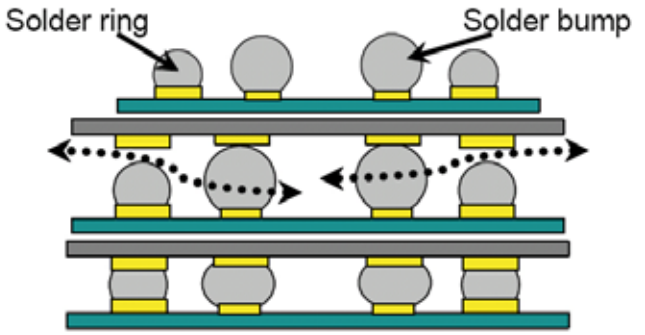


Figure 9 - Bumps and ring height before and after assembly.

ASSEMBLY PROCESS WITH EUTECTIC GOLD TIN

This process must be performed in a clean atmosphere, N_2 or under vacuum as after sealing the cavity within the ring remains hermetic. Some gas could damage the active components within the cavity and reduce the lifetime.

Different parameters are studied to optimize these assemblies: the sample preparation, the temperature and the assembly time, and finally the pressure applied. For this process step we use a flip-chip equipment, **FC150**, developed at SET [11]. This type of equipment enables to adjust the important parameters and to achieve batch processing [12].

As stated earlier two different lids are tested: quartz, which has a CTE of about 0.5 ppm or pyrex, which has a CTE matched with silicon. The quality of the assembly is determined by the wettability of the solder, the height of the final ring, the shear strength and finally the leak rate.

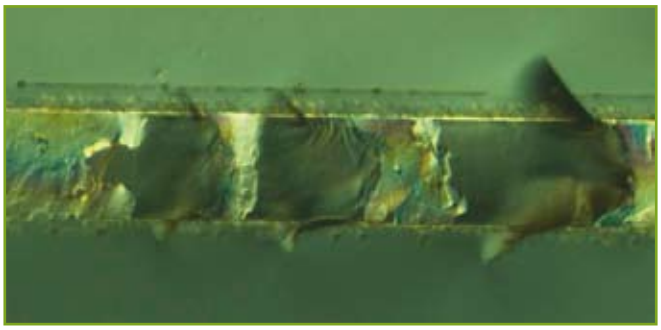


Figure 10 - Assembly of Si and quartz samples exhibiting cracks.

The first samples are assembled under N_2 without any prior preparation at 320°C for a few minutes. However some optical observations after bonding and after lid removal show several problems. First, with the quartz sample, the CTE mis-

match between Si and quartz is too high and causes local cracks on the lid at this temperature (figure 10). AuSn20 is a very hard solder and does not deform under stress so that the difference in deflection causes the quartz to break.

Second, if the pyrex samples are properly assembled some wettability issues are observed after removal of the lid (Figure 11).

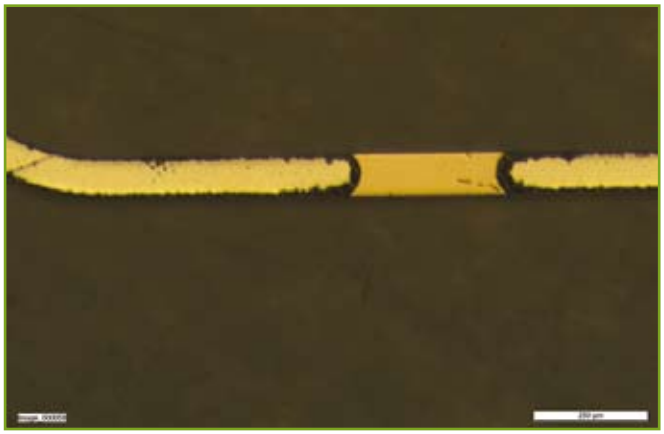


Figure 11 - Optical observation of the lid after removal.

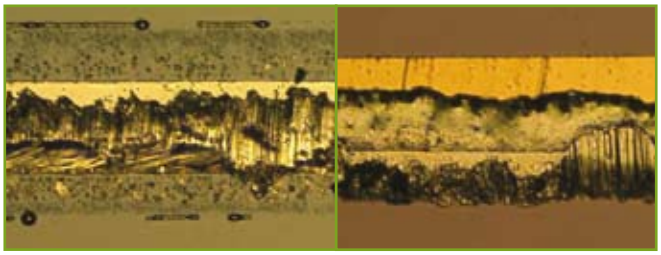
Optical observations of the lid after removal show some zones where the ring does not wet the UBM. This problem is only observed on the ring as all the bumps properly wet the lid. Again, some of the challenges arise from the complex geometry of the sample.

It is then decided to test only the pyrex lids, which have a CTE matched with silicon, and to improve the process by preparing the surface before assembly. Two different preparations are tested, a deoxidization of the solder with an acid prior to assembly and a cleaning of the surface with an oxygen plasma. More assemblies are performed at 330°C under a confined Nitrogen atmosphere.

Additionally another process, called reflow compression, using pressure is tested. Because AuSn20 is a very hard material the samples are also heated and some mechanical stoppers are used to prevent full collapse of the solder.

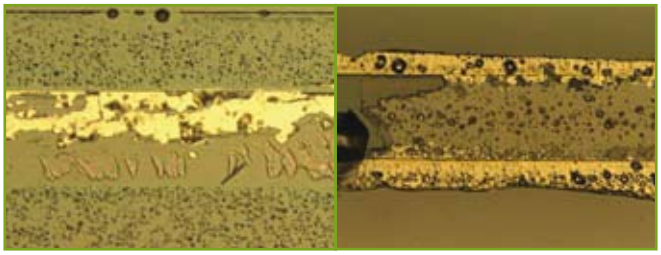
The results show very good bonding in all cases. Cross sections are observed with an SEM and the shear force of the joint is also measured using a Condor shear tester from Xyztec. The values vary from 54MPa to 113MPa, the lower forces are found for the samples assembled under Nitrogen and the higher forces for those assembled by reflow compression.

However, a sample that is subjected to an oxygen plasma prior to assembly has the highest value, proving that with a very clean surface the bonding strength is enhanced. It is also interesting to note that the shear failure occurs within the UBM for all substrates except those that are exposed to an oxygen plasma prior to assembly, confirming the idea that the cleaner surface facilitates the liaisons between the solder and the under layer (Figure 12).



Substrate with plasma O_2 prior assembly after shear test

Corresponding assembled chip after shear test



Substrate assembled under reflow-compression after shear test

Corresponding assembled chip after shear test

Figure 12 - Samples after sheatest.

The cross sections presented in figures 13 through 16 show two phenomena. First, some voids are observed within the ring after assembly, mostly with the reflow process. Second, some delamination is observed between AuSn20 and the UBM of the lid.

Following these observations a series of 15 samples are assembled, 9 using the reflow process with either acid or plasma pre-treatment and 6 using the reflow compression process with acid pretreatment. For these samples the ring width varies between 60µm to 105µm so that after reflow the ring height varies between 10µm to 20µm.

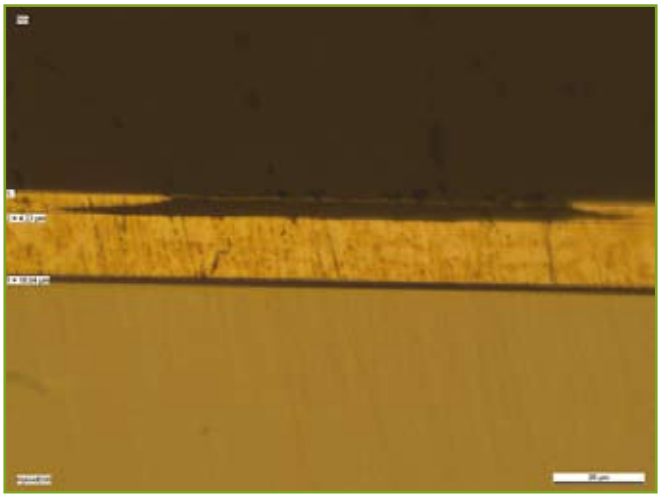


Figure 13 - Delamination observed after reflow assembly between AuSn20 and the UBM.

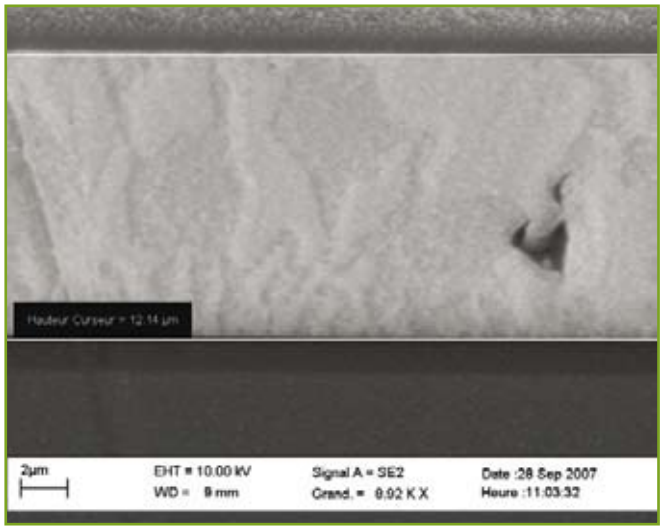


Figure 14 - Voids within the ring after reflow assembly.

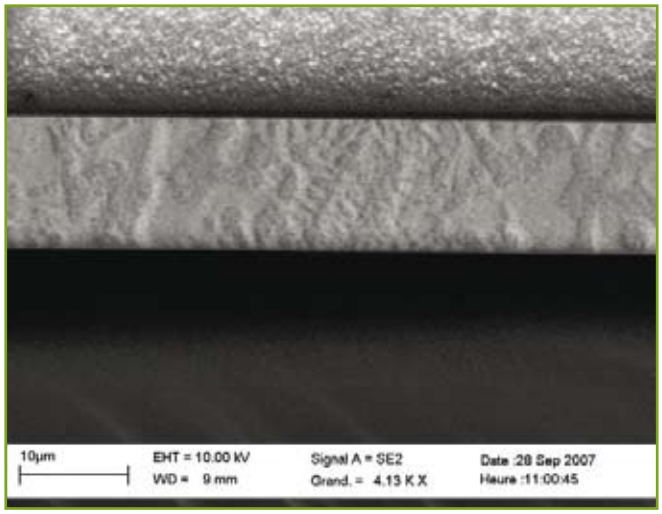


Figure 15 - Zone without defects after reflow assembly.

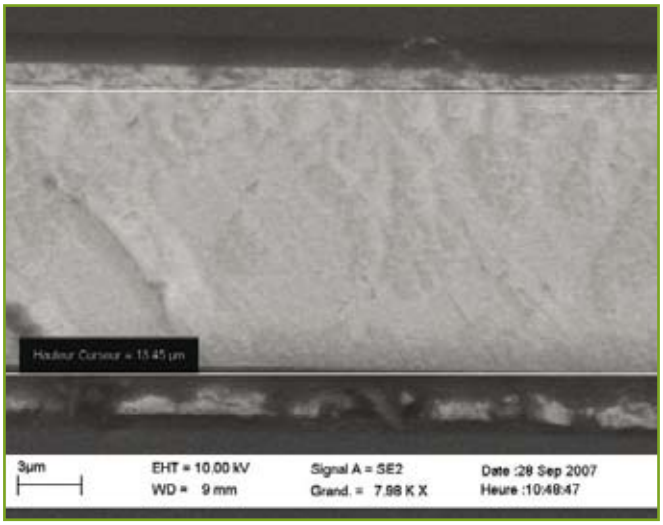


Figure 16 - Assembly with reflow compression process.

HERMETIC TESTS

Hermetic tests are performed on these samples to evaluate the quality of the final bond. The hermetic measurements are performed following the MIL-STD-883^{E} norm. Two different tests must be performed, a fine leak test which should measure the leak rate down to about 1.10^{-9} mbar l/s depending on the equipment sensitivity and a gross leak test which should measure the leak rate down to 1.10^{-2} mbar l/s. The gross leak rate is done using a perfluorocarbon liquid (Galden O2 from ISATIS) which is heated to 125°C, the condition of the testing does not exactly follow the norm since the indicator fluid used is air, and the device is not placed in a vacuum/pressure chamber prior to testing.

However, this test is fast and simple and manages to eliminate quickly the samples with major defects. For fine leak test we follow the A4 test condition procedure. In this method a fixture is directly mounted onto the leak detector (a He spectrometer) and proof of the fixture integrity is first performed (that is no leak at the interface between the fixture and the detector). A cavity is drilled with a micro drill through the package to be tested then, it is mounted hermetically to the fixture. The external portion of the package is flooded with Helium gas and the measured leak rate must not exceed 5.10^{-8}. The sensitivity of our device here is 1.10^{-10} so that using an aspersion method both fine leak and gross leak should be detected.

N°	Process	Leak rate (mbar l/s)
1	Acid treatment + 330°C N_2 reflow	1.10^{-9}
2	Acid treatment + 330°C N_2 reflow	1.10^{-2}
3	Acid treatment + 330°C N_2 reflow	$2.8.10^{-3}$
4	Acid treatment + 330°C N_2 reflow	2.10^{-3}
5	Acid treatment + 330°C N_2 reflow	2.10^{-2}
6	Acid treatment + 330°C N_2 reflow	$2.5.10^{-2}$
7	Plasma treatment + 330°C N_2 reflow	2.10^{-4}
8	Plasma treatment + 330°C N_2 reflow	$1.2.10^{-5}$
9	Plasma treatment + 330°C N_2 reflow	2.10^{-8}
10	Plasma treat. + 330°C reflow compression	1.10^{-9}
11	Plasma treat. + 330°C reflow compression	1.10^{-2}
12	Plasma treat. + 330°C reflow compression	1.10^{-8}
13	Plasma treat. + 330°C reflow compression	7.10^{-10}
14	Plasma treat. + 330°C reflow compression	$5.4.10^{-9}$
15	Plasma treat. + 330°C reflow compression	2.10^{-4}

Table 1 - Leak rate measured for all samples.

With a pressurized chamber test method the time between

immersion in He and detection is generally too long to detect gross leaks as the gas has already left the sample before being measured, however, in the aspersion method the immersion in He and the detection are achieved at the same time. The results are summarized table 1.

The acceptable limit is set to 5.10^{-8} mbar l/s according to norm 1014 of the MIL-STD-883^{E}, which is achieved for 2 samples with N_2 reflow and 4 samples with reflow compression. The pretreatment seems to help and a combination of the two may lead to better results. Only 2 samples out of 9, have a leak rate below the limit for the reflow process. It is therefore possible to use this method for hermetic bonding but some improvements are necessary to increase the yield. The problems probably arise from holes within the AuSn20 ring which is a common effect with gold tin when no pressure is applied. A vacuum environment would probably be very useful in this case. With the reflow compression method, 4 samples out of 6 are within SPEC, which is a very good result. In addition the height of the ring after assembly is controlled. It is suspected that with both methods, some issues arise from defects within the ring after reflow. In both cases, the ring width does not have a significant effect and no differences are observed in the result. In the case of the reflow process the final height of the assembly is a few microns shorter than after reflow and in the case of reflow-compression process the final height is defined by the stopper height. The stopper height is generally chosen a few microns shorter than the ring height. However, no optimization of the stopper height and thus seal height is achieved in this study.

ASSEMBLY PROCESS WITH IN

Indium is not usually used for hermetic assembly, however, it is a soft solder that reflows at low temperature (156°C) and therefore presents two advantages over AuSn20 to accommodate the CTE mismatch. In the field of infrared, it is often used with flux as it usually exhibits a thick oxidation layer which must be reduced before assembly. In this study the use of flux is prohibited so a thermocompression assembly method is investigated. As stated above, the same samples as with gold tin are used.

A preliminary study using temperature from 100°C to 150°C and pressure from 10 to 50MPa with different sample preparations is first performed. The samples are finally assembled at 125°C under 40MPa, right after a reflow process which helps limiting the oxidation layer. The assembly time is varied from 1, 3 and 5 min, some stoppers are also added to control the final ring height. After inspection, these samples are tested with the gross leak test in order to qualify the different assembly times. The results show respectively a 15%, 50% and 100% hermetic yield for 1mn, 3mn and 5mn, proving the major impact of the assembly time. It can be explained by looking at the interdiffusion equation between gold and In [13]:

V (µm/h) = exp(-8410/T) + 20,35 (T en Kelvin)

So that at 125°C the $AuIn_2$ intermetallic layer that forms between gold and indium thickens over time and can be compared with that of a reflow assembly at 180°C under flux (Table 2).

T (°C)	V (µm/h)	Time (s)	$AuIn_2$ thicknesses (nm)
125	0,46	60	8
125	0,46	180	23
125	0,46	300	38
180	5,96	20	33

Table 2 - $AuIn_2$ intermetallic layers thicknesses calculated with different assembly parameters.

From this table it is clear that to obtain similar intermetallic layers between a reflow or a thermocompression assembly it is necessary to keep the pressure and the temperature for at least 5 min.

Great care is also taken for the pressure application so as to achieve an assembly with uniform height and to obtain hermetic cavities. Optical observations of the ring, shown in figure 17, are also performed after assembly.

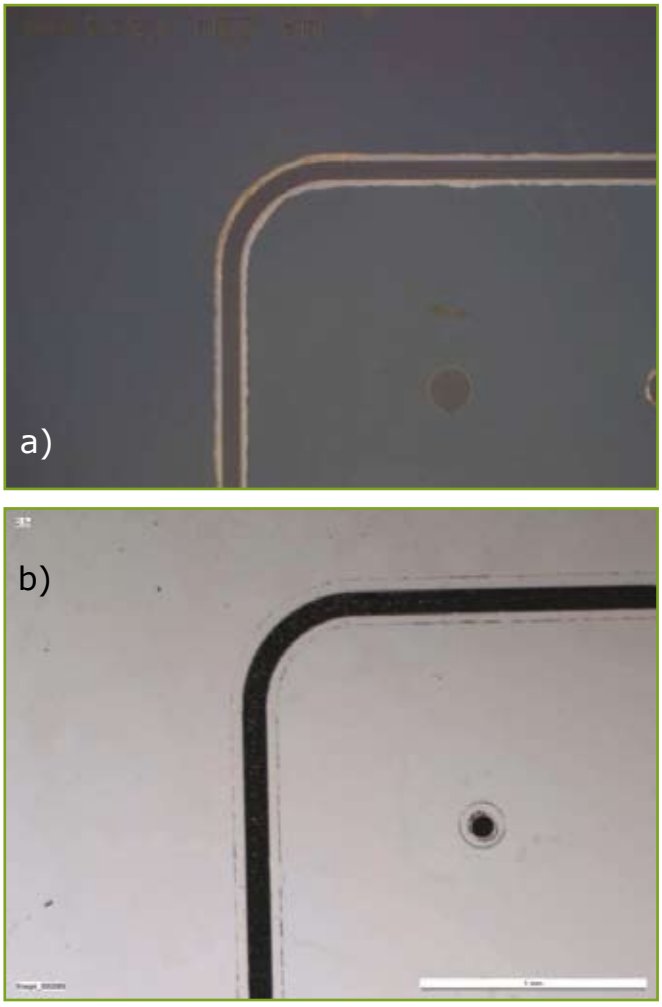


Figure 17 - Optical observation of the ring after assembly a) and after lid removal b).

These observations show that indium is uniformly spread around the UBM which indicates that the pressure is applied

uniformly, enhancing the chances of having a hermetic assembly.

Both quartz and pyrex samples are tested and no differences are observed. Since most pyrex samples are used for the gold tin assembly, we mainly use quartz samples. 11 such samples, with ring width from 60µm to 105µm, are achieved using the optimized assembly conditions and tested under the same fine leak conditions as explained previously. The cavity to test these samples is generally made after assembly except for a few samples.

The results are shown in table 3:

Sample	Process	Leak rate mbar l/s
1	125°C – 300S	$< 10^{-8}$
2	125°C – 300S	$< 10^{-8}$
3	125°C – 300S	$< 2.10^{-9}$
4	125°C – 300S	$< 1,2.10^{-8}$
5	125°C – 300S	$< 2,6.10^{-8}$
6	125°C – 300S	$< 3.10^{-8}$
7	125°C – 300S	$< 5.10^{-9}$
8	125°C – 300S	$< 1,5\ 10^{-8}$
9	125°C – 300S	$< 1,2\ 10^{-8}$
10	125°C – 300S	$< 1,1\ 10^{-8}$
11	125°C – 300S	$< 1,2\ 10^{-8}$

Table 3 - He Leak rate results with Indium ring.

All samples are within spec which is an excellent result. In addition, these assemblies proved to be robust as the hole for leak rate testing is made after assembly which may induces large mechanical stresses on the ring, however it does not seem to influence the result. Again, no influence of the ring geometry is observed.

RELIABILITY TESTS

As indium is not a standard solder used for hermetic sealing, some fatigue tests are performed on the samples. They are subjected to thermal shocks as described below:

- Immersion under 0°C water followed by immersion under 100°C water
- -40°C to +85°C at 10°C/min with 10 min plateau.

The results of these tests are shown in table 4 and figure 18:

Sample	Leak rate before shock mbar l/s	Leak rate after 20 shocks mbar l/s
1	$< 1,5\ 10^{-8}$	2.10^{-8}
2	$< 1,2\ 10^{-8}$	$2.2.10^{-8}$
8	$< 1,1\ 10^{-8}$	$1.1.10^{-8}$
9	$< 1,2\ 10^{-8}$	$1.5.10^{-8}$
10	$<10^{-8}$	$1.6.10^{-8}$
11	$<10^{-8}$	$2.4.10^{-8}$

Table 4 - Leak rate measured after thermal shock.

Again these results are excellent as there is almost no modification of the leak rate before and after the test. It is very promising and shows the robustness of the seal considering the CTE mismatch between the silicon substrates and the quartz lids. Some heights measurements of the ring are also done and no significant evolution is seen. Indium proves to be a good reliable sealing solder, and a robust assembly method is defined here.

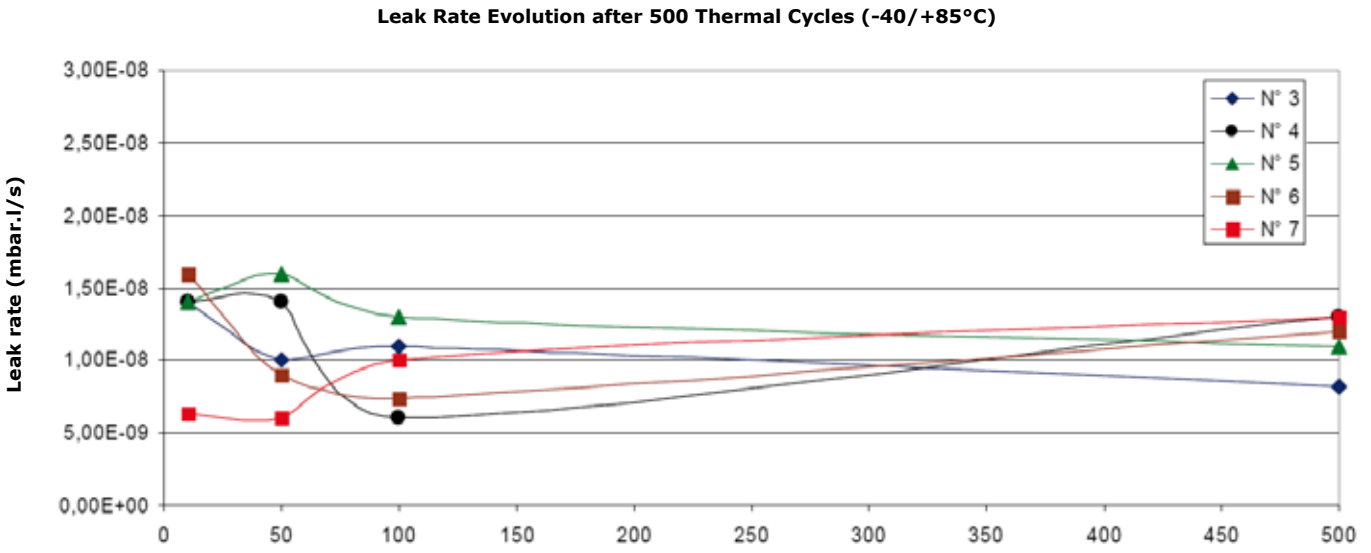


Figure 18 - Evolution of the leak rate after 500 cycling from -40 to +85°C.

CONCLUSIONS

A fluxless sealing method using either AuSn20 or Indium is demonstrated. It achieves hermetic bonding using ring as thin as 60µm wide and a batch deposition process. Two reliable hermetic bonding processes are defined: a reflow compression for AuSn20 and a thermocompression for Indium. In both cases a batch process is demonstrated: The reflow process may be implemented on a full wafer level under a controlled atmosphere and the assembly process using low pressure may be achieved by groups of substrates under a compression arm.

Indium is found to be a very reliable sealing solder passing the hermetic norm 1014 of the MIL-STD-883^{E}, before and after thermal shocks for all assemblies. It also proved to be more flexible than AuSn20 as it handles CTE mismatch.

In a next step some active samples should be made with lasers and photodiodes encapsulated in ceramic lid for examples. The assembly parameters could be refined and the necessity of stoppers investigated. This sealing method seems suitable for MEMS devices as the ring could be designed around the active moving part. The solder should be chosen depending on the temperature limitations, the applications and the thermal stresses.

ACKNOWLEDGMENTS

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REFERENCES

[1] C.G.M. Vreeburg and C.M. Groeneveld, "Packaging Trends for semiconductors Lasers for DWDM-applications", 49th Proceedings of the ECTC, June 1999, pp. 1-4.

[2] Y.S. Bang, J.M. Kim, Y. Kim, J.M. Kim, Y.K Kim, "Fabrication and Characterization of RF MEMS Package Based on LTCC Lid Substrate and Gold-Tin Eutectic Bonding", Solid-State Sensors, Actuators and Microsystems Conference, June 2007, pp 2115-2118.

[3] G. Elger, L. Shiv, C. Ching-Hua, A. Kilian, A. Hase, M. Hescel, J. Kuhmann, "A fluxfree soldering process for local hermetic sealing of optoelectronic subassemblies", hymite, ITG-Workshop, May 2003.

[4] C. Kopp et al., "Merging parallel optics packaging and surface mount technologies" , Proceedings of the SPIE, San Jose, Ca, January 2008, Vol. 6899, pp. 68990Y¬68990Y-8.

[5] http://www.reinhardt-microtech.ch.

[6] M. Fendler, M. Volpert, F. Marion, L. Mathieu, J.-M. Debono, P. Castelein, C. Louis, "Ultra fine pitch hybridization of large imaging detectors ", IEEE-Nuclear¬Science-Symposium conference, October 2003, Vol. 5, pp. 3518-21.

[7] M. Hutter, M. von Suchodoletz, H. Oppermann, G. Engelmann, O. Ehrmann, H. Reichl, "Electroplated AuSn Solder for Flip Chip Assembly and Hermetic Sealing",7th VLSI-PKG-WS, Nov. 2004.

[8] R.R. Chromik, D-N. Wang, A. Shugar, L. Limata, M.R. Notis, and R.P. Vinci, "Mechanical properties of intermetallic compounds in the Au-Sn system", J. Mater. Res., Aug 2005, Vol. 20, N°8, pp. 2161-2172.

[9] M. Hutter, F. Hohnke, H. Oppermann, M. Klein, G. Engelmann, "Assembly and Reliability of Flip Chip Solder Joints Using Miniaturised Au/Sn Bumps", 54th Proceedings of ECTC, June 2004, Vol. 1, pp. 49-57.

[10] S. Bonafede, A. Huffman, W. Devereux Palmer, "Layer Structure and Thickness Effects on Electroplated AuSn Solder Bump Composition", IEEE transact. On components and packaging techno, Sept. 2006, vol. 29, N°3, pp. 604-609.

[11] http://www.set-sas.fr.

[12] Gilbert Lecarpentier, Jean Stephane Mottet, Francois Marion, "Wafer Level Packaging Chip to Wafer approach using Flux Less Soldering and featuring Hermetic Seal Capability", IMAPS, 4th Annual Conference on Device Packaging, Scottsdale, Arizona, March 2008.

[13] Jane E. Jellison, « Gold-Indium Intermetallic Compounds Properties and Growth Rates", Material Control and Applications Branch, 8 November 1979, NASA report.

High Density Cu-Sn TLP Bonding for 3D Integration

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ABSTRACT

3D die stacking is a key technology for enabling 3D integration wherein two or more dies are stacked on top of each other with vertical interconnections. This result in high speed interconnects with reduced noise and crosstalk as compared to wire bonded assemblies. 3D integration may require sequential stacking of multiple dies without disturbing the previously bonded die. This can be achieved by transient liquid phase (TLP) bonding where the melting point of the intermetallic formed after the bonding is much higher than that of the solder itself. In this paper, we demonstrate the feasibility of narrow pitch TLP bonding for the Cu-Sn system in die stacking applications. Furthermore, we explore several process options for cost reduction, throughput enhancement and thermal budget minimization. More than 90% yielding devices are achieved on 40µm pitch peripheral array and 100µm pitch area array dies at 250°C using both flux and No flow UnderFill (NUF) using both die-to-die and die-to-wafer setup. Preliminary bonding results at temperature less than 200°C are also presented.

INTRODUCTION

At IMEC, along with direct Cu-Cu bonding [1], low temperature alternatives for die stacking are being explored. Transient liquid phase (TLP) bonding is a very attractive process for the realization of vertical interconnection between devices. TLP bonding is a relatively low temperature thermo-compression type bonding process that transforms solder into high melting point intermetallic (IMC) bonds [2,3] (an alternative name of solid liquid interdiffusion is sometimes used for what is fundamentally the same process) [4,5]. Such process enables repeated stacking of additional layers without remelting the bumps at lower levels of the stack. In this way, TLP bumping facilitates multi-level 3D interconnects, and hence recently drew much attention in 3D chip stacking technology [6-8].

In this paper, we demonstrate the feasibility of narrow pitch TLP bonding for the Cu-Sn system in die stacking applications. Furthermore, we explore several process options for cost reduction, throughput enhancement and thermal budget minimization. Cost reduction is achieved by reducing the number of process steps required by using no flow underfill (NUF) [8,9] during the bonding instead of flux. No underfilling is required on the samples bonded with NUF thereby eliminating the extra processing steps required during capillary underfilling process. Throughput enhancement is achieved by doing die to wafer bonding instead of die to die bonding. Further lowering of the bonding temperature may be necessary for specific applications such as DRAM memory. Cu-Sn bonding process at temperatures below 200°C has been explored for this reason.

TEST SAMPLE FABRICATION

The test samples are designed so that after the bonding the dies are connected into a daisy chain to measure the electrical yield of the bonding process. Die to die bonding and die to wafer placement is performed on a **SET FC150 flip-chip bonder** and collective bonding is performed on a wafer bonding tool or on the flip-chip bonder with a modified pickup tool. Two different sets of 200mm wafers are processed to form top die and landing die. 300nm single damascene Cu routing lines for the daisy chain connections are processed on both sets of wafers followed by a thin passivation layer on top of the Cu routing lines, which is patterned for electro-plating. The wafers are then bumped with Cu UBM on the landing substrate and Cu UBM and Sn bump on the die substrate.

For bumping the wafers, on the landing substrate Ti/Cu/Ti seed layer is sputter coated followed by lithography for bump electroplating. 5µm thick Cu is electroplated in Nexx Stratus 100 electroplater. Second lithography is performed to pattern Au bond pads for wire bonding. Finally the resist is stripped and seed layer etched to finish the processing on the landing substrate. The wafer is diced into 8x8mm dies for individual die bonding or 48x48mm 6x6 array of landing dies) for collective bonding.

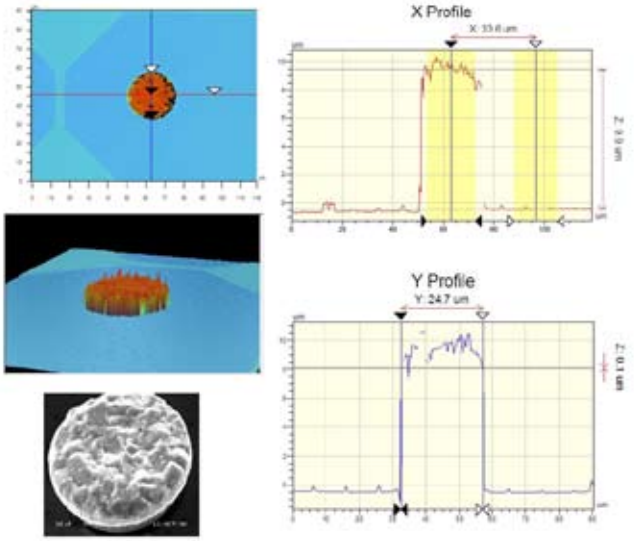


Figure 1 - Optical profilometer scan of the solder bumped die, showing the bump roughness.

On the top die substrate Ti/Cu seed layer is sputtered followed by lithography for bump electroplating. Cu and Sn were deposited as the bump stack. Finally the resist is strip-

ped and seed layer etched to finish the processing on top die substrate. The wafer is diced into 5x5mm dies.

Plated Sn is normally rougher than Cu as can be seen in the optical profilometer scan of the top die with Sn solder bump in Figure 1. Also shown in the figure is a SEM image in the bottom left. The average roughness, R_a, on the solder surface is 500nm as shown in Figure 1. The landing die with just Cu bump is relatively smoother with R_a of 200nm.

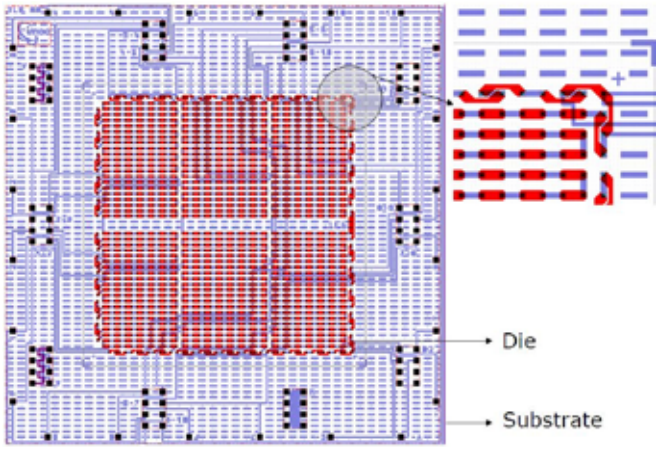


Figure 2 - Layout of the area array assembly with 100µm pitch bumps.

Figure 2 and Figure 3 show the layout of the area array assembly and peripheral assembly. Test devices with 100µm pitch area array (AA) bumps and 40µm pitch peripheral array (PA) bumps are bonded in die-to-die and die-to-wafer schemes. The area array test devices have a total of 2018 interconnects (distributed over 9 daisy chains) at 100µm pitch and the peripheral array devices have 480 interconnections (distributed over 2 daisy chains) on 40µm pitch.

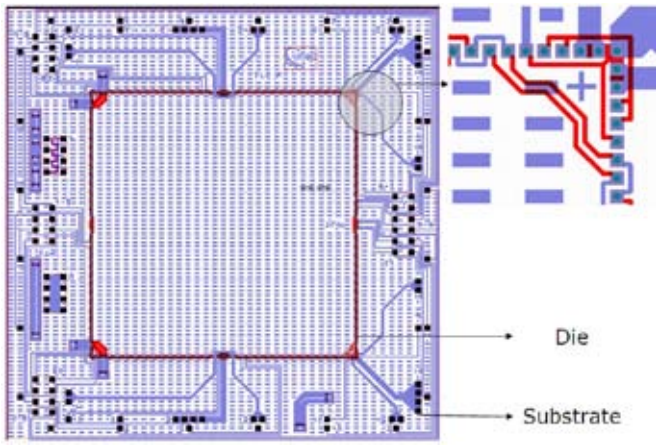


Figure 3 - Layout of the peripheral array assembly with 40µm pitch bumps.

TLP BONDING EXPERIMENTS

It is critical to include a surface cleaning agent during the TLP bonding process in order to allow a good contact between the Sn and Cu surface. TLP bonding experiments in this work are carried out in presence of two different materials, a BGA/ Flip Chip gel flux and a NUF. The flux used in this work is IF8300 from Interflux and the NUF used is FF2300 from Henkel. Besides cleaning the Sn and Cu surfaces, these materials also provide a temporary bond to hold the dies in place between pick and place and bonding in the collective bonding approach (much like the use of tacky fluxes in conventional flip chip bonding).

NUF are flux filled polymer materials that clean the bonding surface during the process and cure at the same time. There has been a limited implementation of NUFs for conventional flip chip bonding primarily due to the fact that the process window NUFs is rather narrow. This is because the flip chip relow soldering relies on a good wetting and collapse of the flip chip bump and the presence of NUF (which cures partially in the soldering process) limits this solder collapse. The NUF materials typically have a higher coefficient of thermal expansion (CTE) than their capillary counterparts and may introduce additional reliability concerns especially while bonding the die to laminate substrates.

The drawbacks that NUF's exhibit in a conventional FC assembly process are to large extent not present when one considers their application to a Si to Si application with thermo-compression bonding. In thermo-compression TLP type bonding one does not rely on the solder collapse and flux assisted wetting of the solder for bond formation. Moreover since the two die being bonded have no CTE mismatch, some of the reliability concerns may become less important.

The experimental section in this paper is divided into two sections:

A) die to die bonding,
B) die to wafer bonding.

A) DIE TO DIE BONDING:

The top and bottom substrates are inspected and cleaned prior to the bonding. During the bonding process a controlled amount of flux or NUF is dispensed on the center of the landing die using a dispenser. After dispensing the flux or NUF the top die is aligned to the landing die in the flip-chip bonder. Following this, the top chuck is moved down bring the two dies in contact while ramping up the applied force. Once the required pressure is achieved temperature is ramped up on both the arm and the chuck to allow both the arm and the chuck to heat up at the same rate and reach the final bonding temperature at the same time. Once peak temperature is reached, the force and temperature are applied following which, the top arm is lifted and the bonded assembly is cooled down. The peak temperature used for the TLP bonding is 250ºC.

The samples bonded with the flux are underfilled using non-filled capillary underfill material. On the other hand when NUF is used the polymer in NUF remains on the substrate which acts as an underfill after the bonding is finalized, hence eliminating an extra processing step of underfilling, as shown in Figure 4 and Figure 5. The bonding profile is altered for the bonding with NUF based on the NUF manufacturer's recommendations. This profile requires the flux in NUF to be activated in the flux activation zone (150°C to 170°C) and is similar to a conventional lead free FC reflow profile.

The consolidated results for the TLP bonding with flux and NUF are presented in Table 1. It is important to point out the device level and daisy chain level electrical yields. For example 30 area array dies are bonded using flux and 28 of these show a 100% electrical yield for the daisy chains with in the die. This translates to a device yield of 93%. However, in the remaining two dies only one daisy chain failed out of 9 individual daisy chains. Hence with respect to the number of functional daisy chains, from a total of 270 bonded daisy chains of 225 bumps each, 268 daisy chains are electrically functional, thus giving a yield of 99.3%.

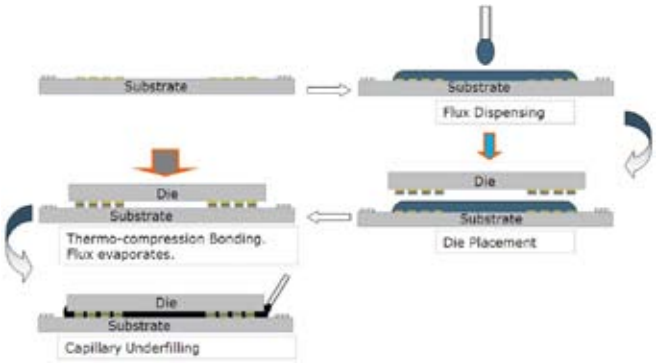


Figure 4 - Flip chip bonding using flux followed by underfilling process.

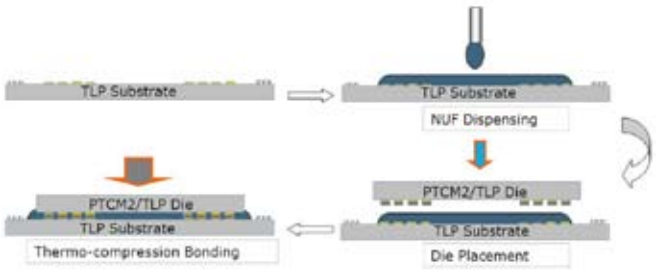
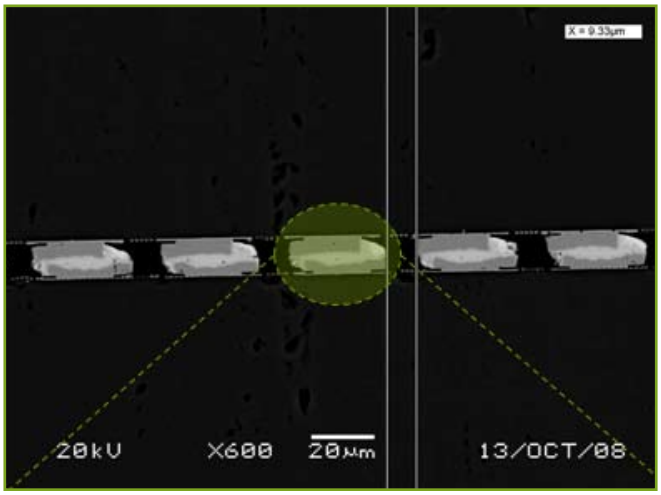


Figure 5 - Flip chip bonding using NUF.

Type of Dies	Cleaning Media	% DC level Electrical Yield	% Device Level Electrical Yield
AA	Flux	99.3	93
PA	Flux	96.7	94
AA	NUF	100	100
PA	NUF	100	100

Table 1 - Electrical daisy chain yield results for die to die bonding at 250°C.

Figure 6 shows the cross-section of a TLP bonded peripheral array test die. The zoomed out image shows the 40µm pitch array while the zoomed in image shows a single interconnect. As expected, Cu_3Sn and Cu_3Sn_5 formation is observed and almost complete transformation nof Sn into these intermetallics is observed. Good wetting of the Sn is seen on Cu and no voids are visible at the bond interface.



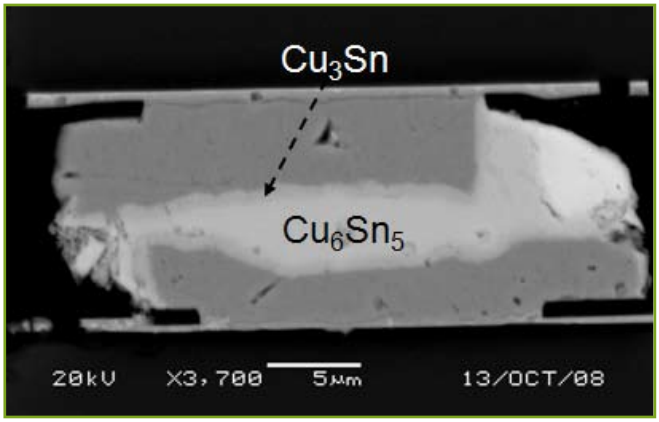


Figure 6 - SEM cross-section of the peripheral array sample.

B) DIE-TO-WAFER BONDING:

Thermocompression die to die bonding requires the entire bonding process to take place with an applied load. While the die to die bonding is useful to define the bonding process and produce tacks in smaller quantities, it is not very cost effective since the individual die bonding can take a very long time. Die to wafer stacking, may be of more interest for an increase throughput and reduced cost for 3D integration. Furthermore, it may be advantageous for the fabrication of heterogeneously integrated systems as it does not impose the any die size restrictions. The method is also compatible with the selection of known good die (KDG) prior to stacking.

The die to wafer bonding scheme relies on a relatively high speed pick, align and place sequence for individual dies. Once the entire wafer is populated, the dies can be collectively bonded. This is similar to a batch reflow process except that a load is applied on the dies during bonding, effectively making it a collective thermo-compression bonding.

In the work presented, the die to wafer assembly and collective bonding is simulated by populating arrays of landing dies/substrates. These were diced in an array of 6 x 6 / 36 devices. Assemblies were made with both the flux and NUF. In each case, flux or NUF is dispensed on all 36 dies. The top dies are aligned with the corresponding bottom die and are

placed there with certain pressure. A fully automatic program is used in the **FC150 flip-chip bonder** for pick and place operation including the alignment of the dies. The collective bonding involves a room temperature pick and place of the dies onto the landing substrate followed by collective thermo-compression bonding in a wafer bonder. The flux/NUF act as a temporary adhesive material during the transport from the pick and place operation to the collective bonding operation. After populating the landing substrate with dies the assembly is then moved to the wafer bonder. The bonded dies are then probed to obtain the electrical yield.

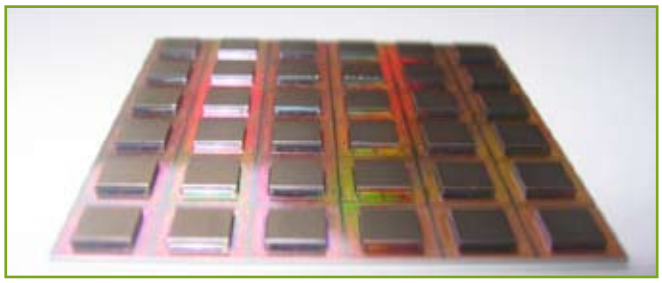


Figure 7 - Optical image of the collectively bonded samples.

Figure 7 shows the optical image of the 36 samples bonded using collective bonding method as described above. In total 58 AA dies was collectively bonded using flux with a device yield of 98%.

Due to the limited bonding area of the bumps, the total force required in the wafer bonder to obtain the bonding pressure is very low and falls below the lower force limit of the wafer bonder. This results in instabilities in the bonder control during operation and the applied pressure per bump was estimated to be ~60% higher than used for die to die bonding. Obviously, the net area to be bonded is increased, one can expect a better control on the applied force in the bonder. The demonstrations of collective bonding on the wafer subsets are therefore expected to translate well when populating and collectively bonding a full wafer.

In order to get a better force control, the peripheral array devices are collectively bonded in the flip chip bonder, since the total area to be bonded is ~25% of the AA samples. A flat bonding tool is used to pick up a blanket silicon piece of 5mmx5mm. This is done to prevent any damage to the bonding tool. The dies are populated in the flip-chip bonder as usual and the final bonding is performed on the flip-chip bonder as well. On the peripheral array devices with flux we have 29 working dies out of 32 good dies giving a device yield of 90%. Similarly for NUF collective bonding on PA devices 88% device yield is obtained. Table 2 consolidates the electrical results for the collectively bonded samples.

Type of Dies	Cleaning Media	% DC level Electrical Yield	% Device Level Electrical Yield
AA	Flux	98	98
PA	Flux	91	90
PA	NUF	88	88

Table 2 - Electrical daisy chain yield results for collective bonding at 250°C.

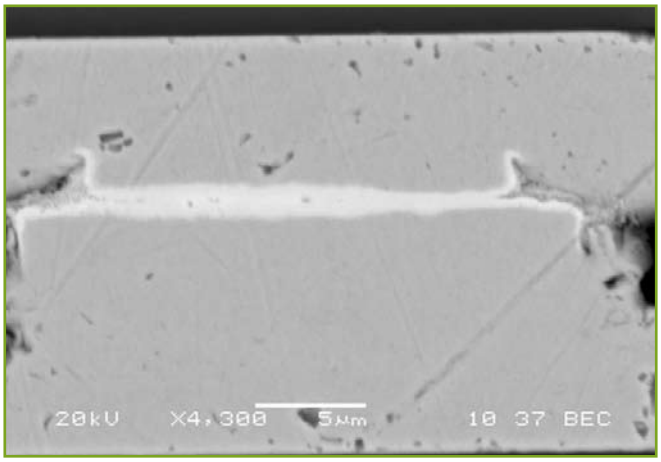


Figure 8 - Cu-Sn sample bonded at 200°C.

SUB 200°C CU-SN TLP BONDING

Certain 3D integration applications such as advanced node DRAM devices are very sensitive exposure to higher temperatures. When one considers the possible integration routes for such devices, the bonding temperature that the device is exposed to (possibly several times in case multiple number of such devices are stacked on each other) becomes a very critical parameter.

For Cu-Sn metallurgical systems, experiments have been conducted to check the feasibility of using a sub 200°C bonding process. The bonding process requires a higher bonding force than the samples bonded using a 250°C peak temperature bonding process. More than 90% electrical yield has been obtained for bonding at 200 and 150°C for samples with the AA configuration samples. A flux is used to clean the Cu landing pads during the bonding process. Figure 8 shows a cross section of a sample bonded at 200°C. A complete transformation of the Sn into Cu-Sn IMCs is observed. Further optimization is ongoing to estimate the limits of the Cu-Sn solid state bonding.

DISCUSSION

A high electrical yield is observed on all of the experiments conducted for TLP bonding. Both D2D and D2W bonding scheme gives very consistent results. The D2D yield is slightly higher than the D2W. It is noticed that even during the temperature ramp up the Sn is transformed into the IMC and hence the hold time at the peak temperature can be reduced or effectively removed. Further characterization of bonding process is required to reduce the bonding process time.

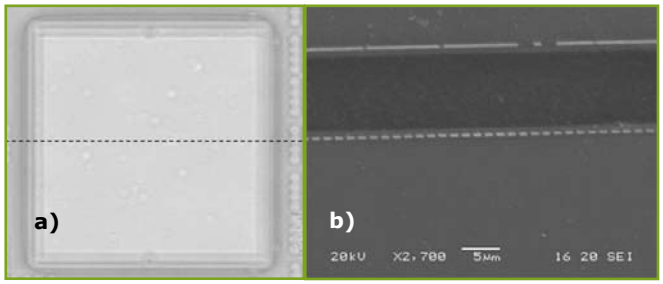


Figure 9 - (a) SAM image of the sample bonded with NUF, (b) Cross section SEM image of the same sample showing void free underfilling.

Figure 9 shows the SAM images of a sample bonded using NUF and the corresponding cross section image. As seen from this figure NUF gives a very uniform filling even with such small bump heights. Small voids are observed n the underfill but the levels are well within the standard underfill acceptance criterion.

The capillary underfill results indicate that further optimization is necessary. Improper filling of the gap between the two dies is attributed to excessive flux deposition prior to bonding. The flux is expected to evaporate during the bonding process leaving behind very low levels of residue. Since the flux is dispensed in the center of the die and spread out during the top die placement, the amount of flux present is much greater than the actual amount needed. Conventional approach of flux dipping the bumps prior to placement is not feasible for TLP bumps since the bump height is less than 10μm. Therefore relatively larger amount of flux residues are observed to be left behind after the bonding. The impact of these flux residues is that the capillary underfilling is difficult to optimize. Alternative means of depositing adequate amounts of flux are currently being explored. It is expected that this will allow easier integration of the capillary underfill process.

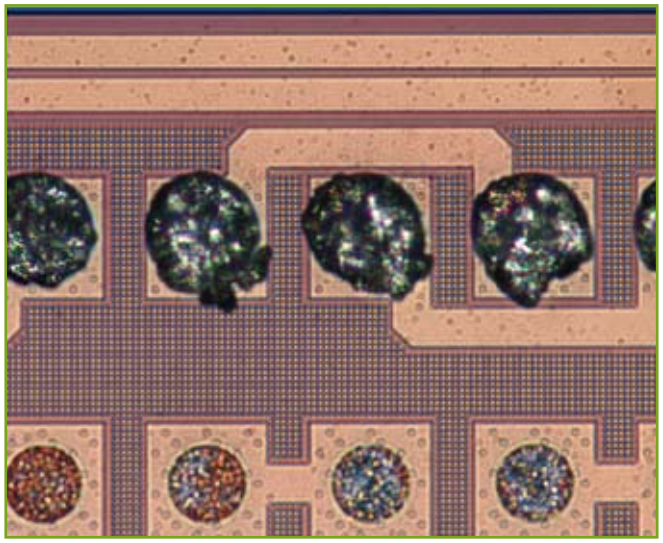


Figure 10 - Sheared die showing the typical mode of failure.

Shear tests are performed on number of samples using XYZtec Condor multifunctional bond tester to check for the bond integrity and observe the failure mode. A 100N force sensor is used in these measurements with a shear height of 20μm and shear speed of 10μm/sec. The average shear force measured on the TLP samples bonded using flux is around 13 ± 2 KgF for area array samples and 4 ± 1 Kgf for peripheral array samples, giving a average shear stress of 122 ± 10 MPa/bump for AA and 167 ± 15 MPa/bump for PA samples. The shear test results are consistent with the trends observed in the electrical yield measurements. The predominant failure mode is fracture through the bonded TLP bump and no UBM delamination is observed as shown in Figure 10 and Figure 11.

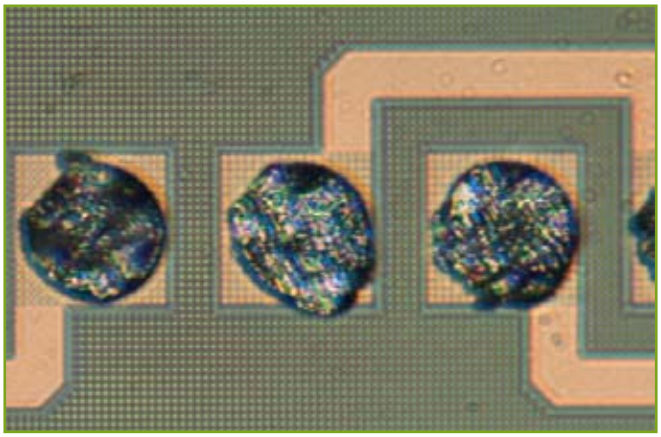


Figure 11 - Sheared substrate showing the typical mode of failure.

CONCLUSIONS

In this work, a TLP bonding process for 40μm pitch peripheral array and 100μm pitch area array with greater than 90% electrical yield has been demonstrated. The TLP bonding process has been evaluated with both flux and a no flow underfill. The individual die pick and place with collective thermo-compression bonding approach has been successfully demonstrated giving yields comparable to the die to die TLP bonding for both AA and PA samples with flux and NUF. A solid state Cu-Sn bonding process has also been demonstrated with >90% electrical yield. NUF samples show a very uniform underfilling of the die despite the low standoff height. Shear test of bonded samples indicates that the predominant failure mode is fracture through the intermetallic bump. Aspects of TLP bonding for 3D integration that require further optimization include the flux deposition methods as well as solid state bonding for Cu-Sn.

ACKNOWLEDGMENTS

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REFERENCES

[1] A. Jourdain, S. Stoukatch, P. De Moor, W. Ruythooren; «Simultaneous Cu-Cu and Compliant Dielectric Bonding for 3D Stacking of ICs», International Interconnect Technology Conference, IEEE 2007, 4-6 June 2007 Page(s): 207 - 209.

[2] W. Zhang, W. Ruythooren, "Study of the Au/In reaction for Transient liquid-phase bonding and 3D chip stacking," Journal of Electronic Material, vol. 37, no. 8, 2008, pp. 1095-1101.

[3] N. S. Bosco, and W. F. Zok, "Critical interlayer thickness for transient liquid phase bonding in the Cu-Sn system," Acta Materialia, vol. 52, issue 10, 2004, pp. 2965-2972.

[4] J. W. Roman, and T. W. Eagar, "Low stress die attach by low temperature transient liquid plase bonding," Proc. of the International Society for Hybrid Microelectronics (ISHM), 1992, pp. 1-6.

[5] L. Bernstein, "Semiconductor joining by the solid-liquid¬interdiffusion (SLID) Process," J. Electrochem. Soc., vol.113, no. 12, 1966, pp. 1282-1288.

[6] S. Wakiyama, H. Ozaki, Y. Nabe, et al., "Novel low temperature interconnection technology for multichip LSI (MCL)," Proc. of ECTC 2007, pp. 610- 615.

[7] K. Sakuma, P.S. Andry, B. Dang, et al., "3D stacking technology with low volume lead free interconnections," Proc. of ECTC 2007, pp. 627-632.

[8] A. Munding, A. Kaiser, P. Benkart, E. Kohn, A. Heittmann, and U. Ramacher, "Scaling aspects of microjoints for 3D chip interconnects," Proc. of IEEE 2006, pp. 262-265.

[9] C. P. Wong, S. H. Shi and G. Jefferson, "High performance low cost underfills for flip-chip applications," Proc. of ECTC 1998, vol. 21, no. 3, pp. 450-458.

[10] P. S. Teo, S. P. S. Lim, T. C. Shai and M. K. Iyer, "Application of no flow underfill for a reliable high performance flip chip flex BGA," Proc. of ECTC 2002, pp. 425-431.

Three Dimensional Interconnects with High Aspect Ratio TSVs and Fine Pitch Solder Microbumps

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ABSTRACT

High density three dimensional (3D) interconnects formed by high aspect ratio through silicon vias (TSVs) and fine pitch solder microbumps are presented in this paper. The aspect ratio of the TSV is larger than 10 and filled with Cu without voids; there are electrical nickel and immersion gold (ENIG) pads on top of the TSV as under bump metallurgy (UBM) layer. On the Si chip, Cu/Sn solder microbumps with 16μm in diameter and 25μm in pitch are fabricated. After singulating the Si chip and the Si carrier, they are joined together and the interconnection is formed between them through the solder micro bumps and the TSV.

INTRODUCTION

To meet the miniaturization trend and to reduce power consumption for next generation information devices, three-dimensional (3D) chip stacking technology is studied extensively. In this technology, short and high density interconnections between logic chips and high-capacity memory chips are required. TSVs can provide the shortest and most effective interconnections between the chips or between the chip and the substrate. Besides, solder microbumps are needed to assemble the logic chip and the memory chip together and also provide interconnections between chips [1-6].

Therefore, integration of solder micro bumps and TSVs is one of the critical steps for 3D chip stacking.

In this paper, fine pitch solder microbumps and high aspect ratio TSVs filled with copper are fabricated and integrated together to form 3D interconnects for integration of the Si chip and the Si carrier. First, designs of the packaging structure are discussed, and then the fabrication and assembly process are presented. The TSVs are constructed in the Si carrier wafer (8" wafer) and etched with BOSCH process in a deep reactive ion etch (DRIE) machine. A bottom-up Cu plating process is developed to fill the high aspect ratio TSVs. After Cu plating and removal of the over plated Cu, the backside of the TSV wafer is passivated and patterned to expose the Cu pad. Then under bump metallurgy (UBM) pads are fabricated on the exposed TSVs. On the Si chip, the solder microbumps with 25μm pitch are made up of plated Cu and Sn with total thickness of 10μm. Assembly of the Si chip and carrier is conducted with **FC150 flip chip bonder** and the optimized bonding conditions are obtained. Good joining with 12.1 MPa shear strength has been achieved.

DESIGN OF PACKAGING STRUCTURE

Figure 1 shows a schematic drawing of 3D chip stacking for a Si chip and a Si carrier. The solder microbumps are fabricated on the Si chip and the UBM pads are fabricated on the Si carrier. The designed pitch for both solder microbumps and the UBM pads are 25 μm and TSVs in the Si carrier are as interconnection. After assembly of the Si chip and the Si carrier, the whole assembly is joined onto a bismaleimide triazine (BT) substrate with redistribution layer and solder joints. The main focuses of this work is to demonstrate fabrication processes of TSV with Cu filling and also the assembly process.

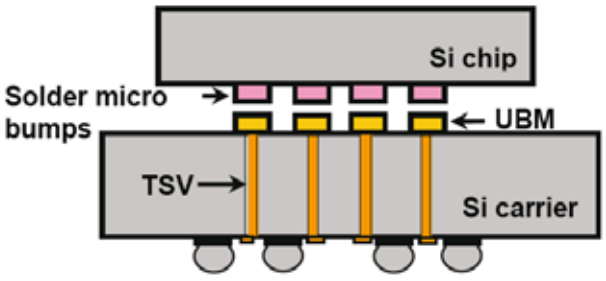

Figure 1 - Schematic drawing of 3D stacking of the Si chip/Si carrier with TSV (not in scale).

DESIGN OF TSV AND UBM PADS ON SI CARRIER

Figure 3 shows a cross-sectional view of TSV and UBM pad. The TSV has diameter of 15μm and pitch of 25μm. The aspect ratio of TSV is greater than 10. Above the TSV is UBM pad. In this work, ENIG is used as the UBM layer. For very fine pitch UBM pads, normal UBM metal films, such as TiCuNiAu or AlNiVCu etc, are difficult to pattern with traditional photolithography and wet etching process. Because the under cut caused

by the wet etching process can damage the small UBM pads. ENIG formation does not require any high vacuum or photolithography equipments to form the metal stack on top of the bond pads, therefore it is a simple and low cost solution for high density and high pin-count build-up IC packages [7].

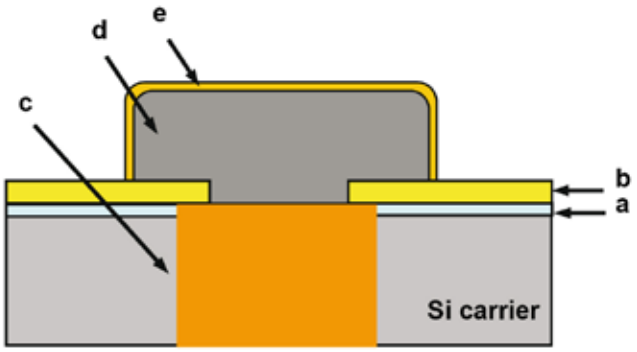

Figure 2 - Cross-section of UBM pad (ENIG) on the Si carrier (not in scale):

a. Passivation layer 1,
b. Passivation layer 2,
c. TSV,
d. Electroless plated Ni,
e. Immersion Au.

DESIGN OF SOLDER MICROBUMPS ON SI CHIP

Figure 4 shows a cross-sectional view of the solder micro bump structure. The CuSn solder microbumps were fabricated on the Si chip at wafer level by electroplating method. The total thickness of the Cu and Sn are 10µm.

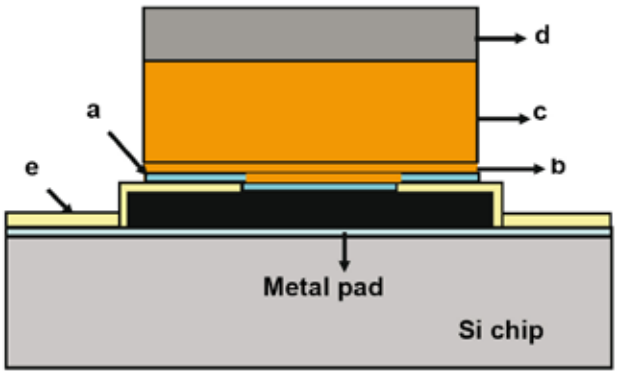

Figure 3 - Cross-section of solder microbump on the Si chip (not in scale):

a. Ti adhesion layer,
b. Cu seed layer,
c. plated Cu,
d. plated Sn,
e. passivation layer.

In order to achieve reliable joining, Sn solder must be thick enough so that after reflow, there is still pure left for joining. It can be seen in the later results, after 1 time reflow, the formed Cu_6Sn_5 intermetalic compound (IMC) thickness is about 1.5µm. Therefore, it is better to have the Sn layer thicker than 1.5µm.

However, if Sn layer is too thick, sidewall wetting will happen, which results in dewetting issue because of shortage of Sn solder on top of the Cu pillar, or leads to bridging between the adjacent joints due to the ultra fine pitch. Either of these can damage the assembly. According to the reference of [8], in order to avoid sidewall wetting, the wetting angle between Sn and Cu should less than 90° and the height of the Sn cap layer should thinner than one fourth of the diameter of the microbump. Especially if one used thermo-compression for micro bump assembly, the bonding force applied will encourage the sidewall wetting if there are too much solder on the top of Cu. In this work, the Sn layer thickness is designed between 1.5 to 4µm.

FABRICATION PROCESS

A) FABRICATION OF TSV

The high aspect ratio TSV's are etched in inductive coupled plasma (ICP) based deep reactive ion etching system from Surface Technology System (STS) by using BOSCH process. Figure 4 shows fabrication process flow.

As shown in Fig. 4, first, a layer of SiO_2 is deposited on the wafer as hard mask (Fig. 4(a)). Then thin layer of photoresist is spin coated and patterned (Fig. 4(b)). After SiO_2 etch and photoresist stripping (Fig. 4(c)), TSVs are etched to the desired depht and SiO_2 hard mask is removed after etching (Fig. 4(d)). After that, a layer of plasma-enhanced tetraethylorthosilicate (PETEOS) is deposited on the front side for sidewall passivation (Fig. 4(e)). Then the wafer is thinned down to expose the backside of the TSV (Fig. 4(f)). In order to fully passivate the side wall of the TSV, another layer of SiO_2 is deposited on the back side of the wafer (Fig. 4(g)) and then a layer of Ti/Cu is sputtered at the back side of the wafer as seed layer (Fig. 4(h)).

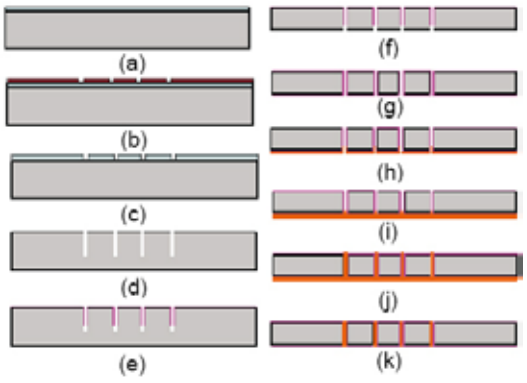

Figure 4 - Process flow for TSV fabrication and Cu filling.

Wafer level plating is done to seal the TSV from the back side of Fabrication of UBM pads on Si carrier the wafer (Fig. 4(i)). After that, bottom up plating is carried out till all the TSV is filled (Fig. 4(j)). After TSV plating, the Cu over burden on the top of the wafer and the Cu on the back side of the wafer are all removed by chemical mechanical polish (CMP) (Fig. 4(k)).

In this process, because the diameter of via is only 15um, therefore it is easier to seal the vias from the bottom (Fig. 4(j)) with high plating current (1 ampere in this work). After

sealing the vias, the bottom-up plating can be done directly without support wafer, as did in reference [9]. Therefore, after bottom-up plating, it is not necessary to remove the support wafer which is difficult and can lead to wafer break easily.

B) FABRICATION OF UBM PADS ON SI CARRIER

After wafer thinning and Cu CMP, the UBM pad can be fabricated on top of TSV. Fig. 6 shows the process flow of UBM pad fabrication. First, a layer of dielectric is deposited on top of the wafer (Fig. 5(a)).

Then a thin layer of photoresist is spin coated and patterned (Fig. 5(b)).

After that, the dielectric layer is etched to expose the TSV and the photoresist is stripped (Fig. 5(c)).

At last, electroless Ni-P plating and Electroless Au plating is done to form UBM pad Fig. 5(d)).

Figure 5 - Process flow for ENIG plating on top of TSV.

C) FABRICATION OF SOLDER MICROBUMPS ON SI CHIP

Figure 6 shows the process flow for fabrication of Cu/.Sn solder micro bump on the Si chip. First, layers of SiO2 and Al film are deposited on the wafer (Fig. 6(a)). Then a layer of 2µm thick photoresist is spin coated and patterned (Fig. 6(b)). Then Al is etched to form the metal pad and the photoresist is removed (Fig. 6(c)).

Another passivation layer is deposited and patterned (Fig. 6(d), (e) and (f)). Then Ti/Cu of adhesion layer and seed layer is sputtered (Fig. 6(g)). Then a thick layer of photoresist is coated and patterned as plating mold (Fig. 6(h)). Cu/Sn is then plated sequentially (Fig. 6(i)) and the photoresist is stripped and the Ti/Cu adhesion/seed layers are etched back.

After plating, a reflow was performed to reshape the solder micro bumps in order to achieve uniform bump heights.

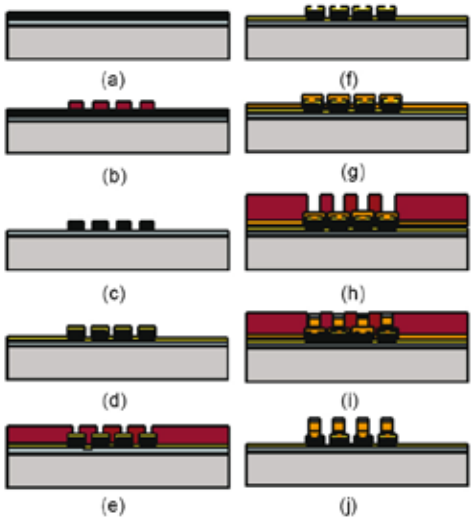

Figure 6 - Process flow for Cu/Sn solder micro bump fabrication on Si chip.

RESULTS AND DISCUSSION

A) TSV DRIE RESULTS

During the DRIE process, many variables can affect the profile of the high aspect ratio vias, such as SF_6/C_4F_8 flow rate, etching/passivation active time, electrode power and automatic pressure valve (APC) orientation [10, 11]. Among of these parameters, it is found that the etching/passivation cycling time is the most critical one.

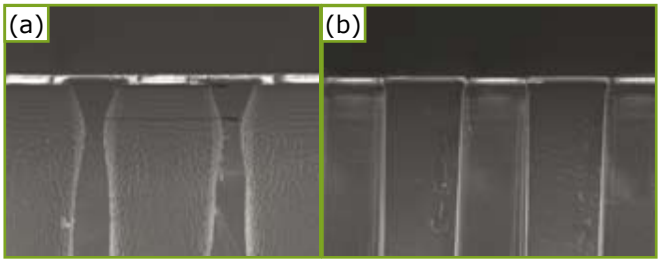

Figure 7 - Effects of time ratio between etch cycle and passivation cycle on under cut and bow shape of TSV:
(a) etch time is 80% longer than the passivation time,
(b) etch time is same as passivation time.

Fig. 7 shows two cross-sections that etched at different conditions. It is found that when the etch cycle time is 80% longer than that the passivation cycle time, the under cut and the bow shape are larger than 2µm, as shown in Fig. 7(a). In Fig. 7(b), the side wall is straight when both the etch time and the passivation time are same.

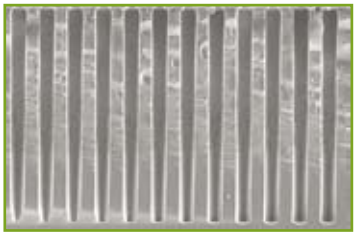

Figure 8: Cross-section of the etched TSV.

Figure 8 shows cross-section of the etched TSV when the etch/passivation time is same.

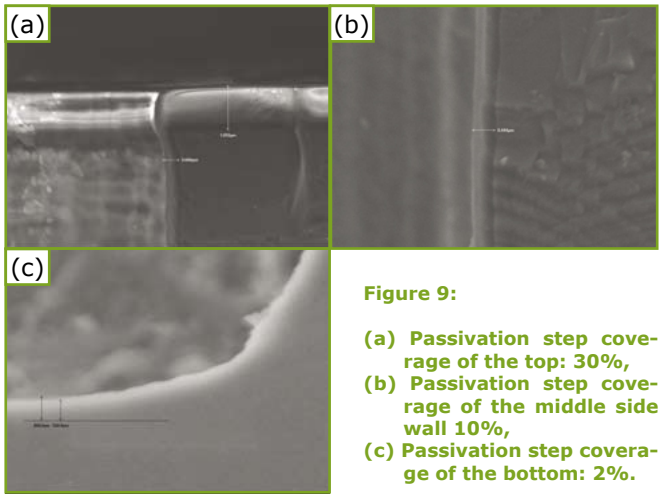

Figure 9:

(a) Passivation step coverage of the top: 30%,
(b) Passivation step coverage of the middle side wall 10%,
(c) Passivation step coverage of the bottom: 2%.

B) SIDEWALL PASSIVATION RESULTS

After TSV formation, PETEOS is deposited from the front side of the wafer to form an insulation layer. Fig. 9 shows the passivation results. It is found that the step coverage of the sidewall at the top and the middle of the TSV is only about 30% and 10%, respectively. On the sidewall at the bottom of the TSV, there is a thin insulation layer.

C) BOTTOM UP PLATING RESULTS

Fig.11 shows top view of Cu filling results It is seen that there is few voids still on top of the TSVs.

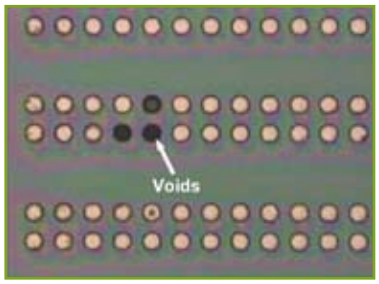

Figure 11:
Cu filling results with few voids on top of TSVs.

In order to completely remove the voids, the wafer was further thinned down for another 50µm, as shown in Fig. 12 that this is no any void and all the TSVs are fully filled with Cu.

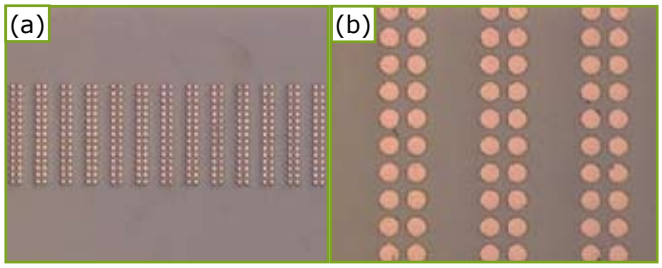

Figure 12 - After wafer thinned down for another 50µm, all the voids in TSV are removed.

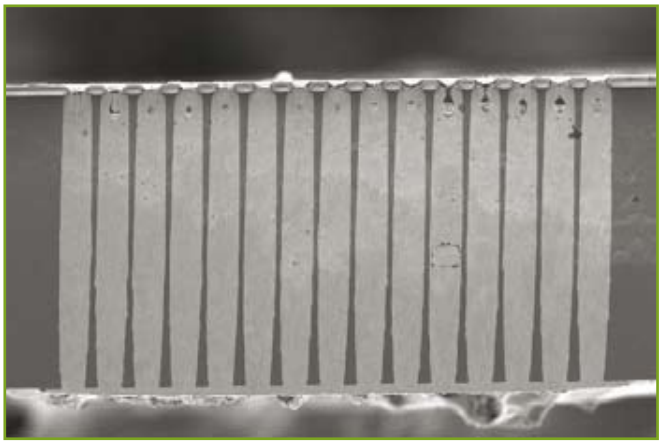

Figure 13 - Cross-section of TSVs after Cu plating.

Fig.13 shows cross-section of TSV after Cu filling. It seen that all the TSVs are fully filled with Cu without any voids in side.

D) ENIG PLATING RESULTS

Fig. 14 shows top view of ENIG plating on top of the TSV. After plating, the diameter of the ENIG pads is about 4µm larger than the diameter of TSV because of radial Ni growth on the passivation layer [12].

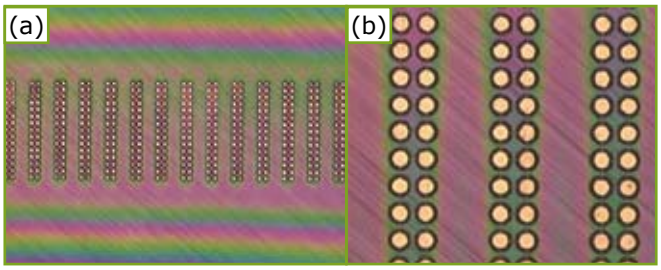

Figure 14 - SEM pictures of UBM layer of ENIG on top of TSV.

E) CuSn SOLDER BUMP FABRICATION RESULTS

Fig.15 shows Scanning Electron Microscope (SEM) photos of the fabricated Cu/Sn micro bumps and Al pad, and Fig.16 shows Focus Ion Beam (FIB) pictures of solder bumps. After plating, a reflow was performed to reshape the micro-bumps and uniform bump heights were obtained, as show in Fig.16. The reflow temperature is 265°C. Variation of bump height within a die is less than 5%. During reflow, flux is used and after reflow, the wafer is cleaned in de-ionized (DI) water to remove the flux residues.

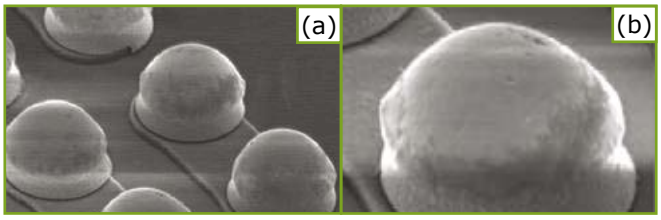

Figure 15 - SEM photos of Cu/Sn solder microbumps after reflow on the Si chip.

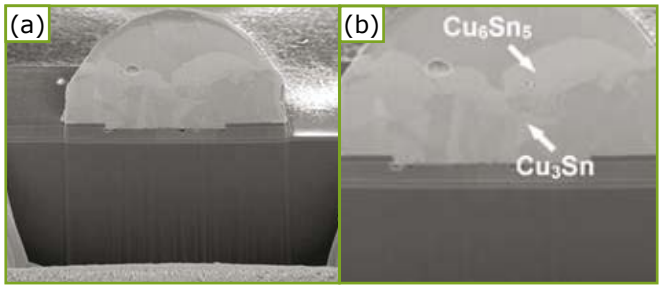

Figure 16 - FIB pictures of Cu/Sn solder microbumps on the Si chip.

F) ASSEMBLY RESULTS

After fabrication of the CuSn solder microbumps on the Si chip and the ENIG UBM pads on top of the TSV on the Si carrier, the Si chip was joined to the Si carrier using **FC150 flip chip bonder**. The assembly process is a non-flux process because after joining, the gap between the Si chip and the Si carrier is only about 10µm. Therefore if flux is used, it is very difficult to clean it and then after underfill process, a lot of voids are formed inside the gaps.

Figure 17 shows the cross-section of the two chips joined at selected bonding conditions. It can be seen that successful joining is achieved. Shear test is performed to evaluate the joint strength of the assembly. The measurements are carried out by a commercially available shear tester (DAGE-SERIES-4000-T, Dage Precision Industries Ltd, Aylesbury, UK). The force applied to the assemblies provides shear in a direction parallel to the surface of the test vehicle by the shear probe. The shear speed for this evaluation is 100µm/s and the height of the shear probe is 400 µm. The average shear strength of the chips joined at this bonding condition is larger than 10 MPa.

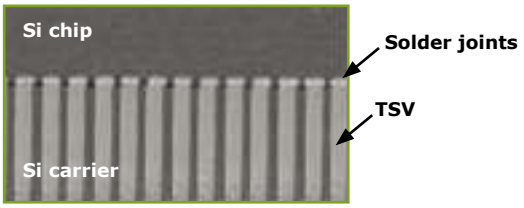

Figure 17 - Cross-section of the chips joined together.

CONCLUSIONS

The development of ultra fine pitch interconnects formed by solder micro bump and high aspect ratio TSV is reported in this paper. Some important results are summarized in the followings:

1. Solder microbumps with 25µm in pitch and 15µm in pad diameter have been developed successfully. The ultra fine pitch and high density bump array can be used for chip stacking.

2. TSVs with aspect ratio larger than 10 have been fabricated in the Si carrier wafer with DRIE method. During DRIE, it is found that when the etching cycle time is 80% longer than the passivation cycle time, the undercut is larger than 2µm and apparent bow shape appears.

3. Sidewall passivation of TSV can be achieved by deposition of passivation dielectric from both side of the wafer.

4. After Cu platting, there are few voids exist on top of the TSV, which can be removed by further thinning wafer for another 50µm. The Cu filling process still need to be optimized.

5. At optimized bonding conditions, good joining with shear strength larger than 10 MPa can be achieved between the Cu/Sn solder micro bumps and the ENIG pads on top of the TSVs.

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REFERENCES

1. Hu G., Kalyanam H., Krishnamoorthy and Polka L., "Package Technology to Address the Memory Bandwidth Challenge for Tera-scale Computing," Intel Technology Journal, Vol. 11, No. 3 (2007), pp. 197-206.

2. Knickerbocker, J. U. et al, "Development of next-gereration system-on-acage (SOP) technology based on silicon carriers with fine-pitch interconnection," IBM J. Res. Dev. Vol. 49, No. 4/5 (2005), pp. 725-754.

3. Tomita, Y., Morifuji, T., Ando, T., Tago, M., Kajiwara, R., Nemoto, Y., Fujii, T., Kitayama, Y. and Takahashi, K, "Advanced packaging technologies on 3D stacked LSI utilizing the micro interconnections and the layered microthin encapsulation," 51st Electronic Components and Technology Conf, 2001, pp. 353-360.

4. Takahashi, K., Umemoto, M., Tanaka, N., Tanida, K., Nemoto, Y., Tomita, Y., Tage, M., and Bonkohara, M., "Ultra-high-density interconnection technology of three-dimensional packaging," Microelectronics Reliability, Vol. 43 (2003), pp. 1267-1279.

5. S. L. Wright, R. Polastre, H. Gan, L. P. Buchwalter, R. Horton, P. S. Andry, E. Sprogis, C. Patel, C. Tsang, J. Knickerbocker, J. R. Lloyd, A. Sharma and M. S. Sti-Jayantha, "Characterization of Micro-bump C4 interconnects for Si-Carrier SOP applications," 55st Electronic Components and Technology Conf, 2006, pp. 633-640.

6. Gan, H., S. L. Wright, R. Polastre, L. P. Buchwalter, R. Horton, P. S. Andry, C. Patel, C. Tsang, J. Knickerbocker, E. Sprogis, Pavlova, A., Kang, S. K. and Lee, K. W., "Ph-free micro joints (50µm pitch) for the next generation micro-systems: the fabrication, assembly and characterization," 55st Electronic Components and Technology Conf, 2006, pp. 1210-1215.

7. Yokomine K., Shimizu N., Miyamoto Y., Iwata Y., Love D. and Newman K., "Development of electroless Ni/Au plated build-up filp chip package with highly reliable solder joints," 51st Electronic Components and Technology Conf, 2001, pp. 1384-1392.

8. D. Q. Yu, H. Oppermann, J. Kleff, M. Hutter, Stability of AuSn Eutectic Solder Cap on Au Socket during Reflow, Journal of Materials Science: Materials in Electronics, 10.1007/s10854-008-9606-4.

9. C.S.Premachandran, Rangnathan N, S.Mohanraj, Chong Ser Choong, Mahadevan K Iyer, "A Vertical Wafer Level Packaging Using Through Hole Filled Via Interconnect by Lift Off Polymer Method for MEMS and 3D Stacking Applications," 55st Electronic Components and Technology Conf, 2005, pp. 1094-1098.

10. Ayon A. A. et al, "Characterization of time multiplexed inductively coupled plasma etcher," J. Electrochem. Soc., Vol. 146, 1999 pp. 339-349.

11. Chen K. S., Ayon A. A., Zhang X and Spearing S. M., "Effect of process parameters on the surface morphology and mechanical performance of silicon surfaces after deep reactive ion etching (DRIE)," J. Microelectromech. Syst., Vol11, 2002 pp. 264-275.

12. Toshihiro I., Masaki W., Shinji B., Yasumichi H., Siori I., Yoshinori Y. and Michitaka K., "Development of 30 micron pitch bump interconnections for COC-FCBGA," 56st Electronic Components and Technology Conf, 2006, pp. 1216-1222.

High Density Cu-Cu Interconnect Bonding for 3-D Integration

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ABSTRACT

The demand for more complex and multifunctional microsystems with enhanced performance characteristics is driving the electronics industry toward the use of best-of-breed materials and device technologies. Three-dimensional (3-D) integration enables building such high performance microsystems through bonding and interconnection of individually optimized device layers. Bonding of device layers can be achieved through polymer bonding or metal metal interconnect bonding with a number of metal-metal systems (e.g. Cu-Cu, Cu/Sn-Cu, etc.) currently under development. RTI has been investigating and characterizing Cu-Cu and Cu/Sn-Cu interconnect processes for high density area array applications, demonstrating bonding between pads less than 15 microns in diameter for large area array configurations. Cu and Cu/Sn bump fabrication processes were developed that provide well-controlled surface topography necessary for the formation of low resistance, high yielding, and reliable interconnects.

In this paper, the effects of Cu interconnect bonding parameters (pressure and temperature) and thermal reliability testing (thermal cycling and aging) on electrical connectivity and mechanical strength are presented and compared to Cu/Sn-Cu interconnect bonding with an eye toward small pitch scaling and ease of assembly. The conditions for producing Cu-Cu bond strengths > 110 MPa and electrical connectivity as high as 99.999% are described.

INTRODUCTION

Of the bonding techniques available for creating 3D integrated devices, metal-metal bonding appears to be the most compatible with die-to-die and die-to-wafer configurations for facilitating processing of known-good-die (the preferred route for integrating chips from low-yielding IC processes) and integrating chips of heterogeneous materials [1, 2]. Thermocompression bonding between arrays of Cu bumps (Cu-Cu bonding) and solid-liquid diffusion bonding between arrays of Cu and Cu/Sn bumps (Cu/Sn-Cu bonding) have been investigated for vertical integration of two or more devices because the rigid nature of these non-collapsible bump structures allows for very fine pitch interconnections to be made with low risk of bridging between neighboring interconnects. In addition, the metal-metal bonds are mechanically stable during subsequent thermal processes, which allows for the stacking of multiple layers of devices without disturbing the interconnections formed in previous bonding cycles.

When bonding two chips in a face-to-face configuration (the simplest case of 3D integration), the choice of the bonding metallurgy is likely to be dictated by the device surface topography and the temperature limitations of the devices. As was demonstrated in previous work [3], the bonding yield of rigid bump structures is critically dependent on a number of factors, including the intrinsic flatness of the device, the degree of planarity with which the devices can be aligned to one another, and the bump height uniformity. The use of Cu/Sn bumps can provide compliance for the bonding process, allowing compensation for small height variations arising from these factors and resulting in a high bonding yield. The lower sensitivity of the Cu/Sn-Cu bonding process to the surface topography and/or flatness is due to the bonding mechanism in which Sn is heated above its melting temperature (232°C) and wets the Cu metal pad on the second chip, leading to bond formation through solid-liquid diffusion [4, 5]. Since the Cu/Sn-Cu bonding process is executed at temperatures below 300°C, Cu/Sn-Cu bonding consumes less of the thermal budget of the ICs and subjects the bonded structures to lower thermal stresses than Cu-Cu thermocompression bonding.

However, there are distinct advantages to Cu-Cu bonding. The Cu-Cu bond contains only Cu (no intermetallic phases) and therefore should be mechanically stronger than a Cu/Sn-Cu bond which contains Cu_6Sn_5 and Cu_3Sn intermetallic phases. The higher mechanical strength of Cu-Cu bonds could be particularly important for the integration of heterogeneous materials from a CTE mismatch and thermomechanical stress point of view. Cu-Cu bonding may also be preferred for ICs with Cu top metal structures because less back-end-of-line processing is required for the Cu terminated ICs. Regardless of the IC top metal material, Cu-Cu bonding requires less pre-bond preparation of the Cu bond pads/bumps (i.e., no flux or plasma pre-treatment) than that required for Cu/Sn bumps in Cu/Sn-Cu bonding [6].

Control of the device surface topography is also desirable in order to achieve a high yielding bonding process for both metal-metal bonding systems. Ideally, devices would be fabricated with the final inorganic passivation layer (typically Si_3N_4 and/or SiO_2) planarized by a chemical-mechanical polish (CMP) process, thus providing a flat surface on which to fabricate the bump interconnects. This is not always the case, however, and it is common for devices to have surface topographies that vary by 1-2 microns, which is enough to significantly impact the bonding yield. Therefore, a process that can both create a flat surface to form the bump interconnects on and be extended to most devices is also needed.

In previously reported work, Swinnen et al demonstrated the feasibility of vertically stacking die by Cu-Cu interconnect bonding performed at 300°C [7]. Huebner et al reported si-

milar results for face-to-face Cu/Sn-Cu bonding of small arrays at temperatures < 300°C performed with the aid of a fixing agent (wax) during chip stacking [5]. In this study, we report on the fabrication and bonding of large area array test devices with Cu-Cu bonding processes. Bonding experiments were performed without the use of resins or fixing agents. The bond strengths and bond yield, as derived from die shear force measurements, post die shear inspections and electrical measurements, are presented. Cross sectional analysis of bonded samples was done to investigate the bond-line formation between bump structures. The thermal stability of the bonds formed with these structures was studied by subjecting bonded test samples to multiple temperature/pressure cycles, simulating multiple bonding cycles as would be encountered in the stacking assembly of a 3D module. Isothermal aging experiments were also performed to determine the long term stability of the bond interfaces; the aged samples were characterized through electrical measurements and die shear testing. Key techniques for uniform area array bonding are also discussed.

EXPERIMENT

The area array test vehicle used in these experiments was a 200 mm wafer with two different daisy chain patterns. The pad layout was based on a pixilated readout IC designed by Fermi National Accelerator Laboratory, used in high energy physics detector applications. While the minimum I/O pitch on the device was 50 µm, the microbump structures were designed to ultimately be compatible with 20 µm I/O pitch. In addition, while the original I/O layout was a sparsely populated area array, microbumps were added to the test vehicle to create a full area array pattern with uniform 50 µm pitch in the horizontal and vertical directions. The full array was 176 x 128 (22,528 total bumps) with a chip size approximately 8 mm x 8 mm.

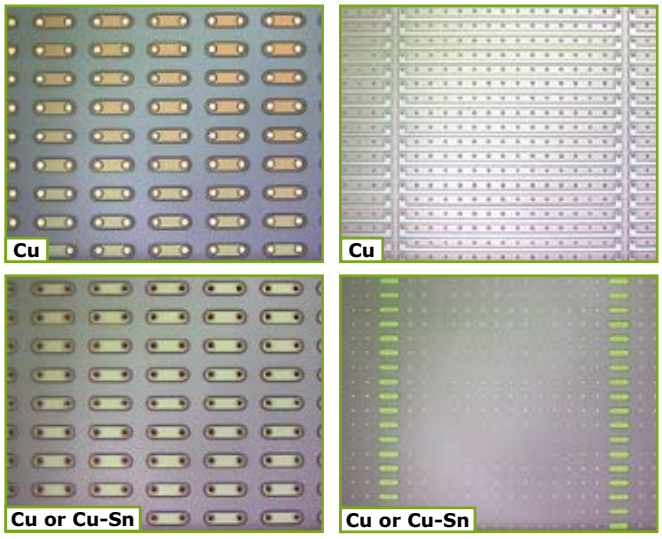

Figure 1 - Optical micrographs of full and device array daisy chain test structure layouts.

Details regarding test chip fabrication were previously reported [6]. It is important to note that two patterns ('device array' and 'full array') were designed to form daisy chain structures for electrically probing assemblies after bonding.

As seen in Figure 1, the device array layout connects every 8th pair of adjacent bumps in a row to create a daisy chain of 22 microbumps. This pattern replicated the electrical connections that would exist on the functional CMOS device with the rest of the microbumps serving as mechanical support only. The full array layout connects all 176 microbumps in each row. It should also be noted that the device array layout produces topography differences across the die requiring planarization of the oxide passivation over the daisy chain metal to provide a common, flat plane on which to fabricate the bump arrays.

Two different plating templates were also designed to provide bumps of different sizes. One plating template formed bumps with 7 µm base diameters over the entire test vehicle; the other template had a mixture of bump arrays with 11 and 15 µm base diameters. The larger diameter bumps allow for some compensation for misalignment during bonding of assemblies.

Once the microbump fabrication process was completed, wafers were diced to singulate the test devices and mating parts were bonded via thermocompression bonding with the parts held together under heat and pressure in order to form the bond interface. Sample bonding was performed in a **SET FC150 automated precision bonder**. Immediately prior to bonding, the Cu bumped chips were chemically cleaned in a weak sulfuric acid solution to remove Cu oxides that might inhibit the bonding process.

Preliminary setup steps were required prior to the bonding of parts, including calibration of the **FC150** and the installation and conditioning of a compliant interposer layer. This compliant layer is placed between the rigid bonding tool and the test chip, helping to distribute force uniformly across the bump array during bonding and to compensate for small setup errors in the tool planarity. Once the test chips were loaded into the bonder, an alignment procedure was carried out to orient the bump arrays to one another using split-view optics. After alignment, the parts were brought into partial contact, a nitrogen purge started around the Cu bumps to prevent re-oxidation, and the thermocompression bonding process begun. The conditions investigated for Cu-Cu bonding were bonding pressures of ~ 113, 226, and 340 MPa, temperatures of 275 and 300°C, and hold times of 3 and 15 minutes. These bonding pressures correspond to applied forces per bump of 0.44, 0.89, and 1.33 g, respectively.

Bonded assemblies were subsequently probed for electrical connectivity (two-wire probe) and die shear tested or analyzed by cross-section secondary electron microscopy (SEM). Die shear tests were performed on a Royce Instruments Model 550 bond test system containing a maximum 10 kg load cell die shear head; samples were held in a fixture that clamped the bottom die of the assembly while a shearing force was applied to the upper die of the assembly. Visual inspections of the failure interfaces were conducted on all die sheared samples to identify the failure modes and any bonds that did not form during the bonding process.

BASELINE RESULTS

In an effort to establish good baseline bonding parameters, the initial bonding experiment was performed with a full array (7 µm bumps) being bonded to a blanket Cu film using conditions similar to those reported in the literature (300°C with a 15 min hold at 340 MPa of bonding pressure) [7]. The assembly was subsequently tested on the die shear tool and would not shear; indicating the bonding conditions chosen would be a good starting point for our experiments. A 7 µm Cu bumped chip was then bonded to a 15 µm Cu bumped chip using the same conditions. Electrical probing of 30 of the 128 channels (rows) across the assembly indicated a high bond yield with 100% of the channels showing good connectivity. Die shear testing of this sample revealed a bond strength exceeding the maximum load (10 kgf = 110 MPa) of the die shear tool. A set of 7 µm Cu bumped chip bonded to a 15 µm Cu bumped chip assemblies (11 samples) comprised of both types of arrays (device and full) were then bonded under the same conditions to provide some statistics on the bond yield for these process conditions.

Table 1 shows the resistance measurement results from two-wire probe testing of these 11 assemblies. The number of open chains is generally very low, indicating good bonding of the bump array over the entire chip area. For all measurements, the lead resistance of 1.4 Ω has been subtracted from the measurement so that the resistance reported is only that of the daisy chain.

Six of the eleven assemblies were die shear tested with none of the assemblies shearing at the 10 kg load cell limit (i.e. die shear strengths > 110 MPa).The samples were then forced to failure through multiple die shear cycles in order to evaluate the failure interfaces. The predominant failure interface was at the bump base/substrate interface. One of the remaining assemblies was cross-sectioned for SEM analysis of the bond interface and misalignment between the samples.

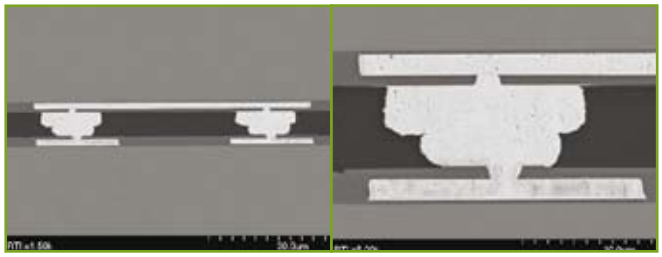

Figure 2 - Cross-section micrographs of Cu-Cu bonds from assembly #1 of Table 1.

Figure 2 shows cross-section micrographs acquired from assembly #1 of Table 1. These results are typical of a Cu-Cu bond formed at 300°C with a 15 min hold at 340 MPa of bonding pressure. The alignment between the bumped parts is very good and the bond line formed between the Cu bumps shows no voids. Some compression of the 7 µm Cu bump (on the bottom) is evident but is not detrimental to the bonded structures.

Using the daisy chain measurements and observations of the failure interfaces following die shear, estimates of bump bonding yield were made. The two daisy chain designs used in the experiments provide different numbers of bump interconnections for electrical measurement, leading to a difference in resistance between the two designs. Since the routing lines contribute approximately equal resistances in the two designs, the difference in resistances can be attributed to the difference in the number of electrically connected bump interconnects in the designs (22 interconnects measured in the device design versus 176 interconnects measured in the full design). The average resistance of the full and device arrays was 14.1 and 11.9 Ω, respectively, for the 7 µm Cu – 15 µm Cu samples. This leads to an interconnect resistance estimate of 15 mΩ for Cu-Cu bonding.

Optical inspections of the post-die shear failure interfaces allowed us to evaluate the number of bad bonds present in a daisy chain row (channel). While a given daisy chain row measures either 22 (device) or 176 (full) interconnects, only one poorly or non-formed interconnect leads to an open channel. Determining how many poorly formed interconnects contribute to an open chain can only be done by optical inspection after separating the bonded sample. Such inspections revealed that open daisy chains were due to no more than 3 bad bonds. Coupled with the electrical measurements (good chain = 176 good bonds), the bond yield for the Cu-Cu bonding process was estimated to be ~ 99.999%.

VARIATION OF BONDING PARAMETERS

Experiments were then conducted to minimize the consumption of IC thermal budgets (lower temperature and soak time) exerted on die during bonding. Attempts to lower the bonding temperature to 275°C, while holding the soak time and mechanical pressure values constant, proved unsuccessful with assemblies exhibiting poor electrical connectivity and low die shear strengths (< 40 MPa). Ensuing experiments performed at 300°C with soak times of 3 min and 10 min also proved unsuccessful. We concluded that, for this

Sample #	1	2	3	4	5	6	7	8	9	10	11
Design	Dev	Full	Dev	Full	Full	Full	Full	Full	Full	Dev	Full
Cu Bump Diameter in µm	15	15	15	15	15	15	15	15	15	15	15
# of Measurements	128	128	128	128	128	128	128	128	128	128	128
# of Good Chains	127	127	127	126	126	121	128	128	128	128	128
Average resistance (Line resistance of 1.4 Ω Subtracted)	11,8	14,4	11,8	13,3	13,0	14,3	12,5	18,3	12,8	11,3	13,1
Standard Deviation	0,9	0,3	4,6	0,8	1,1	2,1	0,9	6,4	0,4	0,4	1,4
# of Bad Chains	1	1	1	2	2	7	0	0	0	0	0

Table 1 - Daisy chain resistance measurements from Cu-Cu samples bonded at 300°C, 15 min soak time, and 340 MPa bonding pressure.

test vehicle and a bonding pressure of 340 MPa, a minimum Cu-Cu bonding temperature of 300°C and soak time of 15 min are required to obtain good connectivity and strong interconnect bonding.

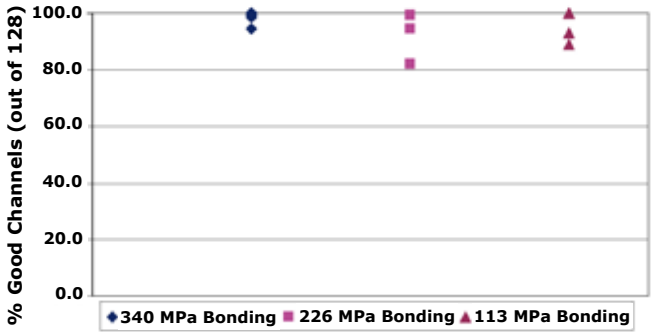

Figure 3 - Effect of bonding pressure on electrical connectivity (% good channels).

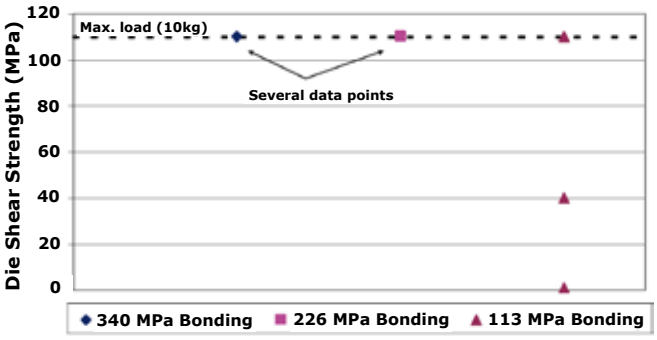

Figure 4 - Effect of bonding pressure on die shear strength. Max. load of tool is 10kg = 110 MPa.

Subsequent experiments were focused on investigating the effects of lowering the bonding pressure. A number of samples were bonded at pressures of 113 MPa and 226 MPa with a bonding temperature of 300°C and soak time of 15 min. As illustrated in Figures 3 and 4, the electrical connectivity (% good channels) and die shear strengths of these assemblies did not match the baseline data obtained from samples bonded at a pressure of 340 MPa. In general, the spread in electrical connectivity and range in die shear strengths increased as the bonding pressure was decreased. Combining these metrics with post-shear microscope inspections, it became obvious that the number of poorly formed bonds increased with decreasing bonding pressure. Specifically, although the 226 MPa bonded parts produced a sample with 82% electrical connectivity, the die shear strengths were still as high as that obtained with 340 MPa bonding pressure. Further, the 113 MPa bonded parts appeared to provide more electrically good interconnects (smaller electrical connectivity spread than 226 MPa bonded parts), but the die shear data indicates that less bonded surface area (i.e., less well formed bonds) was present and that there were more poorly formed bonds along a smaller number of channels. Post-shear optical inspection confirmed these conclusions. The data suggests that for a temperature of 300°C, a soak time of 15 min and a pressure of 340 MPa works best. However, it is possible that a lower bonding pressure could be used if the bonding temperature and/or soak time were increased. Similarly, if a device is more sensitive to thermal budget consumption, a combination of higher bonding pressure (within reason) and lower bonding temperature or soak time may provide high bond yield assemblies. These bonding parameters, along with bonding surface area, are all interdependent parameters when determining the best process conditions for high bond yield assemblies.

THERMAL AGING AND CYCLING RESULTS

Three of the samples from Table 1 (#'s 8, 9, and 10) were subjected to 500 hours of isothermal aging at 150°C. After storage, the samples were re-measured and then sheared. The results of the electrical measurements were mixed. Sample #8 had no open channels prior to storage, but exhibited 6 channels whose resistance had increased to > 100 Ω after storage while the other channels on the assembly showed minor resistance increases (2 – 3 Ω) or slight decreases. Sample #9 had no open channels prior to storage and showed almost no change in resistance after storage. Isothermal storage caused sample #10 to go from no open channels to 9 open channels with an average trace resistance increase of 1.6 Ω.

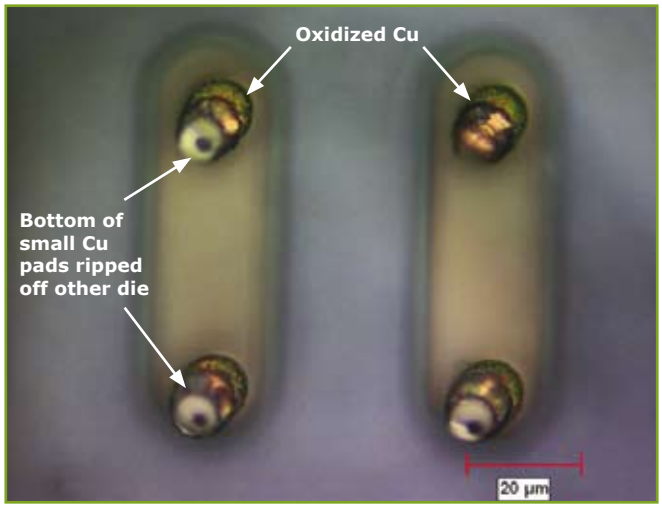

Figure 5 - Optical micrograph of Cu-Cu bonded sample after isothermal aging and die shearing.

These 3 samples were die-sheared and the results were inconclusive, partially due to the low number of samples. Samples 8 and 9 maintained the die shear strength seen with as-bonded assemblies, while sample 10 sheared at just above 40 MPa. All samples showed signs of Cu oxidation (Figure 5), which suggests that oxidative effects at the bonded interface can increase resistance and, in a worst case scenario, compromise the electrical and mechanical integrity of the bonded interconnects. The primary failure interface was the seed layer/oxide interface of the smaller pad. Two samples bonded using the baseline conditions were subjected to multiple bonding cycles (3) to evaluate the effect of multiple thermal/pressure cycles on Cu-Cu bonds. The parts were probed electrically before and after each of the 3 bonding cycles. The number of open channels increased from 0 and 2 (as-bonded) to 22 and 38 (after 3rd cycle), respectively, with the number of open channels generally increasing with each bonding cycle. Die shear testing of the assemblies revealed that the mechanical strength had not deteriorated; both assemblies exhibited bond strengths exceeding the maximum load of the die shear tool (> 110 MPa). Post-shear inspections of the disassembled parts showed

oxidation of the exposed Cu surfaces with the smaller pads being completely flattened out. The multiple bonding cycles appeared to have mechanically damaged the smaller pad to the extent that its contact to the underlying daisy chain may have been compromised. Keeping in mind that the Cu pads were originally 4 µm thick, this result suggests that thicker Cu pads are required for devices that need to survive multiple bonding cycles, such as would be required for vertically stacking more than 2 chips. The main issue that appeared in the thermal aging and cycling tests was oxidation of the exposed Cu surfaces and oxidation migration along the bond interface. Even though this effect may not have lead to immediate failure of all the Cu-bonded interconnects, it presents a reliability issue for Cu-Cu bonding. As a result, RTI is currently investigating underfill and encapsulation materials and processes compatible with Cu interconnects.

Cu-Cu VERSUS Cu/Sn-Cu

The results of the Cu-Cu bonding experiments compare favorably with results obtained from Cu/Sn-Cu bonded assemblies of the same test vehicle (Table 2) [6]. With the proper bonding conditions, both metal-metal bonding systems produced high interconnect yields.

Metal System	Bonding Parameters		Estimated Yield in 176x128 Arrays	Average Mechanical Strength
	Minimum Temperature	Mechanical Pressure		
Cu-Cu	300°C	340 MPa	99,999%	> 104 MPa
Cu/ Sn-Cu	250°C	98 MPa	99,999%	~ 60 MPa

Table 2 - Comparison of bonding parameters and bond characteristics for Cu-Cu and Cu/Sn-Cu bonding.

As expected, Cu-Cu bonds were mechanically stronger but required higher bonding temperatures and pressure to obtain high bonding yields. The assembly process flow for Cu-Cu bonding was simpler than that for Cu/Sn-Cu bonding (no pre-coining and plasma treatment required prior to Cu-Cu bonding) and, thus, would have a higher throughput for manufacturing. Both metal-metal systems are well suited for sub-15 µm diameter interconnects (sub-20 µm pitch) and high density area array bonding. Of the two, the Cu-Cu system is more likely to scale down to smaller pitch dimensions. For both systems, it proved helpful to have the pads on one die in the assembly be slightly larger than the pads on the other die, allowing for high bond yields even when some bonding misalignment was present.

CONCLUSIONS

Processes for producing high Cu-Cu interconnect yield (99.999%) with high mechanical strength (> 110 MPa die shear strength) were developed and demonstrated on an area array test vehicle containing Cu-interconnects ≤ 15 µm in diameter. A short acid clean of the Cu bumps was the only pre-treatment required before bonding. For this test vehicle, the bonding parameter combination of 300°C bonding temperature, 340 MPa bonding pressure, and 15 min soak time provided the best results. When any one of these bonding parameters was decreased, consistently high Cu-bond yield and mechanical strength were no longer possible. Isothermal aging at 150°C for 500 hours showed varying mechanical and electrical performance with some measurements showing improved or consistent performance and others indicating degraded resistance or mechanical performance. Thermal aging and cycling tests also revealed the need for passivation or encapsulation of Cu-Cu interconnects to minimize oxidation of the Cu and improve long term reliability of the bonds. Under-fill materials are currently being investigated for encapsulation of Cu interconnects.

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REFERENCES

1. D. Temple, D. Malta, J.M. Lannon M. Lueck, A. Huffman, C. Gregory, J.E. Robinson, P.R. Coffman, T.B. Welch, and M.R. Skokan, "Bonding for 3-D Integration of Heterogeneous Technologies and Materials," ECS Transactions 16, p. 3-8, 2008.

2. D. Temple, J. Lannon, D. Malta, J.E. Robinson, P.R. Coffman, T.B. Welch, M.R. Skokan, A.J. Moll and W.B. Knowlton, "Advances in 3-D Integration of Heterogeneous Materials and Technologies," Proc. of SPIE 6544, p. 65540-65545, 2007.

3. A. Huffman, M. Lueck, C. Bower, D. Temple, "Effects of Assembly Process Parameters on the Structure and Thermal Stability of Sn-capped Cu Bump Bonds," Proc. 47th Electronic Components and Technology Conference, May 2007.

4. K. Tanida, M. Umemoto, N. Tanaka, Y. Tomita, K. Takahashi, "Micro Cu Bump Interconnection on 3D Chip Stacking Technology," Jap. J. of Appl. Phys., vol. 43(4B), pp. 2264-2270, 2004.

5. H. Huebner et al, "Face-to-Face Chip Integration with Full Metal Interface," Proc. Adv. Metal. Conf., Mat. Res. Soc., 2002.

6. A. Huffman, J. Lannon, M. Lueck, C. Gregory, and D. Temple, "Fabrication and Characterization of Metal-to-Metal Interconnect Structures for 3-D Integration", to be published in Mater. Res. Soc. Symp. Proc. 2008.

7. B. Swinnen, W. Ruythooren, P. DeMoor, L. Bogaerts, L. Carbonell, K. DeMunck, B. Eyckens, S. Stoukatch, D. Sabuncuoglu Tezcan, Z. Tokei, J. Vaes, J. Van Aelst, E. Beyne, "3D Intergration by Cu-Cu Thermo-compression Bonding of Extremely Thinned Bulk-Si Die Containing 10 µm Pitch Through-Si Vias," Proc. International Electron Devices Meeting, Dec 2006, pp. 1 – 4.

Manufacturing and Stacking of Ultra-Thin Film Packages

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ABSTRACT

This paper discloses an ultra-thin and highly flexible package with embedded active chips. In this structure, there are no any supporting and permanent substrates needed. A 3um copper foil with 18um carrier layer was used as temporal substrate. The carrier layer will be removed after chip embedded process. After patterning and etching processes, the temporal copper foil became the bottom circuit that will connect with the other Ultra-Thin Film Package (UTFP). Ultra thin chips with around 15~20μm thickness were assembled directly on the structured Cu foils in a flip-chip fashion. The structured Cu foils were patterned by laser to enhance the wettability with solder. The gap between chip and copper foil was only about 15μm after the die bonding process. In order to fabricate the ultra thin chip, plasma dry etching was applied to release the stress induced during the grinding process and also made the chips' strength higher. The strength of ultra thin chip with and without plasma treatment was also compared. Subsequently, the chips were embedded into highly elastic polyurethane materials, with a copper foil always laminated on the top. The resultant UTFP has a thickness of less than 80 μm. The process details on ultra-thin wafer manufacturing, ultra-thin chip bonding, fine gap with underfill dispensing, thin chip lamination, laser drilling, laser patterning and stacking are also disclosed in this paper. The stacking process of UTFP is also a key technology in this paper. Because the stacking temperature is controlled below 150°C, Anisotropic Conductive Film (ACF) material was used as the connecting medium. So far, the single UTFP has passed static bending test for 200 hours and dynamic bending test for 500 cycles under 5mm bending curvature radius. In the future, the reliability tests which include TCT and TAST tests will be also executed, but not shown in this paper.

The numerical simulation method will also be revealed to figure out the most critical point during UTFP fabrication process and the stacking process.

INTRODUCTION

In past decades, the trends of the electronics devices are going towards high density, low power consumption, high speed and low weight devices. Several advanced technologies such like SiP, 3D stacking and embedding of chips have been utilized to make such devices realized. All the technologies are aiming to smaller form factor and higher performance. Recently since flexible electronics have been drastically developed, adding flexibility into the above mentioned list of functions has set new technical targets for the future.

Consequently, many electronic devices on rigid substrate now will be replaced by mechanically flexible or even stretchable alternatives. Thin and flexible device technologies become very remarkable and have brought out the development of the ambient intelligent vision where more and more electronic systems will be attached on or even embedded inside the human body.

Therefore, flexible electronic system packaging becomes an important technology to carry out the real flexible electronic products. In Europe there are also many EU funded projects, such as SHIFT [1], BIOFLEX [2], and STELLA [3], all of them focus on the development of multi-function, high-integration, mechanically flexible and stretchable electronic systems. The representatives include paper-embedded wireless ID-tags, sensory nodes attached to human skin, wearable electronics, and physiological monitoring systems, etc. A high potential for miniaturization of the electronic system with extremely thin and flexible property is offered by embedding ultra-thin components into flexible materials. Technologies such FCF (Flip Chip in Flex) in IZM [4,5], Flexible SIP Microsystems in IMEC [6], have shown some promising results and demonstrations. In EOL/ITRI, the relative activities in research of Chip-in-Film Package and stretchable circuits had been started since 2005. In this paper, an ultra-thin film package will be demonstrated with only 80um in thickness.

In this paper, the key technologies for fabricating UTFP package that include ultra-thin chip making, embedded process, stacking process, etc. will be particularly described respectively in the following contents.

MANUFACTURING PROCESS OF UTFP

UTFP schematic process flow was clearly shown in Figure 1. Ultra-thin chips are FC bonded on a Cu foil with printed solder bumps. Underfill dispensing and chip embedded within flexible materials are proceeded to fully bury chips forming a flexible thin film structure. The PCB compatible laser drilling, via metallization, and patterning technologies are subsequently followed to fan-out the electric path from chip pads to double sides of the film for electric measurement and for future 3D stacking process. Finally, multilayer UTFP module can then be accomplished by film-to-film stacking. In order to realize an ultra-thin and highly flexible package, many challenging process techniques need to be well developed and qualified, including ultra-thin chip manufacturing, ultra-

low bump printing, ultra-thin chip bonding, fine gap underfill dispensing, thin chip embedded lamination, and film-to-film stacked assembly. Detailed description for all UTFP processing steps is given below, respectively.

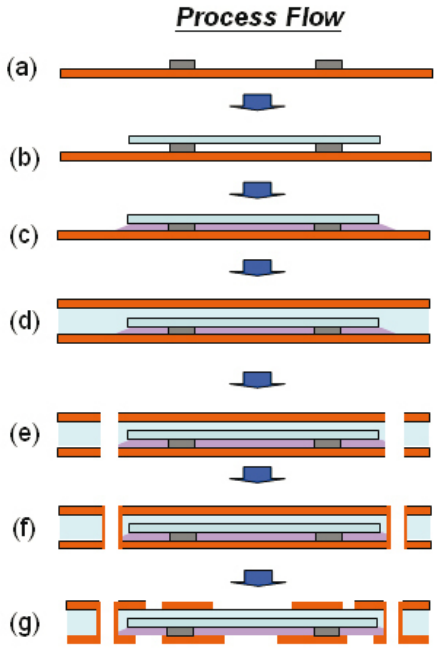
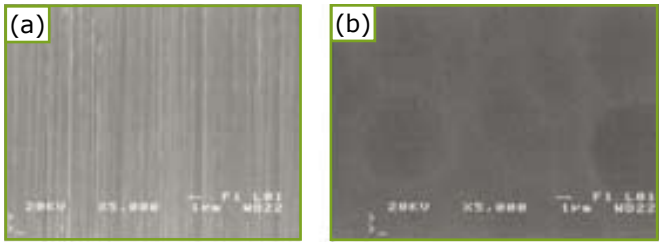


Figure 1 - UTFP schematic process flow.

A) WAFER THINNING

Due to the trends of small form factor, higher performance and lower power consumption, the wafer thickness has gotten much thinner than the previous. As a result, the wafer thinning process becomes a well-known and mature technology. In this paper, mechanical grinding and dry etching process were both used to make the chip down to 15~20μm. For solving the handling issue, DBG (dicing before grinding) was used as well. After the grinding process, the stress release step was applied to strengthen the thin wafer by plasma etching. This process made the surface of ground side smoother to erase the stress concentration phenomenon. The surface condition before and after plasma treatment was shown in Figure 2. Figure 2(a) is the surface condition after grinding process and figure 2(b) is the status after dry etching. The chip strength test was also carrier out by using three¬point bending method. The strength of the chips after plasma treatment is around 40% larger than the chip merely done by mechanical grinding process. The actual stress data is shown in Table 1.



(a) before plasma **(b)after plasma**

Figure 2 - Surface condition.

20μm (only grinding)			
#	Thickness (μm)	Die strength (kg)	Stress (MPa)
1	20	0.011	485.10
2	20	0.0097	427.77
3	20	0.012	529.20
4	20	0.0095	418.95
5	20	0.01	441.00
average			460.40
※ span --> 6mm			

Table 1(a) - Chip strength before plasma etching.

20μm (with plasma)			
#	Thickness (μm)	Die strength (kg)	Stress (MPa)
1	20	0.0154	679.14
2	20	0.0143	630.63
3	20	0.0145	639.45
4	20	0.014	617.40
5	20	0.0142	626.22
average			638.57
※ span --> 6mm			

Table 1(b) - Chip strength after plasma etching.

B) SUBSTRATE PREPARATION & SOLDER PRINTING

Because solder was used as the major bonding material of the electric connection between IZM 40 chip and Cu substrate, it is essential to figure out the wettability between solder and Cu in our structure in advance. In the paper, the 3um Cu foil with 18 um carrier was used as the temporary substrate. After the chip embedded process, the carrier will be removed. Normally, the brown process is used to oxidize the Cu foil and the laser opening process is followed to mark the relative locations of IZM 40 chip's pads.

The target of this process is to remove the oxidation in the IZM 40 chip pads' locations to make better wettability between solder and Cu and will not interact with the other pads. But it is more challenging than the case in the reference [7] due to the thinner thickness in Cu foil. The laser parameter must be carefully controlled to create the bright surface in copper but not damages it, as shown in Figure 3.

This method will replace the usage of solder mask to save the cost and simply the processes. Here, skipping the brown process was also considered to reduce the process steps. Only the native oxide or other protective material on Cu foil was used as the patterning mask. The results are shown in Figure 4. It looks pretty good in the solder ball forming after reflow process. The ball height is also controlled around 15~18um. Figure 5 shows the X-section.

Figure 3 - Copper foil after removing 18um carrier.

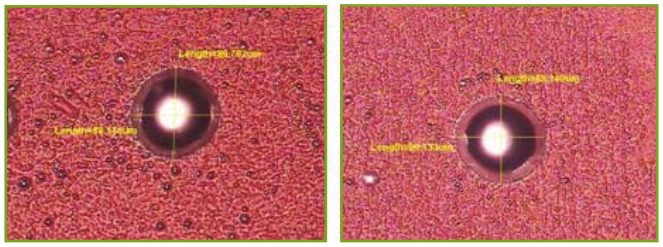


Figure 4 - After solder reflow with brown process (left) without brown process (right).

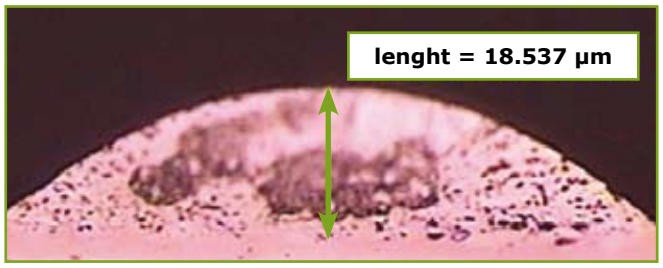


Figure 5 - Ball height after reflow.

C) DIE BONDING

The bonding of ultra-thin chip is one of the key processes in this technology. 15~20µm chip with ENIG UBM was FC bonded to printed solder on Cu foil. Several events such as well-controlled bonding condition, no flux applied, less than 20µm fine gap formation, and no chip crack occurrence are definitely required. Lots of tests were also carried out to catch these performances. Firstly, the copper foil with Sn63/Pb37 solder bumps was placed on the vacuum stage of **SET bonder FC150**. The chip was subsequently bonded on it without applying flux by thermal compression method with the alignment accuracy around ±1µm. Bonding force, temperature and duration time were well adjusted to optimize the width of the gap with around 15µm. The cross-sectional result of connecting joint after bonding is shown in Figure 6. It also demonstrates the 11.5µm thin chip is well bonded on Cu foil. Few voids exist in solder joint and no chip crack occurs.

Moreover, the gap between chip and Cu foil is well controlled around 17µm after bonding, which meets the expected target in this study.

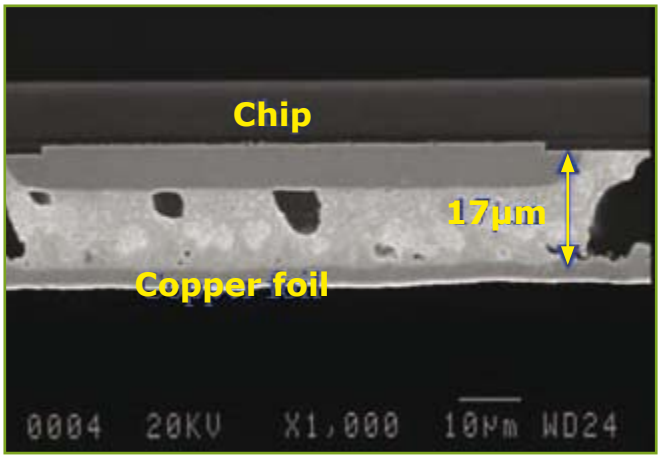


Figure 6 - Connection between chip pad and Cu foil.

D) UNDERFILL DISPENSING

Because of the CTE mismatch between silicon chip and Cu foil, stress would concentrate on solder joints. Underfill could serve as a buffer layer to release the stress. It can also protect the joints from mechanical damage such as impact shock, vibration, bending etc. Furthermore, in order to carry the copper circuits after the metallization process, underfill is definitely necessary to fully fill the gap to form the supporting surface of circuits. Various factors like filler content, CTE, Tg and dispensing pattern should be considered when choosing a suitable underfill material. However, lower CTE and filler content are more important than the others for the reliability and dispensing consideration. Therefore, non-filler underfill is adopted as a solution for 10~20µm gap filling.

There is a trick here when dispensing the underfill. It's because after the bonded sample was removed from vacuum stage of SET bonder and cooled down, the gap between chip and Cu foil became larger and larger from periphery to center due to CTE mismatch. Therefore, in order to solve CTE mismatch problem, Cu foil still stayed on the vacuum plate of bonder to keep uniform width of gap even after underfill dispensing. Subsequently, heating of few minutes was followed to make underfill a little pre-cure. After the pre¬curing process, the sample was removed from the vacuum stage and put into oven under the conditions of 150°C, 20min for the fully curing of underfill. By using this method, there is no any void found between the interfaces. Normally, non-destructive inspection such as CSAM is the best method for void detection. Unfortunately, voids were difficult to be detected here by CSAM due to large warpage. To observe voids under such situation, Cu foil was fully etched by chemical solution after dispensing. Figure 7 is the surface condition after copper removing. It shows the gap was fully filled with underfill and void-free surface was also successfully carried out.

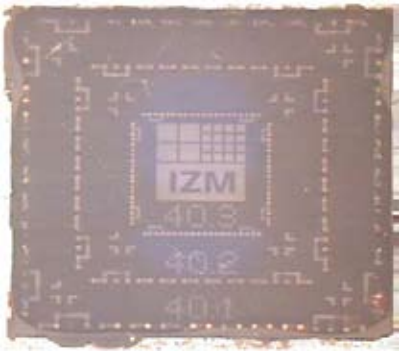


Figure 7:
The surface condition of underfill filling.

E) CHIP EMBEDDED PROCESS

After die bonding and underfill filling process, IZM 40 chip was embedded into flexible material by lamination process. Walopur polyurethane 4201AU from Bayer MaterialScience is used as the embedded material. The thickness is 50µm and the melting temperature rang is from 155°C to 170°C. In order to avoid damaging the ultra- thin chip and let the PU uniformly flow, the lamination temperature is set at 200°C and followed by compression process for 1hr. The vacuum system is also needed to keep the bubbles out of the interfaces. The total thickness after PU lamination process is only 43um. No chip cracks were found on the chip surface as shown in Figure 8. And there is no any void trapped inside as well.

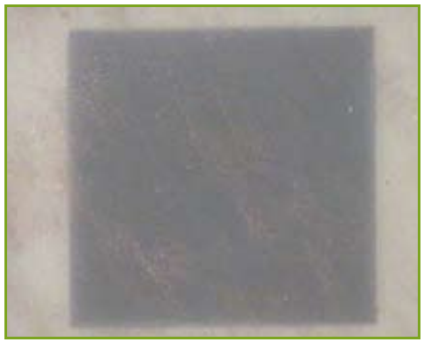


Figure 8: Chip backside after lamination process.

F) LASER PROCESS

The UV laser facility with 355nm wavelength was applied in this paper for laser hatching, laser drilling, laser structuring, and laser cutting process.

In the Laser hatching process, the lower power of 400mW was used for removing the shallow material of oxidation or other protective material on the surface of Cu foil, as shown in Figure 9. For solder paste, the wettability of hatching area is different from other non-hatching area. Therefore, after reflow process, the solder paste can form ball shape on the hatching area.

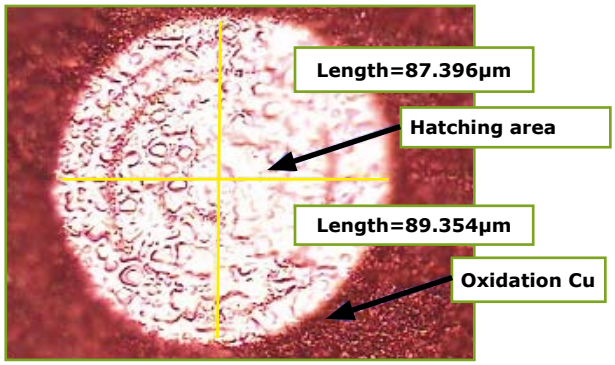


Figure 9 - OM picture of laser hatching on Cu.

Laser drilling process was applied for through via formation. With the metallization process, the front side circuit can be connected to back side circuit by conductive though hole. The diameter of the hole is about 38.5µm on the top and 31.6µm on the bottom, as shown in Figure 10.

The electric patterns were formed by laser structuring process and wet etching process. Laser will ablate 1µm tin and parts of Cu. Tin was set as etching mask to do the Cu etching. Then, the double side pattern was completed after tin striped.

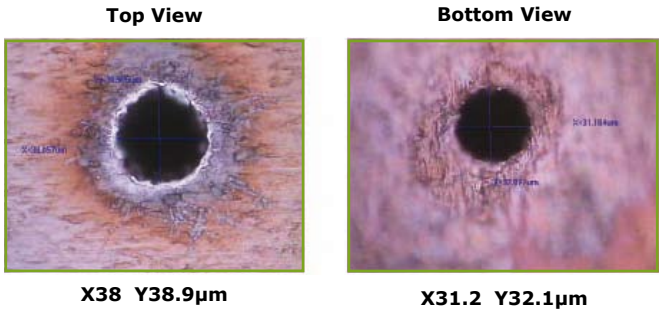


Figure 10 - Laser through hole.

The completed laser structuring pattern is shown in Figure 11. Besides, the accuracy of laser is very important. The accuracy of chip bump with RDL trace was also checked. It is well-aligned, as shown in Figure 12.

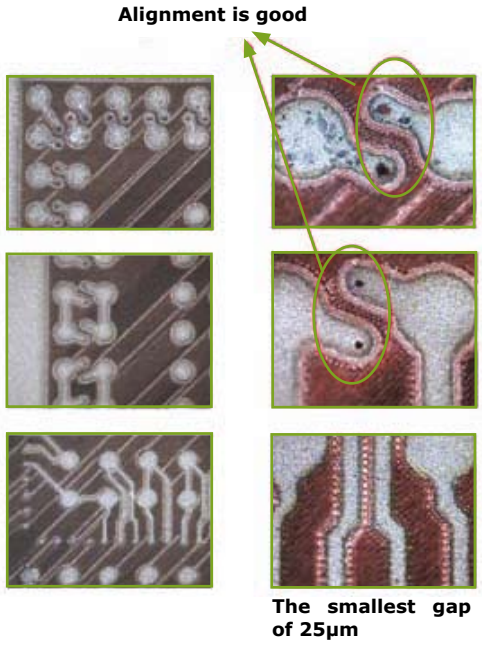


Figure 11 - Laser structuring pattern.

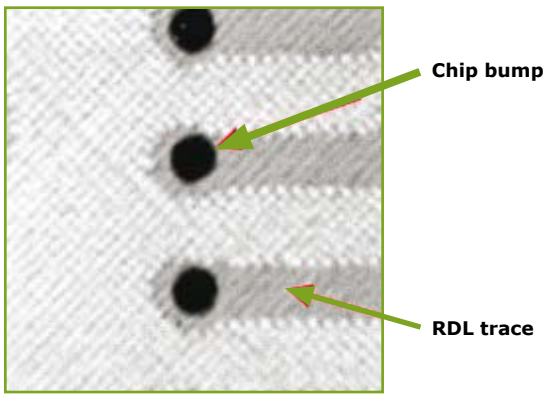


Figure 12 - The alignment accuracy of laser patterning by means of X-ray inspection.

After sample patterning, the laser cutting process was performed to singulate. The cut sample is shown in Figure 13 (a). The PU material of substrate is very soft and no support substrate, so the package is difficult to handle and the PU substrate would be cracked easily. Therefore, our modified method is to leave 1mm Cu frame when cutting, as shown in Figure 13 (b). The Cu frame will provide the support of the package and avoid the crack from PU.

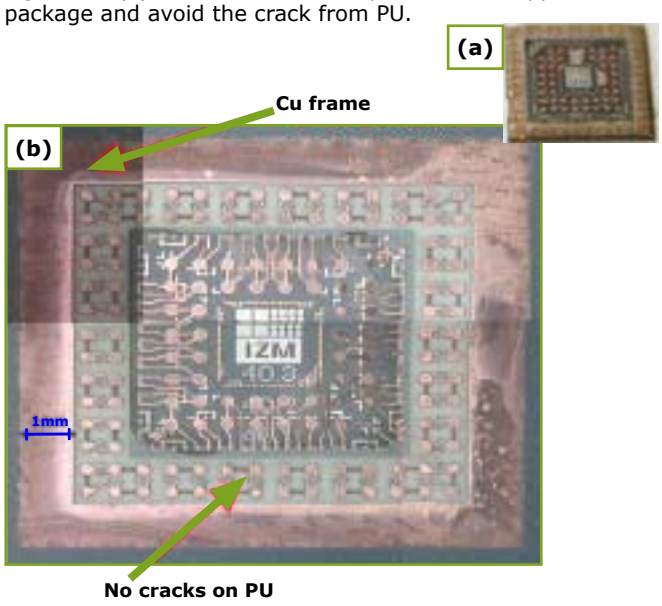


Figure 13: (a) UTFP without Cu frame; (b) UTFP with 1mm Cu frame.

STACKING PROCESS

In the stacking process, ACF was pre-attached on the chip's bottom surface before stacking and precisely covered the whole I/Os area, to prevent the over-covering resin from sticking on the bonder's tooling during the stacking process. The setting of bonding parameters for ACF material is generally divided into two steps. The first step is to soften ACF to uniformly cover the chip. And the second step is to make ACF fully cure.

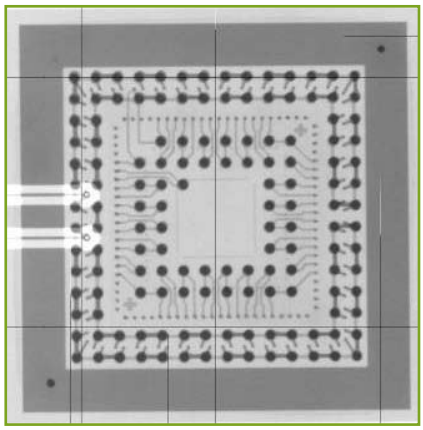


Figure 14: Good alignment accuracy in stacking process.

Figure 14 shows good alignment accuracy after stacking process by using X-ray inspection. The upper and bottom pads were aligned very well, and even no significant shifts or errors are seen. Although the alignment and bonding were controlled well, the resistance measurement of the designed daisy chain still can not pass. This is because the conductive particles of ACF are just around 3um in diameter and ACF did not have effective deformation to make the small conductive particle contact with upper and bottom metal pads.

The bonding force was also raised to compress ACF a little more. As Figure 15 shows, when the load is increased higher than 15kg, chip cracking comes up. Then, even though the electric connection of daisy chain is completed, as Figure 16, the embedded chip was broken into pieces due to higher compressing force.

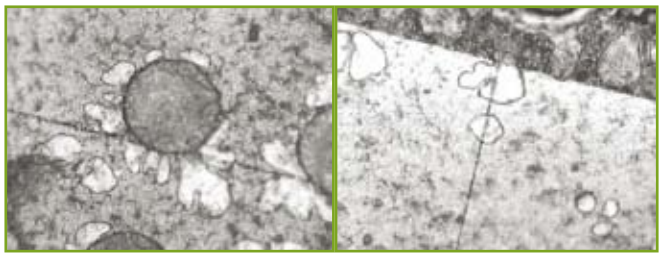


Figure 15 - Chip crack after stacking process.

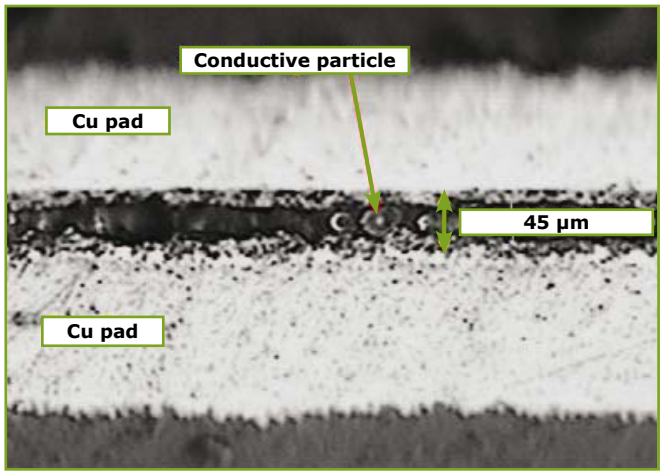


Figure 16 - The status of ACF after stacking.

Referring to the experience in the stacking and bonding process using ACF as a conductive medium, an integrated concept of this process can be brought up. ACF is mostly used in fine pitch applications, such as LCM (Liquid Crystal Module) and so forth. In such a square I/O area with 7mm x 7mm in size, the uniformity in the ACF's deformation is not guaranteed due to incoherent curing status of the resin. The compressing force also needs to be seriously taken into consideration especially for ultra-thin chip. Therefore, the material with low bonding temperature and low bonding force is sill needed to explore and research in UTFP case.

SIMULATION ANALYSIS

A three-dimensional quarter symmetric finite element model was developed by commercial software, ANSYS multiphysics. The numerical simulations of the mechanical behaviors of UTFP structure were subjected to the thermal loading conditions of package stacked process. The package stac-

king stress concentration, distribution, and warpage were analyzed to compare the performance with different structure. Two UTFP structures have been constructed to find the best performance which has minimum warpage and copper via stress. In order to compare the performance of different structures, the mesh density was respectively controlled in these two simulation models. One of UTFP quarter symmetric finite element model is shown in Figure 17, and another structure has a copper stiffener around the outmost area of the package shown in Figure 18. Furthermore, the 3D UTFP stacked with Cu via inside the package was shown in Figure 19. All the main components of multilayer UTFP model, such as substrate, copper pad, through via, bonding adhesive, and PCB are included in the reasonable simplification model. Moreover, all the materials are assumed as isotropic and linear elastic, except the bonding adhesive.

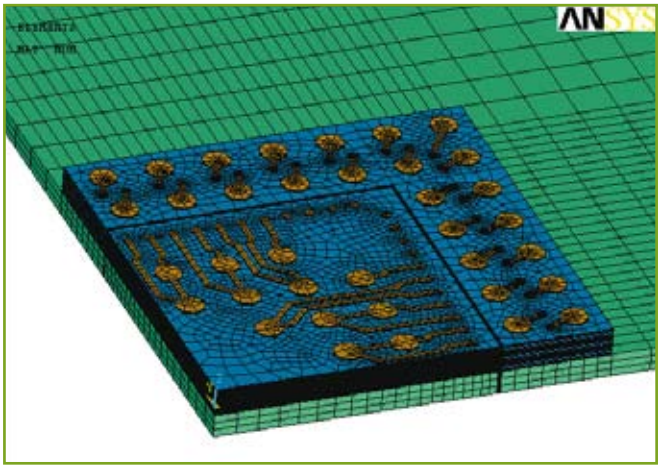


Figure 17 - UTFP finite element model.

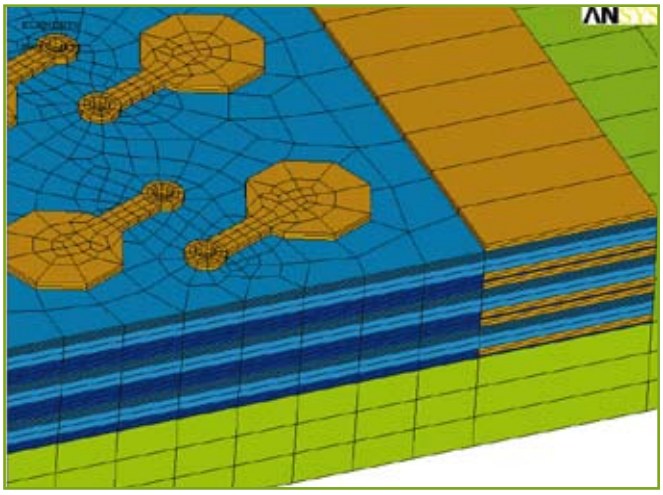


Figure 18 - UTFP with Cu stiffener structure.

In this study, the birth and death simulation technique was used to estimate the residual stress of each stacking process step. Three packages stacking process was simulated step by step in variant thermal condition. Figure 20 shows the residual stress distribution of Cu via and trace in two structures which is with/without Cu stiffener respectively after stacking process. Figure 21 and Figure 22 are the warpage and stress variation during stacking process.

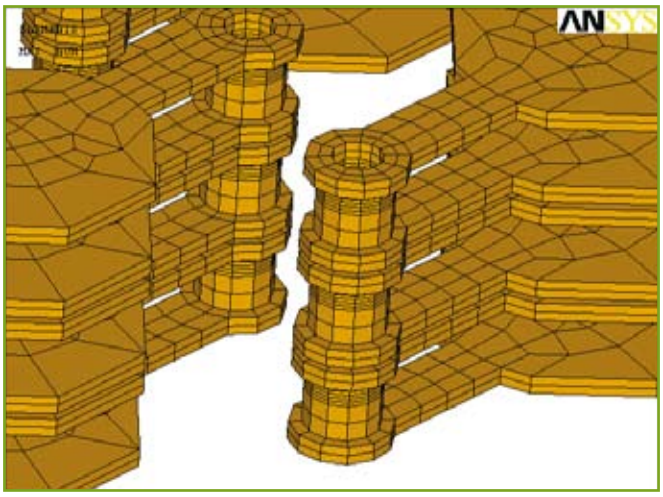
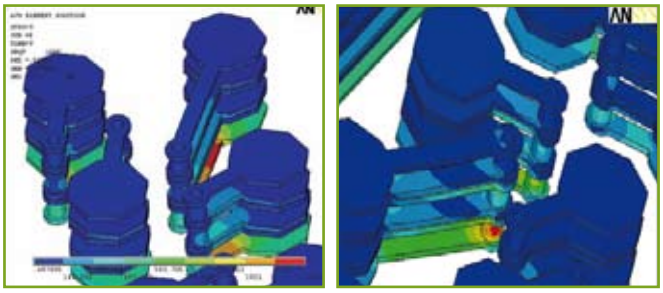


Figure 19 - 3D stacked Cu via structure.

The numbers of simulated steps corresponding to the process condition are shown in Figure 23. From the results, it is found that both of the structures induced larger warpage and stress after each stacking process. Moreover, UTFP with stiffener structure has lower Cu trace stress and smaller package warpage in each process step. These results could give us some significant references for UTFP structure fabrication in the near future.



(a) (b)

Figure 20 - Cu via/trace residual stress distribution.

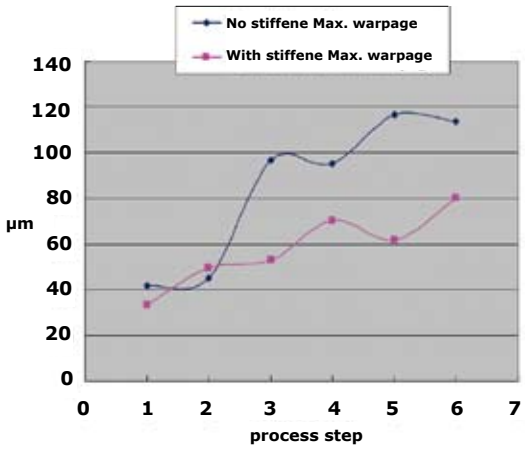


Figure 21 - Warpage variation comparison.

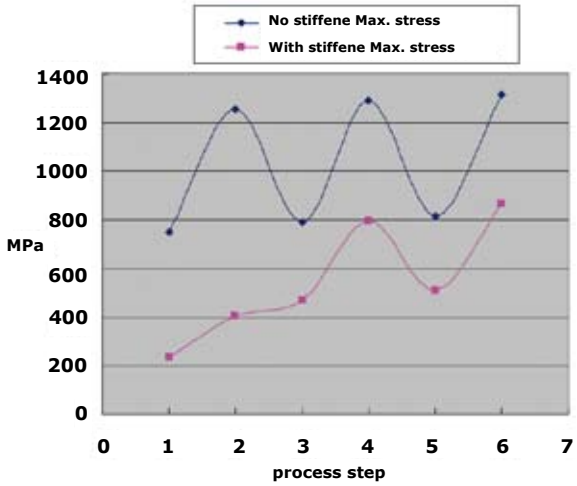


Figure 22 - Stress variation comparison.

- **Step 1:** T= 25°C → T=150°C ⇨ #1
- **Step 2:** package stacked
- **Step 3:** T= 150°C → T=25°C ⇨ #2
- **Step 4:** T= 25°C → T=150°C ⇨ #3
- **Step 5:** package stacked
- **Step 6:** T= 150°C → T=25°C ⇨ #4
- **Step 7:** T= 25°C → T=150°C ⇨ #5
- **Step 8:** package stacked
- **Step 9:** T= 150°C → T=25°C ⇨ #6

Figure 23 - Birth and death process condition.

BENDING TEST

Although the stacking of UTFP is not completed, the flexibility of this structure also needs to be realized. In this part, static and dynamic bending test is applied. In static bending test, single UTFP can resist more than 200hrs under 5mm curvature radius and still does not have any change in electric measurement.

In the dynamic bending test, single UTFP package also can pass more than 500 cycles that includes back and forth procedures. There is no any chip crack found in the chip surface. The electric resistance of the daisy chain is almost the same. Figure 24 shows schematic picture of the bending test. The results of bending test clearly indicate this kind of flexible electronics.

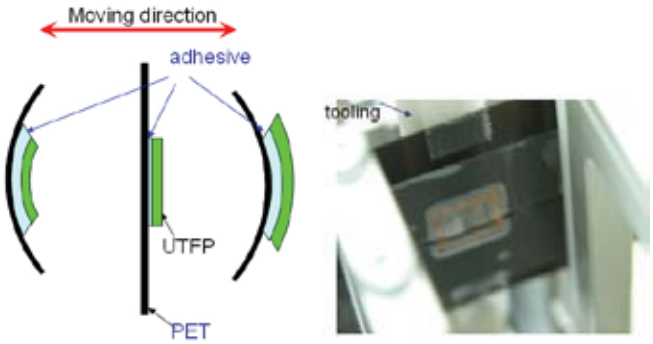


Figure 24 - Bending test scheme.

CONCLUSIONS

So far, UTFP technology has been successfully developed and demonstrated with extremely thin chip and highly flexible embedded material. The bending test of single UTFP that includes static bending test for 200hrs and dynamic bending test for 500 cycles was also accomplished. Because using PU as the chip embedded material that cannot resist over 150°C for a long time, the fail occurred in the stacking process by using ACF. Currently, low temperature bonding materials such as ACA or ACP are positively studied. Besides, the embedded alternatives of PU material is also evaluated in parallel that could endure higher temperature process but still flexible. Although there are some problems in the stacking process, UTFP is also a promising SIP technology for high performance, miniaturization, and multifunctional system integration, especially for the application of flexible electronic products.

Because the manufacturing technology is almost low cost and PCB compatible, it has high potential for mass production cost-effectively if the yield could be well controlled. Therefore, in the future, the reliability tests will also be carried out to verify the feasibility for mass production.

ACKNOWLEDGMENTS

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REFERENCES

1. http://www.vdivde-it.de/portale/shift/default.html.
2. http://tfcg.elis.ugent.be/projects/bioflex/Welcome.html.
3. http://www.stella-project.de/Home/tabid/66/Default.aspx.
4. Löher, T., Neumann, A., Böttcher, L., Pahl, B., Ostmann, A., Aschenbrenner, R., Reichl, H., "Smart PCBs Manufacturing Technologies", *6th International Conference on Electronics Packaging Technology*, Shenzhen, China, Aug. 2005.
5. Löher, T., Neumann, A., Sommer, J.-P., Ostmann, A., Reichl, H., "Chip Embedding into Polymer Matrices of Printed Wiring Boards", *8th VLSI Packaging Workshop in Japan*, Dec. 2006.
6. Cauwe, M., Christiaens, W., Vanfleteren, J., De Baets, J., "Embedding active components as a 3D packaging solution", *Advancing Microelectronics*, Vol. 15, 2006, pp. 15-19.
7. Cheng-Ta Ko, Ying-Ching Shih, Jing-Yao Chang, Tzu-Ying Kuo, Yu-Hua Chen, "Stacking of Ultra-thin Film Package " *Proc 2nd Electronics Systemintegration Technology Conference*, pp.125-130.

New Reflow Soldering and Tip in Buried Box (TB2) Techniques For Ultrafine Pitch Megapixels Imaging Array

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ABSTRACT

Flip chip is a high-density and highly reliable interconnection technology which is mandatory for the fabrication of high end heterogeneous imaging arrays. The control of ultra-fine pitch (<10 µm) and high bumps count flip-chip bonding technology represents a challenge on the roadmap of next generation devices [1].

This paper describes and compares in details two new flip-chip technologies that can address the challenges at the 10 µm pitch node: a modified reflow soldering technology and a thermocompression "tip in buried box" (TB2) insertion technology.

The technological preparation of the flip-chipped devices is fully described including new maskless underbump metallization (UBM) technique, new maskless soft solder buried box filling technique and new "micro-tube" fabrication technique.

First the flip chip experiments are described as well as two methods to evaluate minimum insertion force for the TB2 technology: 500x500 area arrays insertion/ pull out forces are measured as well as original "single tip into solder" insertion/ pull out forces.

The reduction of the required thermocompression forces obtained with "micro-tube" is demonstrated, finally first reflow and thermocompression hybridization results are achieved and commented.

1. INTRODUCTION

Today, two types of flip chip techniques are generally performed for the assembly of high complexity imaging arrays: the "reflow soldering" [2] and the "thermo-compression" technique. However, both techniques present specific issues regarding hybridization yield, most of which are related to planarity and warping of devices to be assembled. In standard reflow soldering approach, planarity defects can be compensated by the relative geometry of the bumps and the wetting surfaces [3]. However, below 10µm pitch the increasing number of interconnection (i.e. device size) and the smallest size of the bumps are not favorable to balance planarity defects, inducing defects such as unconnected bumps. On the other hand, standard thermo-compression technique reduces planarity issues by using force and plastic deformation of solder bumps to compensate non¬planarity. However, any parallelism or local non-planarity defects can induce local over-pressure and generate shorted bumps during thermo-compression.

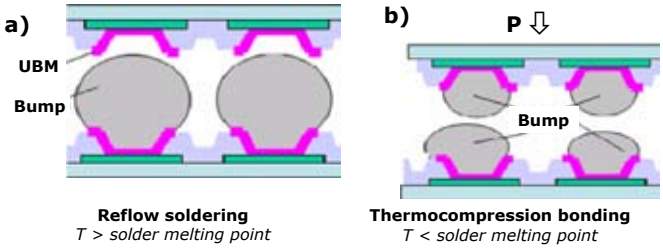


Figure 1 - Flip chip techniques a) reflow soldering, b) thermo-compression.

2. NEW APPROACHES

In this paper, we investigate and compare two new flip-chip approaches using micro-tips to achieve ultrafine pitch (<10 µm) and high bumps count (2000x2000 interconnections): a new reflow soldering flip-chip process and a "Tip in Buried Box" (TB2) insertion technology [4].

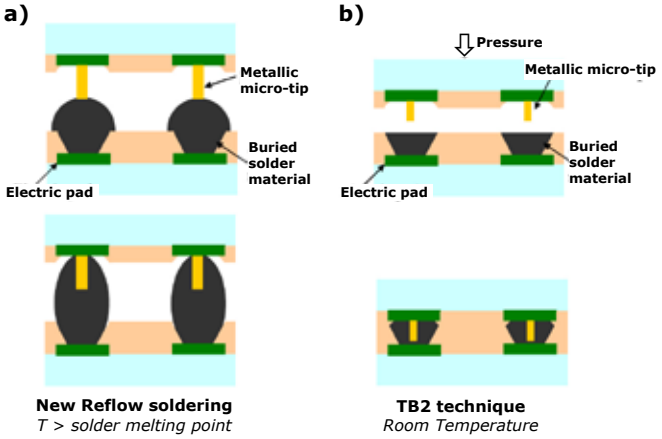


Figure 2 - A new reflow soldering technique (a) and TB2 proprietary technique (b).

A) DESCRIPTION OF THE MODIFIED REFLOW SOLDERING APPROACH (FIG. 2A)

Flip-chip elementary joining is no more achieved between bumps and a planar under bump metallization (UBM)(Fig. 1a) but between bumps and micro-tips used as wicks during the

reflow soldering step (Fig. 2a). This improved technology aims at balancing the planarity defects and bumps non-uniformity by the use of a metal micro-tip as a wick for the solder wetting. This technique described in [5] raises the acceptance level of chip's surfaces non-co-planarity by increasing temperature slightly over solder melting point.

B) DESCRIPTION OF THE TB2 TECHNOLOGY APPROACH (FIG. 2B)

Reflow soldering technique requires the use of chemical flux to break solder oxide during soldering; this may require a costly post-soldering cleaning step. To solve this problem, TB2 technology proposes to break the native solder oxide film by using fluxless physical insertion. Electrical connections are performed by the insertion of conductive micro-tips in ductile material (Fig. 2b). After the initial alignment step, metal micro-tip is inserted into solder box. Thanks to the micro-tips geometry and the indium ductility, the applied pressure can be compatible with conventional Flip Chip bonding equipment. Also, the bonding step can be performed at room temperature followed by solid-solid diffusion [6].

Next sections describe the different processes developed to prepare chips for these two new types of hybridization as well as the development of the hybridization techniques themselves.

3. EXPERIMENTAL STUDY

3.1 UNDER BUMP METALLIZATION (UBM) FABRICATION

The UBM material stack is directly fabricated and self-aligned to passivation openings (vias) delivered chips. For example, the use of standard CMOS surface morphology (Fig. 3) provides immediate fine pitch post-process capability.

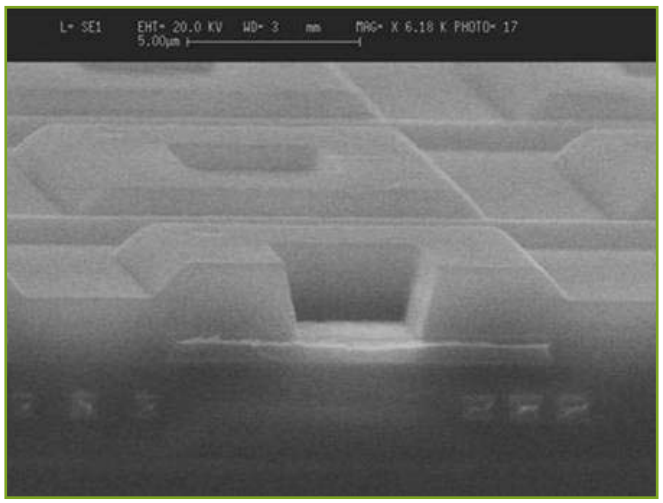


Figure 3 - Typical Si-CMOS Surface Morphology.

3.1.1 MASK-LESS TECHNOLOGY TO BUILD THE UBM WITH A "GAP-FILL" PROCESS

First, a UBM tri-metal stacked layer is full sheet sputtered (Fig. 4a). A planarizing resist layer is spin-coated on wafers to fill the vias. The resist is etched by an anisotropic O_2 plasma (RIE) and the end of etch is controlled by the resist's thickness between the vias (Fig. 4b). The vias are protected by the resist and the unprotected top surface metal layers may be etched by a wet or dry etching (Fig. 4 c). The resist is then stripped to make isolated vias filled with UBM.

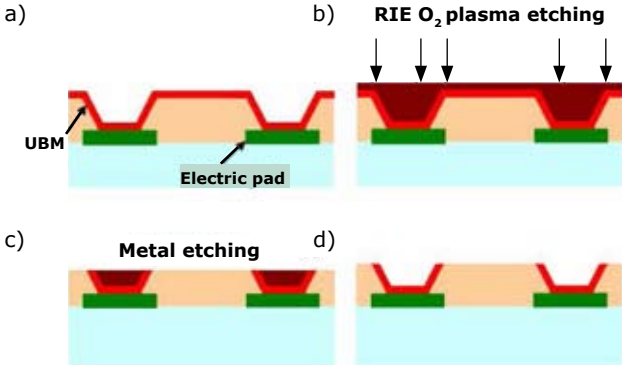


Figure 4 - Maskless "Gap-fill" process to make isolated UBM.

3.1.2 RESULTS ON GAP FILL UBM

Fig. 5a is a SEM picture of 10 µm pitch vias coated with a Ti/Pt UBM and ion-milling etched using the mask-less "gap fill" process. The metal over-etch showed on Fig. 5b is due to the resist over-etch during RIE O_2 plasma etching step. Indeed, in order to control the uniformity of the resist etching, an over etch has to be done. On 2000x2000 unplanarized vias with 10µm pitch, the maximum over-etch is around 650nm (measured by high resolution profilometer) on a passivation thickness of 2200 nm. However, better results can easily be achieved on planarized topology.

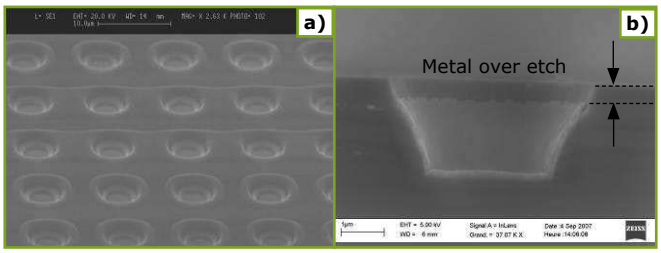


Figure 5 - SEM images of mask-less "gap fill" process to keep the UBM into the vias using the natural topology of the CMOS: a) top view of unplanarized 10 µm pitch vias, b) cross section of planarized 15µm pitch vias.

3.2 BUMPS FABRICATION FOR REFLOW TECHNOLOGY

This technique is a modified version of a standard reflow soldering technique. The 4 millions bumps at 10 µm pitch are fabricated by a standard lift-off technique, however (and as expected) the bumps height and uniformity are degraded for a 10 µm pitch (Fig. 6) compared to "state of the art" 15µm bumps pitch.

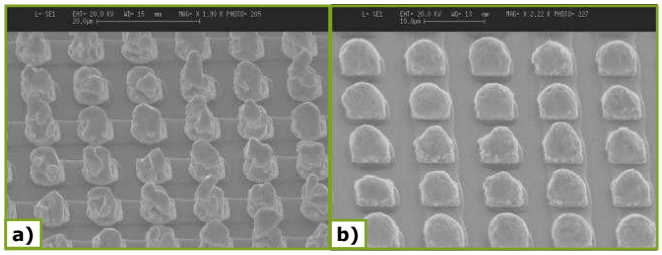


Figure 6 - SEM images of 10µm indium solder bumps made by lift-off technique: a) after lift-off, b) after reflow.

3.3 BURIED BOX FABRICATION FOR TB2 TECHNOLOGY

Mask-less technology was also developed to fill vias (2,2 µm deep) with indium solder material. This technology consists in making a full sheet evaporation of indium (4,5 µm thickness) over UBM made by the mask-less "gap-fill" process. A widely accepted rule for planarization is to deposit a coating whose thickness is at least twice the depth of the vias, prior to polishing. Next, wafer is placed on a Logitech's jig and polished with Logitech® PM5 machine. The polishing planarity is both controlled by optical and mechanical methods. The pad used is made on extra-soft polyurethane (Chemocloth from Logitech®) and different powders (material, particule sizes repartition, shape) have been tested.

Best results were obtained with 1µm alumina powder and a pressure of 2,5KPa. The pressure parameter does not seem to critical for the homogeneity but rather governs the process. The polishing homogeneity is mostly governed by the materials under indium coating. Indeed, the adhesion of indium is lower over SiO_2 than over the UBM surface metal layer (most commonly gold or platinum). Therefore the indium wear rate is more important between vias (on SiO_2) than into the vias. Fig. 7 shows the results of indium polishing.

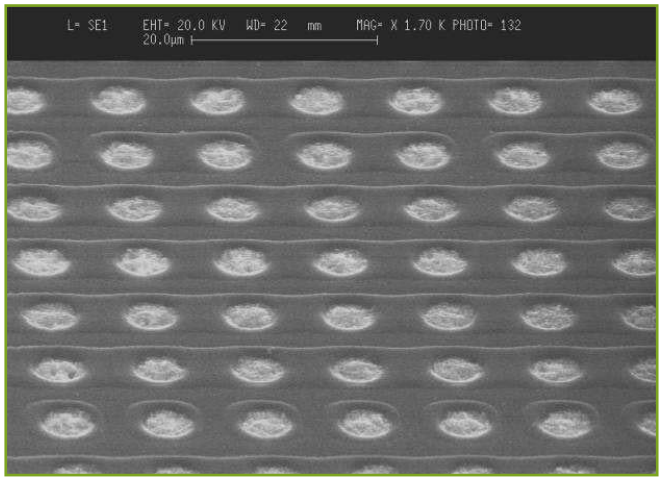


Figure 7 - 2000x2000 vias with 10 µm pitch fill with indium solder material polishing on CMOS topology.

AFM analysis has been done on 2000x2000 array with 7,5 µm pitch. A maximum dishing was measured around 550nm for a thickness of 2200 nm.

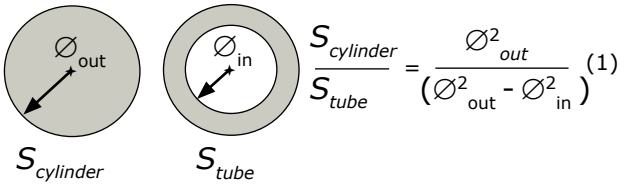
3.4 FABRICATION OF THE MICRO-TIPS FOR REFLOW AND TB2 TECHNOLOGIES

3.4.1 RATIONAL

In this study, all tested flip-chip technologies need micro¬tips for hybridization (Fig. 2a and 2b). The development of a unique "tube shaped tips" process (patent pending) was chosen for all flip-chip sketches.

The insertion force is expected to be proportional to the inserted area cross-section of the tip in the TB2 technology. To reduce insertion forces we developed a proprietary process to make metallic micro-tubes.

The fraction between the surface contact of a cylinder and a tube is given by (1):



$$\frac{S_{cylinder}}{S_{tube}} = \frac{\varnothing^2_{out}}{(\varnothing^2_{out} - \varnothing^2_{in})} \quad (1)$$

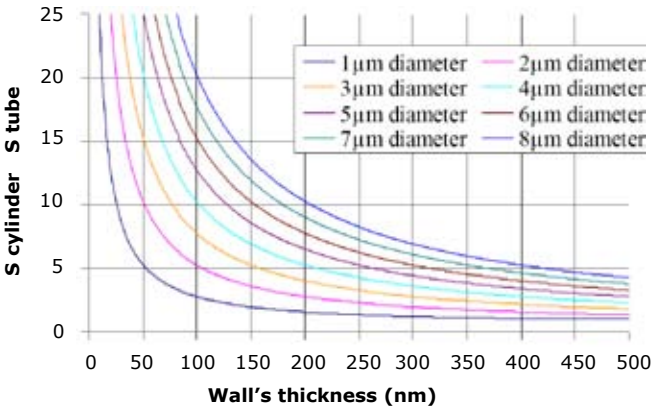


Figure 8 - Tabulated fraction between the surface contact of a cylinder and a tube.

In the case of TB2 technology, the tube shaping:

- Minimizes the insertion surface by reducing the inserted tip area, hence the hybridization insertion force
- Increases lateral contact surface, hence decreases contact serial resistance.

The process developed for such tube like structures uses conformal metal deposits and "gap fill" processes similar to those presented in the UBM fabrication section.

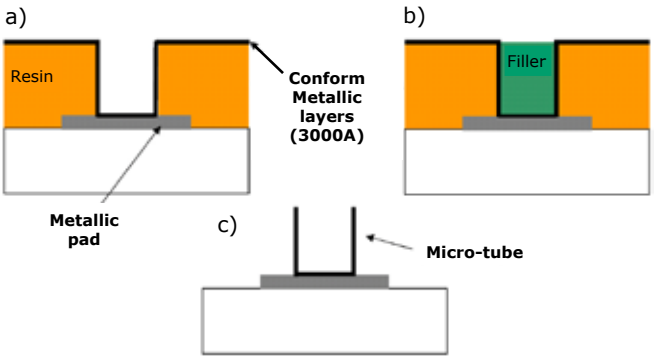


Figure 9 - Micro-tube process flow.

A polymer is first spin-deposited and photo-lithographed over contact pads. Metallic layers of 300 nm total thickness are then deposited (Fig. 9 a). A gap fill process is used to protect the metal located inside vias (Fig. 9b). Top unprotected metal layer is etched by RIE plasma and polymer removed by plasma cleaning thus leaving metallic micro-tubes on the wafer top surface (Fig 9 c). The height and the diameter of the micro-cylinder are defined by the initial polymer thickness and the photolithographic step.

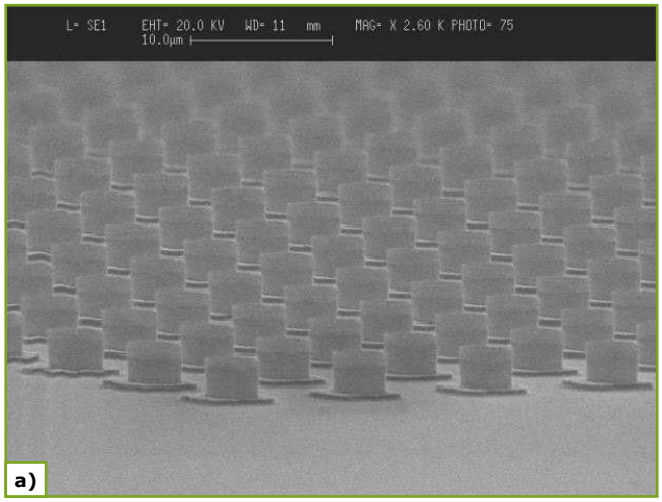
Process was optimized on 3µm diameter micro-cylinder. Test patterns with 1 to 8 µm tube diameters were fabricated for full process capability evaluation.

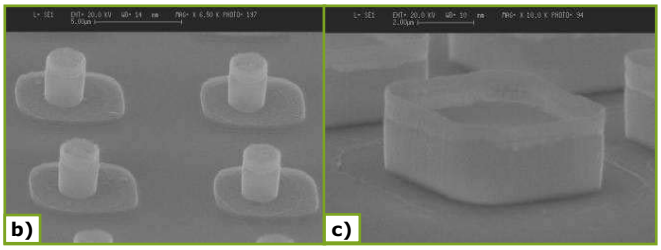
3.4.2 TUBE FABRICATION RESULTS

Arrays of 4-million micro-tubes with 10µm pitch have been processed with excellent yield and uniformity. Fig. 10 shows different micro-tubes diameters, between 2.5-2.8 µm height, aligned on metallic pad of 6x6µm². Micro-tubes from 2 to 8µm came out easily and simultaneously on the same wafer but 1µm diameter test pattern did not. This shows that specific process arrangements need to be developed to get down to such dimension.

Figure 10 - Micro-tubes of:

a) 3µm diameter
b) 2µm diameter
c) 8 µm.





The total metallic wall thickness of the deposited micro-tube is 300nm. However, due to the form factor, a wall thickness less than 300 nm was expected mostly for small diameters. From Fig. 11, the FIB image shows a wall thickness close to 100nm for 3µm diameter micro-tube. We can also see that the tip of the micro-tube is very thin and will be an advantage to decrease the insertion pressure. Notice that local in situ TEOS coating was deposited on the micro-tube to prevent any parasitic redeposit during FIB and improve the resolution of the measure.

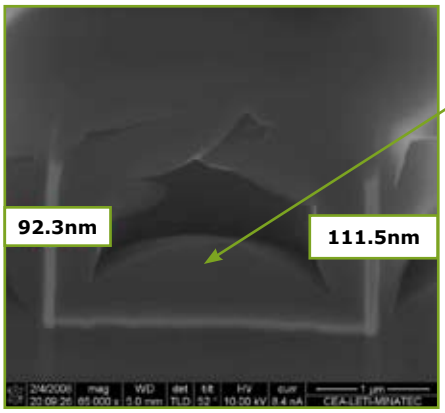


Figure 11: FIB image of 3µm diameter micro-tube.

3.5 FLIP CHIP: REFLOW SOLDERING TECHNOLOGY

The bondings were done using a **SET FC150 bonder** with 500x500 interconnections with 10 µm pitch. A standard reflow soldering flip-chip technology was used, the only difference with classical process being the micro-tube tube presence instead of more conventional planar UBM soldering pads.

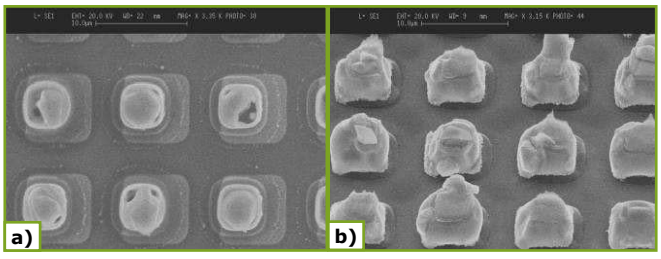


Figure 12 - FIB SEM images after pull tests of:

a) micro-tube of 4 µm diameter at 10 µm pitch,
b) indium bumps at 10 µm pitch.

From Fig. 12 we can see both surfaces after pull out test. Gold finished micro-tubes show indium in their centers (Fig. 12a) transferred from bumps (Fig. 12b) meaning a solder joint was readily achieved.

3.6 FLIP-CHIP: TB2 TECHNOLOGY

3.6.1 PROCESS CHARACTERIZATION USING MICRO-TUBES ARRAY INSERTION IN FULL SHEET SOLDER

The aim of this preparation study was to quantify the force per tip necessary for full penetration of a 500x500 micro-tubes array into a full sheet evaporated indium layer (6µm thickness). Three forces of 0.32; 1; 2 mN / µtube are used to make the insertion, then the top chip is disassembled and the required pull force measured. These tests were done on a Dage microtester 22.

As no metallurgic reaction is expected between the micro-tube's metals and indium solder, we assume that the pull force measured during disassembly is mainly related to friction force between indium solder and inserted micro-tubes.

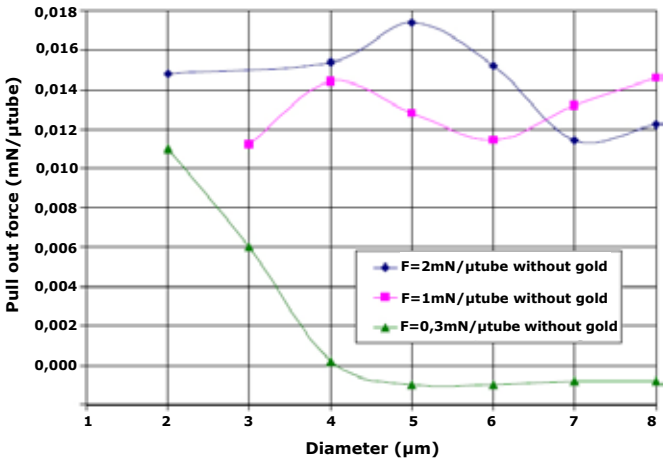


Figure 13 - Release pull out force of 500x500 micro-tubes inserted into indium sheet for different insertion forces and micro-tubes diameters.

For insertion force of 1 mN/tube and 2 mN/tube, high pull force are measured which proves that the micro-tube are well inserted regardless of the diameter. This full insertion of micro-tubes is illustrated Fig. 14.

For insertion forces of 0.32 mN / tube, very low pull forces are measured for tubes diameter > 4 µm (poor insertion), pull force increases dramatically for 3 and 2 µm tubes diameter. Better insertion can be explained quite thoroughly when considering tube perimeter and tube's wall thickness. Indeed, these parameters decrease with tube diameters (asserted by SEM measurements, see example on fig 11) and the insertion surface decrease too.

A first conclusion is that a minimum insertion force to fully insert micro-tubes is included in the range of [0.32-1] mN/µtube depending on tube diameter and tubes wall thickness.

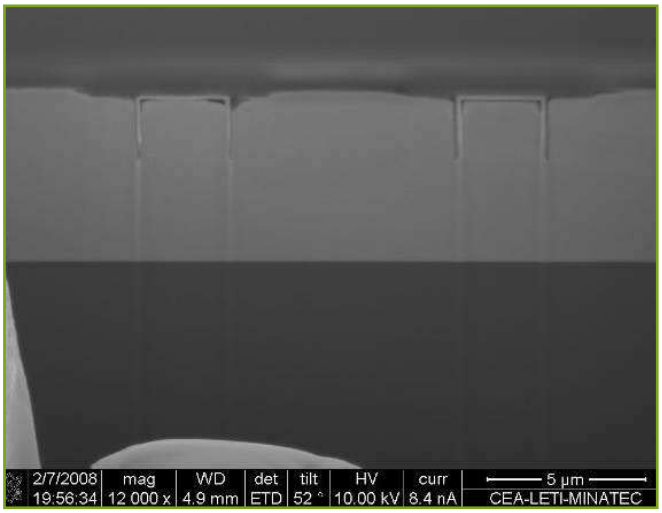


Figure 14 - FIB image of micro-tubes inserted at a pressure of 2mN/micro-tube into 6µm evaporated indium solder.

Pull out forces are close to be divided by 100 folds compare to the insertion force for all diameters. To improve cohesive strength, a solution consists of creating a strong mechanical link between the tip and the solder by creating post-insertion low temperature $AuIn_2$ intermetallics [5].

Hence, in the next experiment micro-tubes were coated by Ti (400A) / Au (500A) sputtering. Insertions of 500x500 gold finished micro-tubes with 10µm pitch were performed with 0.3 mN/tube on all diameter range. A 5 hours / 80°C annealing was added to initiate a gold/indium (solid/solid) diffusion and the formation of an $AuIn_2$ intermetallic consolidation phase between tip surface and solder. [5]

From Fig. 15 the pull out force of gold finished micro-tubes with 5h/80°C increases for low diameters tubes (2 to 5µm) but not significantly for other diameters.

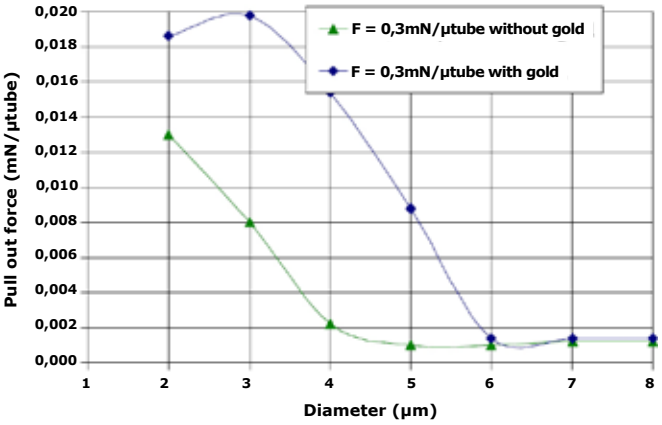


Figure 15 - pull out force after 5h at 80°C annealing of 500x500 micro-tubes gold finished into indium solder material for different diameters (insertion force: 0.3 mN/tube).

Poor improvements of the pull out force between uncoated and gold finished micro-tubes for diameter above 5 µm are mostly related to poor insertion depth. As demonstrated before insertions of micro-tubes above 5 µm diameter are only superficial (Fig. 13). In this case, the gold to solder contact

surface is too small to complete intermetallic phases and to reinforce cohesive mechanical properties.

However, SEM images of the 3 µm diameter gold finished micro-tube prints, after pull test, show some missing indium solder region meaning an intermetallic consolidation (Fig. 16).

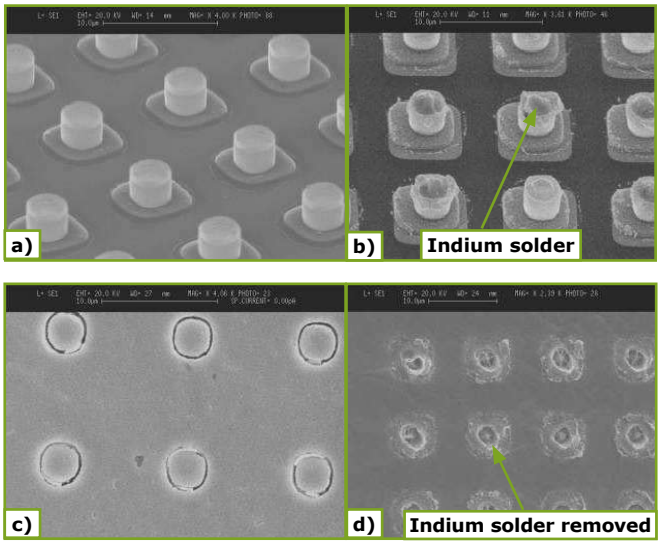


Figure 16 - SEM images after pull test of:

a) 3µm diameter uncoated micro-tubes,
b) 3µm diameter gold finished micro-tubes with 5h/80°C,
c) 3µm diameter uncoated micro-tube prints into indium full sheet solder with 5h/80°C diffusion step,
d) 3µm diameter gold finished micro-tube prints into indium full sheet solder with 5h/80°C diffusion step.

The pull out results for the gold finished micro-tubes results were not as good as expected which is probably due to a too thin gold thickness.

The drawback of pull test is the separation mode of the two dies. Indeed it may not correspond to a simultaneous separation of all the micro-tubes of the upper die from their indium target. It can rather correspond to a complex peeling mode and the calculated mean pull out force per micro-tube is certainly underestimated. Moreover pull out test does not give a direct access to the load/displacement micro-tube curves.

3.6.2 PROCESS CHARACTERIZATION USING NANOINDENTER AND SINGLE TIP INSERTION

To obtain more accurate insight into the tube insertion process, a nanoindentation apparatus (MTS instrument, nanoXP) was modified. Isolated 13µm radius indium bump reflowed on 3x3 mm^2 silicon chip (Fig. 17) were mounted at the end of the indentation column facing 5x5 mm^2 dies with 500x500 micro-tubes of 3µm diameter and 2.8 µm height at 10 µm pitch where mounted on the substrate holder as target to the indium bumps.

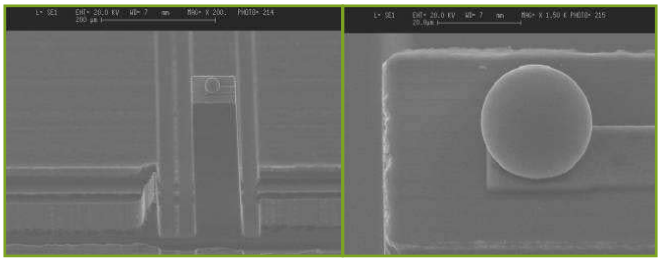


Figure 17 - Sample of 26µm diameter indium solder bump over 200µm silicon structure for unitary insertion by a micro-tube.

In this configuration, four insertion experiments were carried out. Each experiment corresponds to one new indium bump and one new micro-tube.

Insertion experiment number	1	2	3	4
Tube gold coated	no	no	yes	yes
Target die number	1	1	2	2
Loading rate (µN / sec)	33.3	33.3	33.3	33.3
Max load (µN)	1382	295	1043	575
Creep delay (sec)	240	240	240	240
Load decrease during creep (µN / sec)	81	26	71	45
Unloading rate (µN / sec)	33.3	33.3	33.3	33.3

Table 1 - Single tube microinsertion experiment parameters.

Indium bump versus micro-tube axis alignment is performed with a +/-1µm lateral precision using the indenter column as a profilometer. During this operation, contact force between the micro-tubes and the indium bump is always bellow 3µN. Insertion tests are constructed to simulate the matrix die assembly process with a 2 mN/min loading and unloading rate and a 4 minutes creeping stage at max load. Max Load for experiments 1 and 3 are not explicitly chosen at the beginning of the experiment but is automatically chosen during the experiment to correspond to a 3.5 µm insertion depth to be sure to have a contact between indium top surface and tube bottom. Maximum load for the experiments 2 and 4 was explicitly chosen to have indium surface just in contact with tube bottom after analysis of experiments 1 and 3 results.

After the experiments, each indium bumps was observed with a SEM (Fig. 18). Experiment 1 SEM image shows a slight imprint of the tube at the bump top due to a too high tube detection load level at the beginning of the experiment. We consider that it has not impacted the obtained load vs. displacement curve.

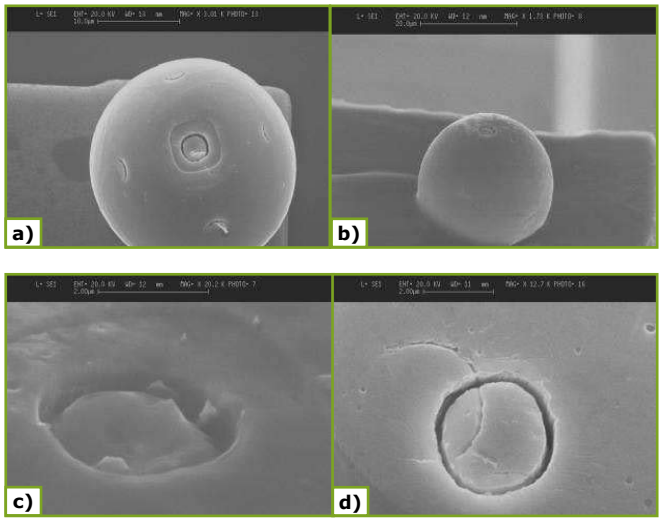


Figure 18 - SEM images of indium bumps after experiment :

a) experiment 3,
b) experiment 4,
c) experiment 4 detail,
d) experiment 1 detail.

Fig. 19 shows the obtained load vs. displacement curves for respectively the two uncoated and the two gold coated micro-tubes at different loads. Main results of the experiments are described in Table 2.

In both cases, indium contact with tube bottom is identifiable on the displacement curves at roughly 2.6 µm depth by a change of the curve slope which is confirmed by the SEM images of indium bumps (Fig. 18) where the impression mark of the rectangular metallic pad positioned under the tube bottom can be identified. Simple geometrical consideration shows that at 2,8 µm insertion depth, the first neighbours of the tested tubes should also touch the indium bump surface as seen on Fig. 18a. Only experiment 2 didn't insert the tube down to it bottom. Full micro-tube insertion arise at loads around 500 µN and no appreciable differences is seen between gold coated and uncoated tubes. At maximum load, the 240 seconds creep time corresponds to the plateau on the curves. This plateau is slightly decreasing due to applied load drift. The obtained drift values during experiment are summarized in table 1.

Creep depth is important and corresponds to tube insertion at constant load for experiment 2 and bump flattening for the three other experiments. Tubes pull out occurs without important tube breaking as shown with SEM images of tube imprints (Fig. 18). Pull out occurs suddenly when a critical pull out load is reached. Assembly elongation is of tens of nanometers. The higher the maximum load applied, the higher the tube pull out load, with a pull out load that should be situated between 200 and 500 µN for a tube ideally inserted with the indium surface just touching the tube bottom.

Figure 19 - Load vs displacement curves for insertion experiment:

a) uncoated tubes (exp. 1 and 2),
b) gold coated tubes (exp. 3 and 4).

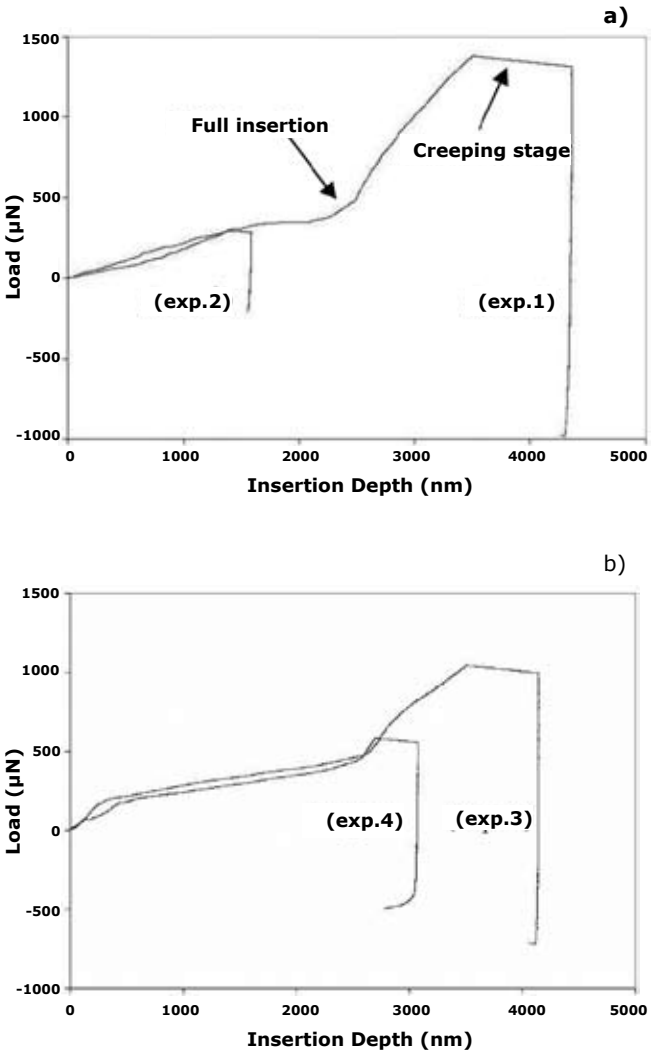


Table 2 - Single tube microinsertion experiment results.

	1	2	3	4
Load at indium contact with bottom (µN)	490	n.p.	510	478
Creep plateau depth (nm)	835	185	612	349
Pull out load (µN)	-980	-212	-719	-492
Pull out assembly elongation (nm)	70	33	43	50

Finally, pull out curves does not help concluding on a different behavior of gold coated and uncoated tubes. The only noticeable difference arise on the first 200 µN of loading where tube insertion is more difficult for gold coated tubes certainly due to their less sharp wall at the top.

Using the nominal hardness value of 8,8 Mpa [7] for in

dium, the plastic deformation should begin at 8,3 µN for ideal 200 nm thick tubes. Therefore, we can consider that load vs. displacement curves correspond mainly to viscoplastic deformation of indium and further analysis of insertion mechanism will require the study of insertion creep behaviour of micro-tubes under constant load and at different insertion depth.

3.6.3 COMPARISON BETWEEN AREA ARRAY INSERTION AND SINGLE TIP PULL OUT TESTS ON 3 µM DIAMETER MICRO-TUBE

		Insertion force (µN/µtube)	Pull out force (µN/µtube)
Area array insertion	Uncoated	[320 ; 1000]	> 8
	Gold coated		> 20
Single tip insertion	Uncoated	≈ 500	< 210
	Gold coated		490

Table 3 - A summary of main insertion results from both techniques (nanoindentation & pull out tests) on 3 µm diameter micro-tube.

Minimum single tip insertion force is measured to be 500 µN which is effectively inside the initial range of [320 ; 1000] µN indicated by area array insertion method. Single tip pull out forces are much higher than those calculated with area array method. This indicates that a complex peeling mode is taking place during the separation of the 500x500 array connections. Considering a 500 µN single tip insertion force, calculated insertion force for 4 megapixels area array should be 2 kN, which is easily achievable with **SET FC300 High Accuracy & High Force flip-chip bonder.**

4. NEXT STEPS

Previous results show that the insertion forces are proportional to the micro-tube diameters. Next the hybridization of 4 megapixels arrays will be achieved using 3 to 5 µm micro-tube diameters which are the available tubes today.

The next following step will be to investigate the newly developed reflow soldering and TB2 techniques using available (ready for flip-chip) 4 megapixels arrays. Indeed, to test electrical performances of the bonding techniques daisy chains have been implemented on chips (Fig. 20) to accurately calculate the resistance access and the defectivity (open or short circuits).

Both bonding types (reflow or thermocompression) between chips will be done using the SET FC300 bonder thanks to its reflow soldering or thermocompression versatile configurations. The alignment capability of the bonder is a primordial parameter and the misalignment of this equipment should be less than ± 0,5 µm at the 2 kN thermocompression force required in our case.

Eventually, reflow soldering can be achieved using oxyde reduction atmosphere or vacuum to avoid gas trapping inside tubes.

Different annealing and gold thickness will be performed to improve pull out forces and electrical results. More experiments should be done on unitary tip insertion by nanoindentation to optimize the insertion process. Indeed, creep delays must be studied to further decrease the insertion pressure.

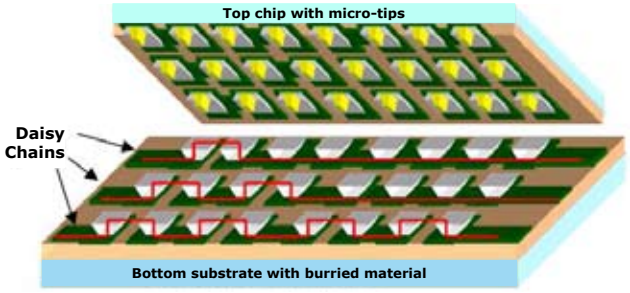


Figure 20 - Daisy Chain Test Vehicle for Electrical Validation.

5. CONCLUSION

The latest developments on technologies for high complexity 10 µm pitch area arrays hybridization have been presented. Important efforts were done to modify the buried box fabrication from CMOS vias in a maskless and low cost process at 10µm pitch. To reduce insertion force, a proprietary process to build 4 million metallic micro-tubes with 10 µm pitch has been developed. Insertion pressure has been theoretically reduced by 8 folds for a 3 µm diameter micro-tube compared to a full cylinder tip. A unitary insertion experiment was used to measure the minimal insertion load, which was up scale to estimate the load for a 4 million area arrays hybridization. Next step will be to measure electrical resistance of such interconnections made by reflow soldering and thermocompression and choose which should be the best scalable technology for future.

ACKNOWLEDGMENTS

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REFERENCES

1. L. Kozlowski Progress in Ultra-Low Noise Hybrid and Monolithic FPAs for Visible and Infrared-Astrophysics and Space -Science Library-vol. 300 pp123-130
2. M. Fendler, F. Marion, et al. "Wafer scale flip-chip technology for IRFPA", Proc of Advanced Technology Workshop on Military, Aerospace and Homeland security, Baltimore, 2003
3. US Patent.5,489,750
4. C. Davoine, M. Fendler, F. Marion, "Low temperature F/C technology for fine pitch bonding", Proc of ECTC San Diego, 2006, p 24-28
5. F. Marion and all, "Système de composants à hybrider autorisant un défaut de planéité", PCT Application WO99/16120.
6. C. Davoine, «Densification des connexions "flip-chip," grande surface», M.S. thesis, CEA-LETI, MINATEC, Grenoble, France, 2006.
7. William Alexander, James Shackelford, CRC Materials Science and Engineering Handbook, Third Edition, 2001.

Electrical Characterization of High Count, 10 µm Pitch, Room-Temperature Vertical Interconnections

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ABSTRACT

In order to increase the format of heterogeneous staring arrays to 2Kx2K pixels or even larger complexities, limited substrate size and cost reduction considerations make mandatory the reduction of the pixel size, but the mastering of ultra-fine pitch and high count flip chip bonding technology represents a challenge [1,4].

To overcome the planarity and thermal mismatch issues while reducing the bonding thermo-compression forces and the hybridization temperature, a new room-temperature insertion technology has been proposed and developed [2,3,4]. This study gives first measured interconnection yield and serial access resistance of 2Kx2K, 10µm pitch hybridized arrays fabricated using this technique. A comparative study proves that parallelism during insertion is a key parameter. The micro-tube insertion technique is scalable to complexities of over four million connections, with pixel pitches down to 5µm. Hence, a derivative low temperature insertion concept could possibly be applied to 3D interstrata interconnections solving the cumulative high temperature cycles issues encountered when using more conventional high temperature processes.

1. INTRODUCTION

Two main families of flip-chip joining techniques (fig1a, fig1b) are commonly in use for the fabrication of heterogeneous imaging arrays [5].

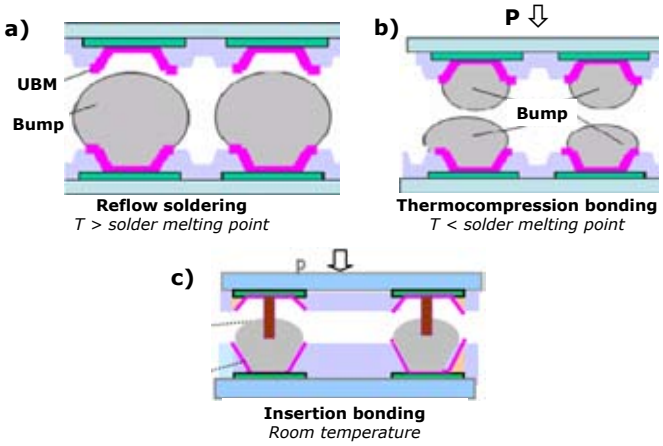


Figure 1 - Flip-chip techniques (imaging arrays).

When high pin count (i.e. 10k connections /mm²) and low pitch (i.e. <10µm) complexity is required, **classical C4 type reflow soldering techniques** (Fig. 1a) do not allow the balancing of chip planarity defects, leading to unconnected bumps. CTE (Coefficient of Thermal Expansion) mismatch can also be a major issue due to high solder reflow temperature (for heterogeneous materials the X, Y misregistration can approach pitch value at solder temperature).

Thermo-compression technique (Fig. 1b) can reduce planarity issues (using force and plastic deformation of solder bumps to compensate Z non-planarity), however high pressure levels are required and can induce local over-pressure defects or generate shorted bumps during thermo-compression. X,Y CTE mismatch is still a problem if compression temperature is set too high.

To solve these issues, a new **"insertion" flip-chip technique** (fig 1c) is proposed [2,4]: metallic tips are inserted in solder lands to perform ultrafine pitch (< 10 µm) and high bumps count (2000x2000) interconnections: it features a fluxless, low pressure, room temperature joining process well adapted to heterogeneous imaging arrays fabrication.

The present work gives the first electrical results obtained with that approach when using "micro-tubes" as the inserted tips [2].

2. RATIONAL FOR MICRO-TUBE

In the beginning of this project [4] first insertion experiments were realized using plain cylindrical tips (Fig. 2). One of the conclusions of that work was that insertion forces would be too high for future higher complexities and that sharper tips geometry were mandatory.

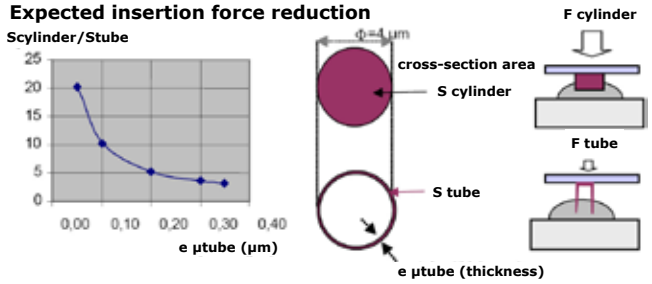
In a first approximation we postulated that the insertion force would be roughly proportional to the insert cross-section area: then one idea was to build a "cylinder shaped" insertion tip to reduce the insertion force.

The insertion force for a tube-like shape can be approximated from the insertion force of a plain cylinder with the formula:

$$F_{tube} = \sim F_{cylinder} / (S_{cylinder} r / S_{tube})$$

With:
F tube = force to insert one tube into one solder land
S cylinder = cross section area of one cylinder
F cylinder = force to insert one plain cylinder into one solder land
S tube = cross section area of one tube

Numerical application of the formula demonstrates that insertion force could hopefully be divided by 10, thanks to the using of 4µm external diameter / 0.1µm thin micro-tube (compared to the insertion force required by a 4µm diameter plain cylinder).



Hypothesis: Ftube = Fcylinderx (Scylinder/Stube)

Figure 2 - Insertion force reduction.

3. PROCESS SKETCH

The following global process scenario was then developed: first, chip 1 is processed with soft solder lands (Fig. 3), then Chip 2 is processed with "insertion" tips/micro-tubes (Fig. 3), finally, after a classical alignment, the metallic micro-tubes arrays are inserted into solder lands arrays at low temperature and low pressure (Fig. 4).

Figure 3 - Chips preparation.

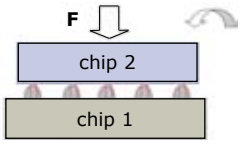


Figure 4 - Chip joining (insertion).

Fluxless process: the gold plated micro-tubes break the native solder oxide film establishing an immediate electrical contact. No flux cleaning is required.

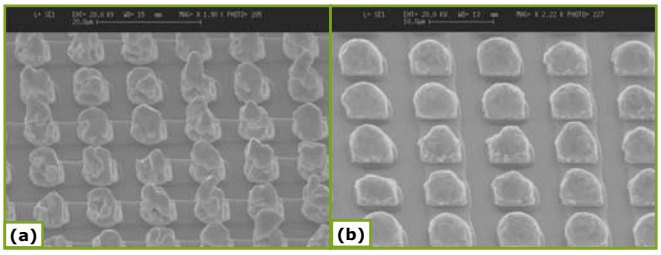
Low pressure process: thanks to the sharp micro-tubes geometry and high indium solder ductility, insertion forces are reduced (<0.5mN/connection) like the local overpressure. Applied forces can be handled by conventional flip chip bonding equipment even for very high pin counts (i.e: >4 million connections).

Room temperature process: CTE mismatch issues are suppressed; the bonding step can eventually be completed by solid-solid diffusion.

4. PROCESSES DEVELOPMENT: SOLDER LANDS AND MICRO-TUBES FABRICATION

SOLDER LAND FABRICATION RESULTS

The 4 millions indium solder lands at 10µm pitch were fabricated using a standard "lift-off" technique; solder lands were reflowed at 180°C for 1 minute (final solder reflow).



(a) After lift-off **(b) After reflow**

Figure 5 - SEM images of 10µm indium solder lands made by lift-off technique.

MICRO-TUBES FABRICATION RESULTS

A proprietary "micro-tube" fabrication process was developed using conformal metal deposition and "gap fill" type processes.

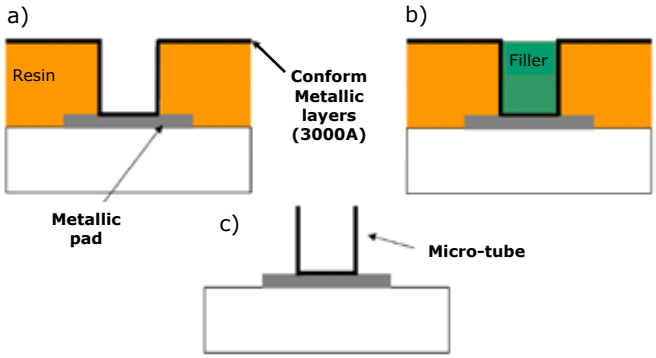


Figure 6 - Micro-tube process flow.

First, a sacrificial polymer layer is spin-coated then etched over contact pads, micro-tube skin is then fabricated:

a) A metallic layer stack of 300nm total thickness is sputtered
b) The metal layer located inside vias is protected (thanks to a proprietary gap fill process)
c) The unprotected top metal layer is etched by RIE plasma, residual polymer inside vias is removed by plasma cleaning to complete micro-tube fabrication.

The geometry (height, diameter) of the micro-cylinder are defined by the initial polymer photolithographic step, the micro-tubes skin thickness is controlled by the metal deposition parameters.

Test patterns with 1 to 8 µm tube diameters were fabricated for full process capability evaluation; however, electri-

cal evaluation was limited to 4µm diameter tubes. Arrays of 4-million micro-tubes with 10µm pitch were processed with excellent yield and uniformity.

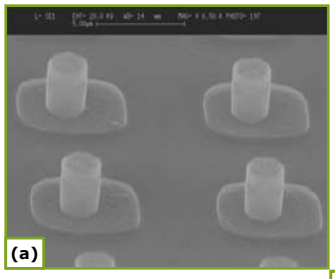
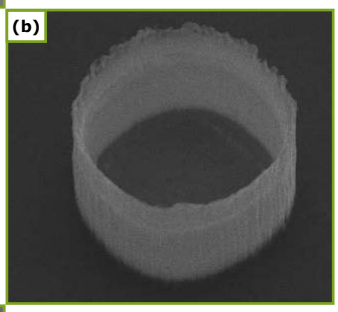
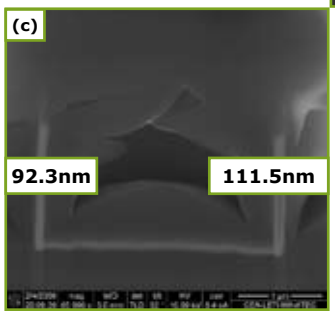


Figure 7:
Micro-tubes fabrication results (a, b: SEM top views, c: Micro-tube's FIB cross section).

Fig 7 shows different micro-tubes diameters, between 2.5-2.8µm heights, aligned on 6x6µm² metallic pads.





The final vertical skin thickness was measured at 100 nm on 4µm diameter tubes (Fig. 7c).

5. FLIP CHIP BY INSERTION: PROCESS DEVELOPMENT

As-built chips were readily assembled by insertion with 0.5mN applied load per connection, this resumes to 2kN applied load per chip for 4. 10^6 total vertical connections. First electrical results showed that parallelism during insertion was a critical parameter.

Next section evaluates how parallelism control during insertion can influence connection yield.

PARALLELISM CONTROL

A room temperature, low force assembly process was developed using a commercial SET FC300 type machine. Two types of chip to chip parallelism control were compared in this study (Fig. 8-9).

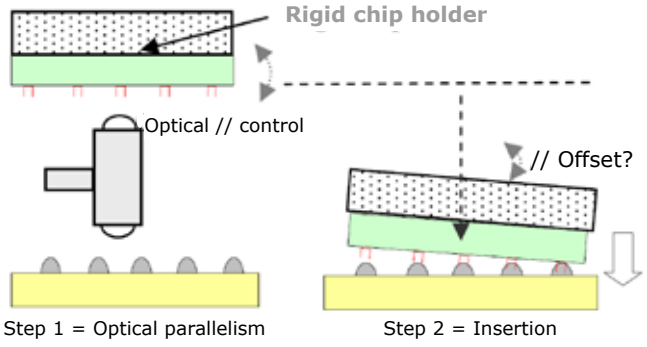


Figure 8 - Parallelism without auto-levelling.

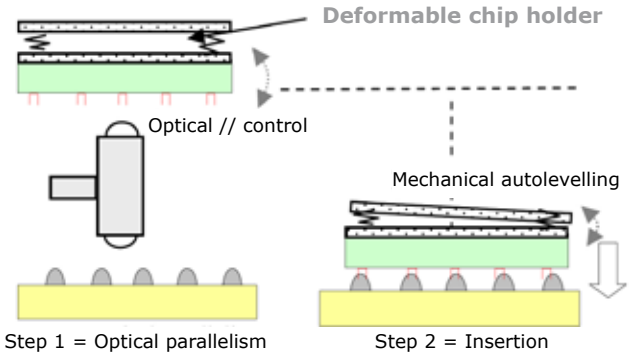


Figure 9 - Parallelism by mechanical auto-levelling.

Type 1 - Pure optical parallelism (Fig. 8): upper chip is held by a rigid (flat) holder tool, chips parallelism is tuned prior to thermo-compression thanks to the integrated optical autocollimator. Parasitic parallelism offset can occur between alignment position (separated chips) and insertion position (chips in contact).

Type 2 - Optical parallelism + Mechanical Auto-levelling (Fig 9): upper chip is held by a specific **"auto-levelling holder tool"** which deforms under applied load. Optical parallelism is still performed in upper position (same as 1) but, during the insertion step, the autolevelling tool can deform mechanically if load proves to be non uniform. This tool allows to spread an uniform load (i.e.: recovering parallelism) between mated chips surfaces while preventing X, Y in-plane misalignment.

The two parallelism principles were evaluated and compared on two hybridized chips using the SET High Accuracy & High Force FC300 bonder in thermo-compression configuration for the same 2kN insertion load (i.e. 0.5mN/connection). The alignment capability of the bonder is a primordial parameter and pre-measured misalignment proved to be less than ± 0.5 µm at the 2kN compression force required in our application, chip parallelism was pre-tuned in alignment position thanks to the built in autocollimator (spot diameter 8mm, pre-leveling accuracy of 25µrad).

6. ELECTRICAL RESULTS

6.1 TEST VEHICLE

The 20x20mm arrays are hybridized using chips processed with 4 µm diameter micro-tubes. Daisy chains are implemented on chips (Fig. 10) and make possible to compute either serial resistance access per connection or local defectivity yield: open and short circuits percentage are statistically calculated by a 2.56% sampling of all connections (102312 connections are tested out of a total of 4. 10^6 total connections).

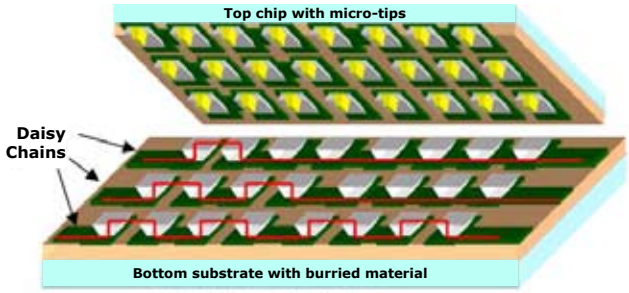


Figure 10 - Daisy Chain Test Vehicle.

6.2 TEST RESULTS

A) CONNECTION RESISTANCE

The vertical access resistance (including contacts resistance and serial resistance) is calculated from the measurement of a large number of uniformly spread daisy chains with 2, 20 or 100 connections.

The access resistance value is directly derived from the slope of the regression line obtained when plotting the chains serial resistance versus the number of connection of the chain (Fig. 11).

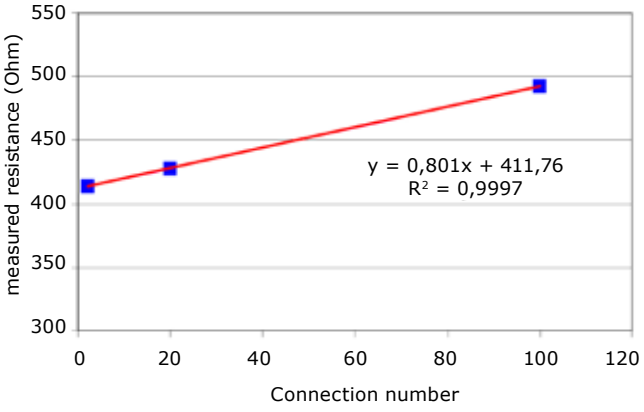


Figure 11 - Serial access resistance.

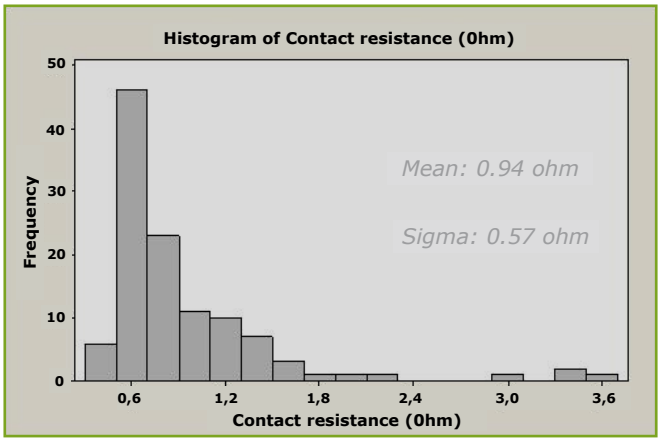
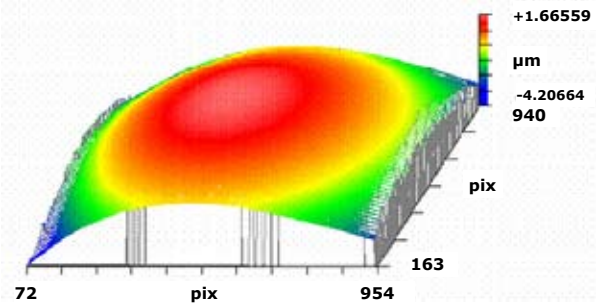


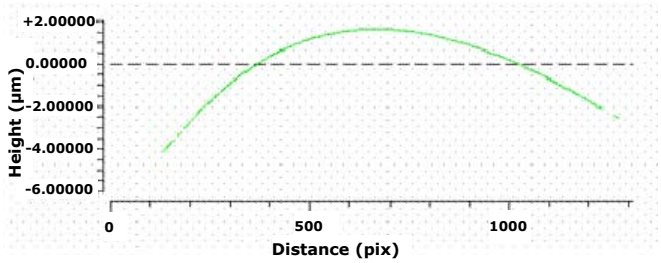
Figure 12 - Serial access resistance histogram.

B) YIELD COMPARISON (WITH OR WITHOUT AUTOLEVEL):

PLANARITY MEASUREMENTS

With conventional hybridization techniques (i.e.: reflow soldering and bump to bump thermocompression), the non planarity of the chips before hybridization is a key parameter strongly impacting connection yield, the processed faces (indium lands and micro-tubes faces) need to be fully characterized before joining. Both chips were measured convex and the maximum out of plane face to face value "deltaZ" was extracted from Zygo measurement's data (Table. 1).





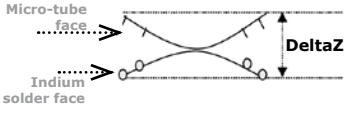
Experiment 1 DeltaZ		Experiment 2 DeltaZ
8.3µm		8.1µm

Table 1 - Out of plane deltaZ.

Notice that such out of plane large values (>8µm) would have render "hybridization by reflow" technique (fig. 1) physically impossible (reflow technique does not allow to reduce warping by pressure).

YIELD MAPPING

Each chip is divided into 60 sectors. The yield is calculated using the numbers of closed daisy chain in each sector. Using a statistic method, we can plot the hybridization yield (Fig.13).

Experiment 1: without autolevelling

98,6	99,1	99,1	98	99,1	99,1
99,6	98,6	99,1	97,3	98,6	99,1
99,6	100	100	97,3	100	100
98	100	100	99,1	99,6	100
99,6	99,6	100	98,6	100	99,6
94,7	93,3	100	98	98,6	99,6
98,6	99,1	95,7	99,6	97,3	100
88,3			88,3	93,3	95,7

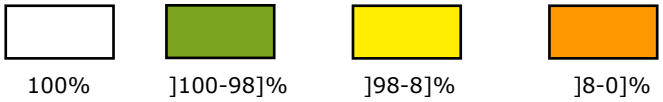
Experiment 2: with autolevelling

	93,3	98	98	95,7	93,3
	94,6	94,6	94,7	99,1	99,6
91,4	97,3	98	99,1	99,1	100
91,4	91,4	96,6	99,6	99,6	100
98	99,1	99,6	99,6	100	100
98	100	100	100	100	100
94,6	99,1	100	100	100	100
	98,6	98,6	99,1	100	100
	91,4	98,6	99,1	100	100
		96,6	98	96,6	98

20mm

20mm

Connection (%):



100%]100-98]%]98-8]%]8-0]%

Array connection yield >75,3%
Mean array short circuit <0,01%

Array connection yield > 88,1%
Mean array short circuit < 0,01%

Figure 13 - Connection yields.

7. DISCUSSION

Results obtained in this work (using 4µm diameter micro-tubes) are compared with previous results obtained using 4 µm diameter plain cylinder insertion [3].

	Micro-tube insertion	Cylinder insertion	Gain
Insertion force (per connection)	0.5mN	3.6mN	7.2
Insertion T°	Room temperature	80°C	
Vertical access resistance (per connection)	0.94Ω	7.4Ω	7.9

Table 2 - Micro-tubes versus cylinder insertion.

Insertion force:

The 7.2 fold reduction of insertion force agrees with the 10 fold initial extrapolation (fig2): standard thermocompression machines can be used for 2K*2K array insertion.

Access resistance:

The mean access resistance per connection is measured at 0.94 ohms/connection (with a standard deviation of 0.57 ohms across the 20*20mm array), this is a reduction by 7.9 compared to plain cylinder insertion [3]. It can be partly explained by a larger contact surface between the tube and the solder (2 faces contact) and secondly by the different mechanical plastic deformations behavior shown by SEM analysis.

Yield discussion:

1) No short circuit between adjacent connections are measured throughout the whole hybridized arrays: this demonstrate the advantages of the insertion technique over indium/indium thermo-compression technique;

2) The connection yield (open circuit) is encouraging for a first experiment and, regarding the large unfavorable "out of plane" non-planarity, demonstrates the advantages of the insertion technique over pure reflow technique (note that that reflow technique would have shown many open circuits with the same initial non-planarity conditions).

Finally it is shown (fig.13) that the implementation of an autolevelling tool significantly enhances the global connection yield (from 75.3% to 88.1%).

8. CONCLUSION

A low temperature, low pressure flip-chip process has been developed and proved feasible using two different insertion scenarii, connection yield has been measured on first 2K*2K hybridized arrays.

We demonstrated a connection density of 10k connections /mm² with a mean Z connection serial resistance of 0.94 ohm (σ = 0.57 ohm) per 100µm². First yield evaluation show 88.1% connection yield and 0% short circuit between connections, these results are encouraging despite the large

unfavorable 8µm out of plane chips non-planarity (either reflow or thermocompression techniques would have been ineffective with such conditions).

Finally, two room temperature insertion processes have been compared and show significant connection yield enhancement when using a specific "autolevelling" holder tool.

9. FUTURE WORK

First, connection yield has to be improved and to be fully distributed over the 20x20mm chip, second no specific temperature baking were performed after room temperature insertion to complete intermetallic formation and to improve contact resistance: these topics will be part of our next work for imaging applications.

Applying this technology to other application is also part of our objectives and, provided the choice of a new metallurgical configuration is made (solder type, tube type, etc…), a derivative low temperature insertion concept could possibly be applied to 3D interstratas interconnections : this opportunity is also under evaluation.

ACKNOWLEDGMENTS

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REFERENCES

[1] L. Kozlowski Progress in Ultra-Low Noise Hybrid and Monolithic FPAs for Visible and Infrared- Astrophysics and Space -Science Library- vol. 300 pp123-130.

[2] D. Saint-Patrice, F. Marion et al. New Reflow Soldering and Tip in Buried Box (TB2) Techniques For Ultrafine Pitch Megapixels Imaging Array Proceedings ECTC Orlando FL2008 pp 46-53.

[3] C. Davoine, M. Fendler, F. Marion, "Low temperature F/C technology for fine pitch bonding", Proc of ECTC San Diego, 2006, p 24-28.

[4] C. Davoine,"Densification des connexions flip-chip grande surface", M.S. thesis, CEA-LETI, MINATEC, Grenoble, France, 2006.

[5] G.Humpston, D. Jacobson Principles of soldering pp 199-203 Ed ASM International The material Information Society.

3D Stacked Chip Technology Using Bottom-up Electroplated TSVs

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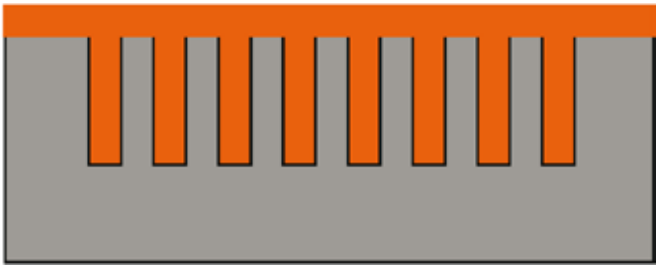
ABSTRACT

In this study, bottom-up electroplating is used for TSV (Through Silicon via) fabrication. With the metal temporary bonding technology, we could remove the handling substrate and perform the chip stacking process. The TSVs made by bottom-up electroplating do not need the expensive MOCVD seed layer deposition and special designed electroplater/solution. Moreover, it is independent with the DRIE angle and the scallop at the sidewall of the vias. By using the bottom-up electroplating technology, we could fabricate the TSVs in much shorter process time to save the process cost. From the X-Ray images and the SEM pictures, the diameter of the vias is 5.3 micronmeters and the length of the vias is 67 micronmeters. The aspect ratio of the bottom-up electroplated TSVs is larger than 12 and all the vias are definitely void free. X-Ray image also shows the process yield is very high. After the thermal shock reliability test, the resistance measurement and the vias are fine from the SEM pictures. There is no crack found at the sidewall of the vias. After the TSV process, the bonded electrode continues to serve as electrode for the mask-less Sn electroplating. The electroplating current goes through the bottom electrode TSVs and the Sn is electroplated on the TSVs without mask define. Sn bump served as mechanical and electrical connection. We also demonstrate the dry etching process for wafer thinning on a 170°C thermal release tape with handling substrate. After the etching process, the thickness of the chip is about 5μm and then it is released from the handling substrate successfully. For thin wafer handling technology, we proposed a metal temporary bonding technology. Au to Au bonding is used here for metal temporary bonding. After the wafer thinning process, the sample could sustain high temperature process without crack and could be removed from the handling substrate after the process. This study also demonstrates the process flow for the 3D chip stacking by using the bottom-up electroplated TSVs. The handling substrate is removed by metal temporary bonding technology and the interconnection is done by Cu/Sn bump. Based on this technology, the TSVs in the 3D chip stacking could be made in shorter electroplating time and low cost way by a traditional electroplater.

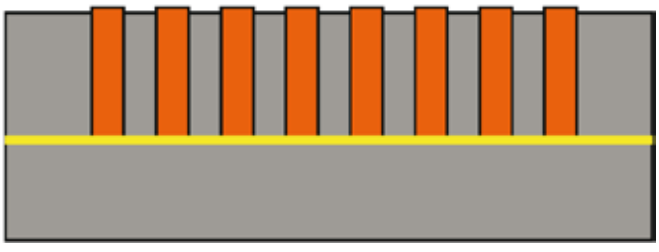
INTRODUCTION

3D IC package has good ability to integrate several chips. High capacity memories and multi-functional packages, for example, could be easily made by this technology. SiP (System in Package) apply spacers and wire bonds for electrical interconnection, but it is not suitable for high performance packaging due to high RC delay caused by lengthy wire bonds. TSV technology is another way to achieve 3D packaging. Signals are transmitted directly from upper layers to lower layers through TSVs which have the shortest path and minimum RC delay.

There are several ways to form the TSV structure. Fig. 1(a) shows the most common TSV processes starting with DRIE, insulation/barrier layer deposition, seed layer deposition and via filling. As the trend for high density package, via diameter is getting smaller and smaller. The aspect ratio is usually larger than 5 with a 10μm diameter opening. Seed layer deposition by MOCVD is needed for good step coverage in such a high aspect ratio micro vias. High performance electroplating machine with special designed solution is used for via filling and the filling process is usually time consuming and expensive.



(a) Traditional TSV Process



(b) Bottom-Up TSV Process

Figure 1 - TSV Process Introduction.

Fig. 1(b) shows an alternative way to fabricate TSV structures starting with bottom electrode PVD, DRIE, bonding and bottom-up electroplating. The bottom electrode could be made by sputtering metals on polymer and then remove the polymer to form the film type bottom electrode [1] or by

direct metal to metal bonding. Metal to metal bonding had been widely researched and evaluated [2] [3] [4]. In this study, both Cu to Cu and Au to Au bonding are considered and tested. Due to the demands for the low temperature process and Cu oxidation issues, Au to Au bonding is finally adopted as the bottom electrode [5].

BOTTOM-UP TSV FORMATION

TSVs made by bottom-up Cu electroplating is proposed in this paper for high aspect ratio via filling. Fig. 2 illustrates the process flow for bottom-up Cu electroplating. One of the wafers is resized by laser cutting for electrode contact during electroplating. The wavelength of the UV Laser is 355nm and the process time for the diameter of 140mm after cutting is less than 30min. for each wafer. Wafers are then cleaned by ultrasonic, Ar plasma and sputtered with TiW/Au for following bonding process. Photolithography process and DRIE process are performed on the resized wafer for via formation. The two wafers are then bonded without alignment by Au to Au wafer bonding process. Due to the low temperature requirement for process integration, the Au to Au bonding is finished below 200°C within 30min.

Plasma activation is an important factor to enhance the bonding strength and lower the bonding temperature. Both Ar plasma and N_2 atmospheric plasma could be used here. Since the N_2 atmospheric plasma do not need the time consuming pumping down steps for vacuum environment, N_2 atmospheric plasma is more suitable for low cost process and mass production. The power of the plasma is 250W and the process time is 150sec. Bonding strength is evaluated by the pull test equipment and the result showed more than 30MPa bonding strength is achieved by this bonding condition.

After bonding process, the resized wafer is thinned to 67µm and since the diameter of the vias is about 5.3µm, the aspect ratio of the via is larger than 12:1. Finally, the sample is electroplated in a fountain type Cu electroplating machine and uses the DC power supply, standard electroplating solution for via filling.

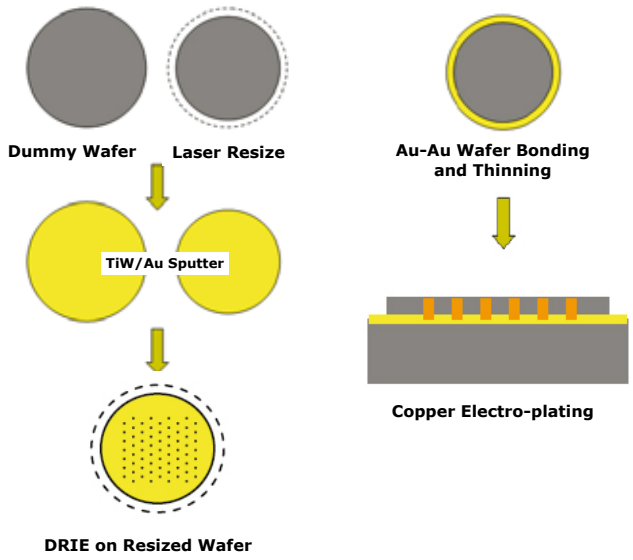


Figure 2 - Process flow for bottom-up Cu electroplating.

The SEM picture of the crossection after bottom-up Cu electroplating is shown in Fig. 3. All the vias are electroplated from the Au to Au bonded bottom electrode. Generally speaking, the Cu electroplating time for standard TSV process showed in Fig. 1(a) is usually 3 to 12 hours [6]. It also needs expensive MOCVD for Cu seed layer and slow etching rate in DRIE process for smooth sidewall roughness. Via shape also plays an important role in standard TSV process, because the tapered via shape with smaller opening at the surface is very hard for conformal void free Cu electroplating. High performance electroplating machine and special designed electroplating solution is also needed.

In our proposed bottom-up TSV structure, it takes only 1.5 hours for A.R. > 12 TSV formation. With the bottom-up electroplating mechanism, it is independent with via shape or sidewall scallop from the DRIE process. In our experiment, a typical fountain type DC electroplating machine with a general commercialized electroplating solution is used.

After the TSV formation process, the reliability of the vias is evaluated by thermal shock test. The purpose of the reliability test is to evaluate the vias fabricated by bottom-up electroplating and the thermal shock test is adopted since it provides more strict conditions and cost less time compared with thermal cycling test. We follow the JEDEC standard JESD-A106B condition C for this reliability test. Temperature ranges from -55°C to 125°C, dwell time in 5min. and the transfer time is less than 3min. After 1000 cycles test, there is no damage, crack or de-lamination on the via side wall. All the failures come from the metal peeling of the RDL (Re-distribution layer) at the surface of the chip.

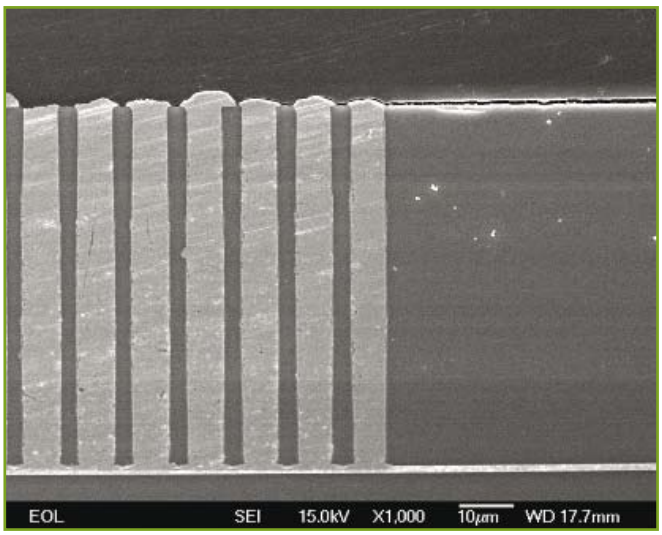


Figure 3 - SEM Picture of A.R. > 12 (Via diameter: 5µm).

Fig. 4 demonstrates the yield of the Bottom-up electroplated vias is very high. From the top view in Fig. 4(a), all the vias are electroplated successfully and the electroplating uniformity is less than 10% within a 6 inch wafer. From the angle view in Fig. 4(b), all the vias are filled from the bottom electrode and it is definitely void free. There are some over plated copper which could be eliminate either by process control or by post CMP(Chemical Mechanical Polish) or mechanical grinding process.

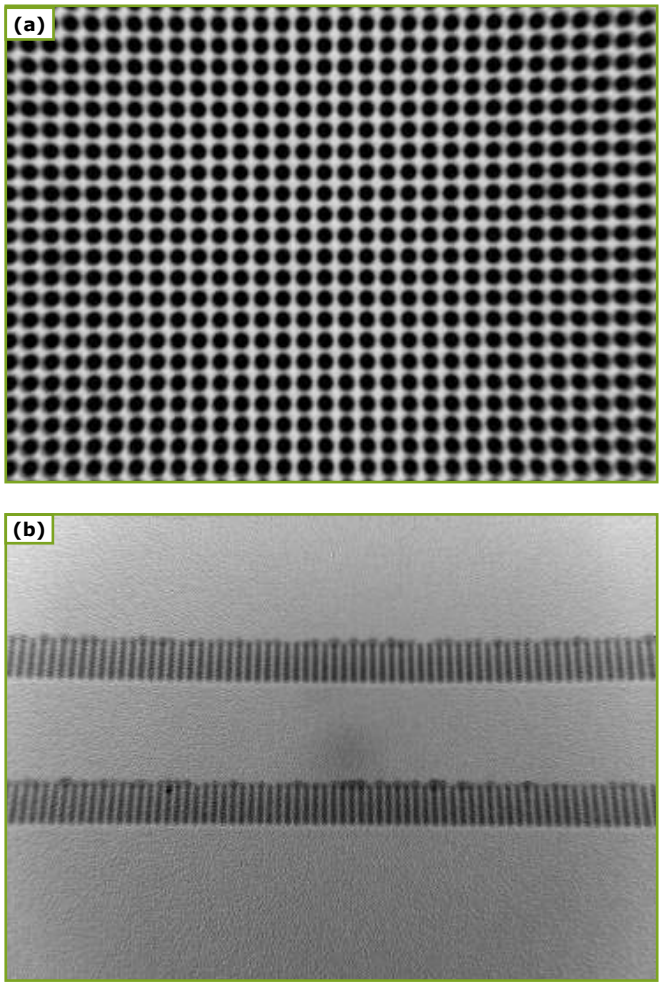


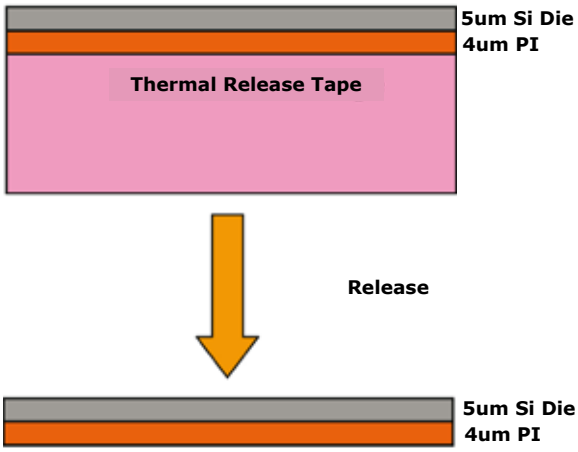
Figure 4 - X-Ray image of Bottom-up electroplated TSVs: (a) Top view X-Ray image of TSVs, (b) Angle view X-Ray image of TSVs.

WAFER THINNING TECHNOLOGY

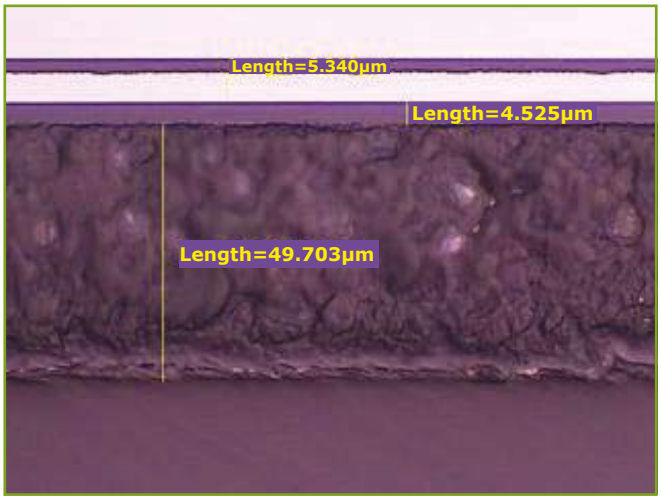
After the TSV fabrication is usually followed by the wafer thinning process. Mechanical grinding is generally adopted to thin the wafer down to 50µm or even 25µm in an 8 inch wafer without carrier substrate. The thickness of the wafer should be less than the length of the fabricated TSVs. For 3D IC process integration, grinding process is usually not the final process. In this case, we need a handling substrate to support the wafer after thinning. Besides, there are still many processes need to apply on the thinned wafer. Some processes with high temperature such as PI process or BCB process; some processes with chemical solutions such as solvent, acid or alkaline solution. We need to choose a suitable temporary bonding material for thin down process and the following high temperature or chemical processes.

There are many materials available for temporary bonding. Thermal-plastic materials have high chemical resistance and temperature stability, and are widely used in 3D IC temporary bonding today [7]. Because it needs equipment for thermal-plastic type material de-bonding, here we use thermal release tape to substitute it. Fig. 5(a) is the process flow for wafer thinning down to 5µm in a 6 inch wafer. First of all, the PI is spin coated on the 6 inch wafer as solder mask and cured at 250°C. Then the wafer is bonded to the handling substrate with the thermal release tape. For the void free and good adhesion needs of bonding, the process is done in a vacuum environment and bonding temperature is raised to 60°C. Since the de-bond temperature of the thermal release tape is 170°C, all the process temperatures after bonding should below this temperature.

After bonding the wafer to the handling substrate, the wafer is thinned down to 25µm with TTV < ±1µm. Then we apply the plasma for further wafer thin down. Finally, the wafer is thinned down to 5µm without crack. From Fig. 5(b), the thickness of the wafer is about 5.3µm, the thickness of the PI is 4.5µm and the thickness of the release layer is about 50µm.



(a) Wafer Thinning Structure



(b) Crossection for Thinned Wafer

Figure 5 - Wafer Thinning Technology.

The wafer is diced to 5mmx4mm shown in the left side in Fig. 6. To release the 5µm ultra thin chip from the handling substrate, we simply place the chip on the hot plate setting at 180°C. After releasing the chip from the thermal release tape, the chip warps seriously. This is because the CTE mis-

match between Si and PI.

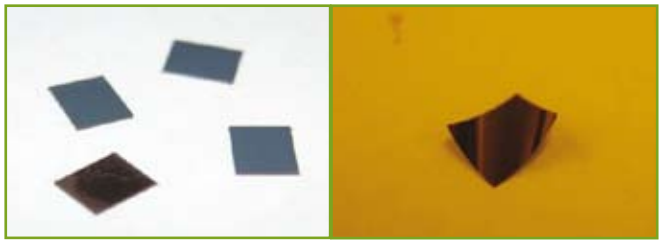


Figure 6 - 5µm ultra thin chip after release.

METAL TEMPORARY BONDING

Although thermal release tape is very simple to use and do not need the de-bonding equipment, the temperature for further process integration is limited within 170°C. For some important 3D IC process such as PI, BCB or CVD process, the process temperature is usually over 250°C. Chemical resistance is another issue for using thermal release tape as temporary bonding material. The thermal release tape peels very quickly in some kind of acid solutions.

Metal temporary bonding is proposed in this research for 3D IC integration. Au is selected as our metal temporary bonding material since our bottom electrode is made by Au. The advantage of Au metal temporary bonding is high temperature stability up to thousands of Celsius degrees and it also has excellent chemical resistance. By using the metal temporary bonding technology, we could put the bottom-up electroplated TSVs to real process integration.

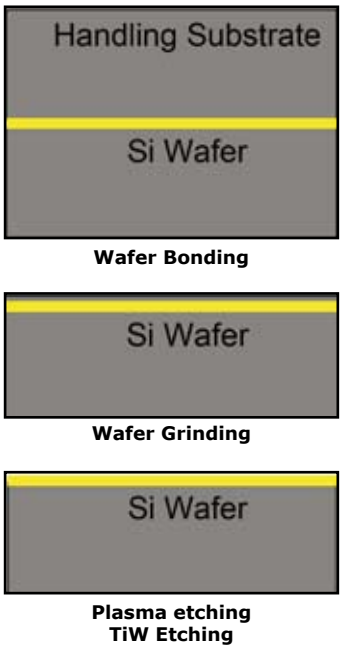


Figure 7 - Metal Temporary Bonding Process Flow.

Fig. 7 illustrates the structure for metal temporary bonding. First of all, TiW/Au is sputtered on both surface of handling substrate and Si wafer. Followed by the plasma activation process and bonding process. Then the Si wafer is backside thinned to desired thickness. By using the Au metal temporary bonding and the wafer thinning technology mentioned above, we could perform high temperature process, chemical or etching process on it. When all the process is finished on the thin Si wafer, we can perform the de-bond process as shown in Fig.7.

The handling substrate is thinned to less than 25µm by grinding machine as first step. Then the 25µm handling substrate is removed by plasma etching. The Au on the Si wafer could be removed by wet etching. Fig. 8 shows the wafer de-bonds by metal temporary bonding. The left figure demonstrates the surface before TiW etching and the figure at the right hand side is after TiW wet etching.

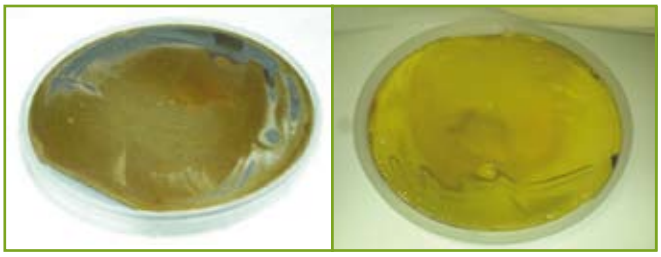


Figure 8 - Wafer de-bond by metal temporary bonding.

If the device wafer is thinned below 300µm and very hard to de-bond directly, it is recommend to use the thermal release tape for assistance. Since all the processes are finished before de-bonding, thermal release tape is suitable as handling material. Before handling substrate thinning, we attach another handling substrate under the thinned Si wafer for support and the rest of the process flow for de-bonding are all the same.

3D IC PROCESS INTEGRATION

There are many advantages to fabricate the TSVs by bottom-up process :

- independent of the via shape of DRIE;
- we could apply high etching rate with large scallop;
- expensive MOCVD process is not needed in high aspect ratio seed layer deposition;
- the vias could be void free filled with traditional fountain type electroplating machine and commercialized electroplating solution.

The most important thing is that it is definitely void free and the electroplating time is very short compared with the standard TSV electroplating process.

Of course there are some disadvantages to fabricate the TSVs by bottom-up electroplating. We need the additional wafer bonding process; more complex process flow for process integration. By using the wafer thinning technology and the metal temporary bonding technology, we could put the TSVs made by bottom-up electroplating to real process integration.

Fig. 9 demonstrates the process flow for 3D IC process integration by using the TSVs fabricated by bottom-up electroplating. From the process flow, we could do the chip stacking experiment. The interconnection is done by Cu/Sn bonding.

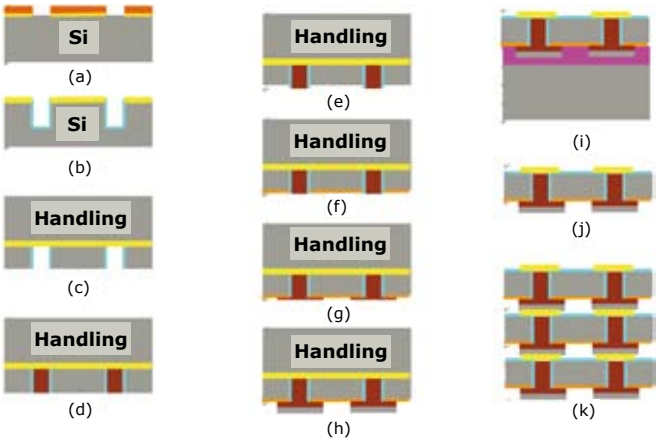


Figure 9 - Process Flow for 3D IC Integration.

The detailed process flow are listed below, we can divide the processes in three main parts, fist one is via formation (a~d), the second part is bumping process (e~h) and the last part is de-bonding and chip stacking process (i~k).

(a) The Si wafer is resized by laser cutting from a standard 6 inch wafer to 140mm in diameter. This is done in a 355nm laser and the process time for each wafer is less than 30min. The main objective of the laser resize is to expose the contact ring for bottom electrode during bottom-up electroplating. TiW/Au is then sputtered on both handling substrate and the resized Si substrate, then the photolithography process is performed for the via opening.

(b) is the DRIE process and the CVD SiO_2 insulation process. Since the etching mask of the DRIE is the PR, the under cut during Au wet etching in step (a) do not affect the via diameter.

(c) is the Au to Au bonding and thinning process. N_2 atmospheric plasma is used for surface activation which could lower the bonding temperature and increase bonding strength as well. Plasma treatment time is about 150sec. with 250W to 400W. Au to Au bonding is finished at 200°C, 30min. Pull test shows the bonding strength is larger than 30MPa and it is sufficient for the following grinding steps. The wafer is then thinned down to 50µm with TTV < ±1µm for via exposure.

(d) is the via filling process. There are many ways for better wetting condition, for example the ultrasonic treatment, plasma treatment or high pressure flow to force the wetting inside the vias. Since the Si wafer is resized to 140mm in diameter, the bottom electrode ring (TiW/Au) is exposed for machine electrode contact. Generally speaking, the uniformity for the traditional fountain type electroplating machine is less than 10% within the whole wafer. After bottom-up electroplating process, there are some over-plated Cu due to the uniformity issues. A grinding or CMP step can remove the over-plated Cu easily and the wafer thickness reduced to about 45µm. Process steps from (a) to (d) mentioned above describes the TSVs formation procedure.

Step (e) to (h) describes the bumping process. After the grinding or CMP process, we apply the plasma to remove the residue stress from grinding or CMP. The thickness of the wafer is removed about 5µm in this process (e).

(f) is the backside insulation process, PI or BCB could be used here. After the PI or BCB process, the RIE is performed to expose the vias.

(g) is the RDL process if needed.

(h) is the bumping process. In our stacking structure, Cu/Sn interconnect is used. The Sn bump is fabricated by electroplating. Because the bump is just at the top side of the TSVs, a mask-less electroplating is suitable here for low cost issue. This can save a photolithography process for Sn electroplating. The electroplating current comes from the power supply, goes through the bottom electrode and the TSVs, the Sn bump is electroplated without mask finally. Fig. 10 shows the mask¬less electroplated Sn bump. From the top picture, we can see the Sn bump is electroplated uniformly and the yield is very high. The bump height is measured about 6µm. An enlarged picture is shown at the bottom, the grain size is very big and this do not affect the interconnect result. In our experiment, the backside insulation process is skipped due to the equipment problem.

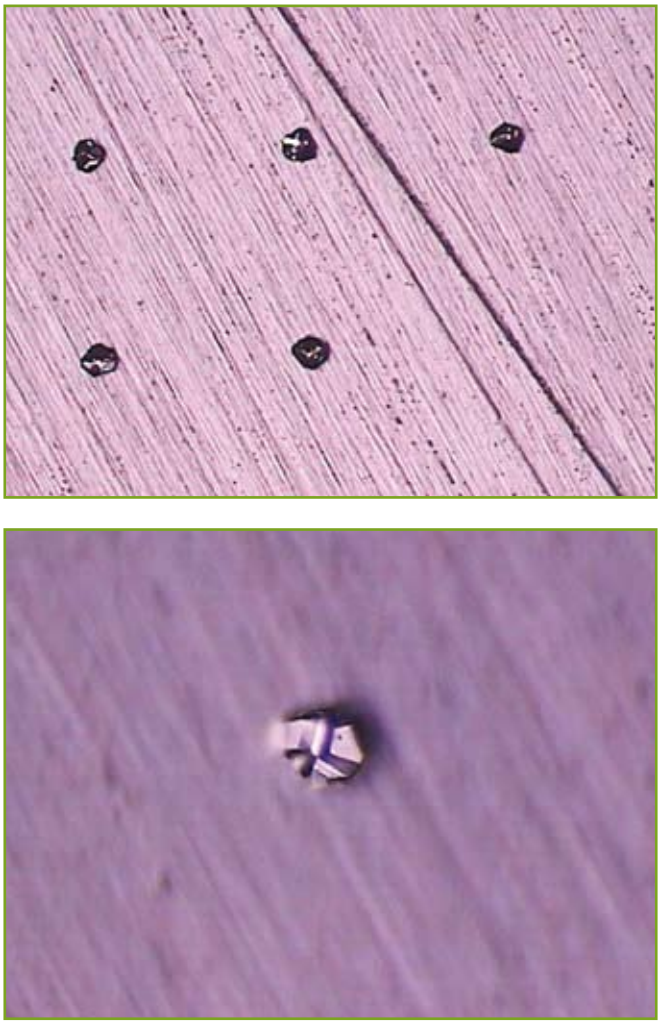


Figure 10 - Mask-less Sn electroplating.

Process (i) to (k) illustrates the handling and the chip stacking procedure. After the bumping process is the metal temporary bond release. Since the thickness of the Si wafer is

about 60µm and is very hard to handle, we use the 170°C thermal release tape for thin wafer handling material. The bonding conditions had been discussed before and the handling substrate is released by the metal temporary bonding technology.

After die saw and release process, we can get the chip that is ready for stacking (j). Release method is the same as the wafer thinning technology described before. Because the chip thickness is about 40µm, it is much easier to release it from the thermal release tape compared with 5µm chip. Fig. 11 shows the crossection of the chip. The diameter of the vias is 10µm and the chip thickness is about 40µm.

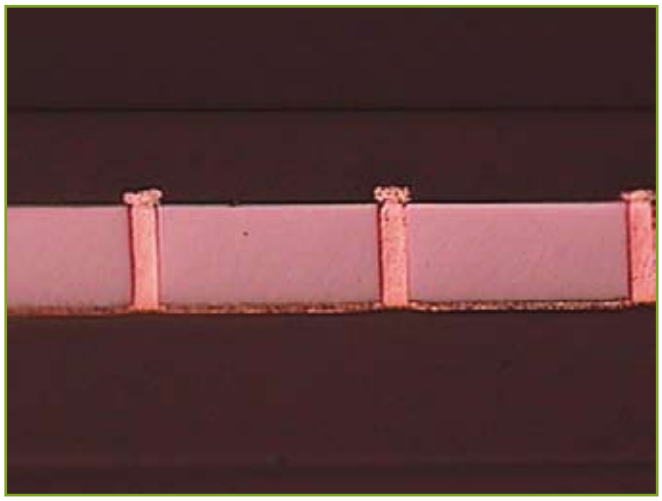


Figure 11 - Crossection of chip.

In our experiment, the bottom electrode after metal temporary bonding is served as bonding pad. Therefore, this metal layer won't be removed. (k) is the die bonding process. There are two ways for chip stacking. The first one is to stack the chip one by one. It takes time to raise the temperature for bonding and also takes a lot of time for cooling. There is no problem for the machine to pick up the chip with 40µm in thickness. Some flux is added manually by brush. Because the spacing between each layer is less than 6µm, there is no under fill dispensed between each layer. **SET FC150 Die Bonder** is used here with alignment accuracy within ±1µm. The bonding temperature is 240°C and the bonding force is about 1Kg, total bonding time is about 3min. Because the upper bonding pad is made by Au, oxidation problem during the high temperature bonding process is not as serious as that of copper pad.

The second way for chip stacking is one reflow process after all the chips are stacked. Die bonder picks up the chip with flux, align and place the chip at the designed position. The chip will stick at the position by flux. After all the chips are aligned and placed at the designed position, the temperature is raised to the bonding temperature. All the interconnection bumps reflowed at one time. The bonding force, bonding time and temperature are the same as the first way. For the throughput concern, the second way is recommended since it has only one temperature cycle and cost much less time. But the yield is an issue for the second way. If the flux does not actually stick the placed chips, the bonding process would fail. Also, the second bonding may probably shift the first layer a little bit.

Fig. 12 is the X-Ray image of 4 layer stacked chips by the second way. Pick and place the 4 chips and perform the bonding process at one time. By the x-ray image, we can understand that the bonding accuracy is acceptable and the shadows beside the vias are come from the flux.

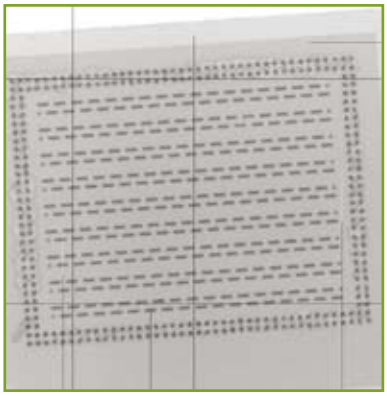


Figure 12:
X-Ray image of 4 layer stacked chips.

Fig. 13 demonstrates the crossection image of 4 layer stacked chips, all the vias are connected by the mask-less electroplated Sn. The total thickness of the 4 stacked chips is less than 160µm.

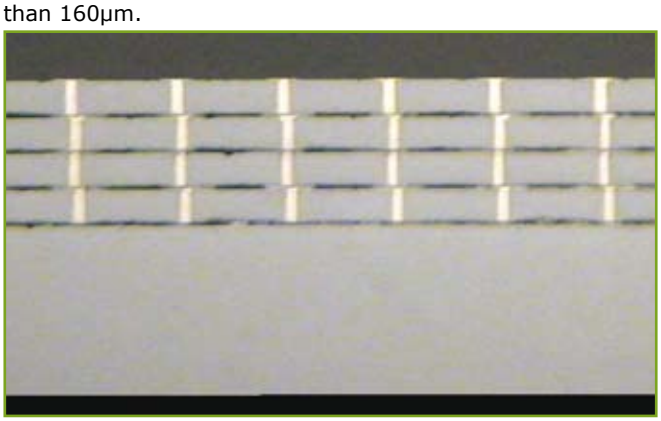


Figure 13 - Crossection of 4 layer stacked chips.

Figure 14 - Cu/Sn Bonding Interface.

Cu/Sn interconnection SEM picture is shown in Fig. 14. The Cu3Sn at the interface is confirmed by EDX inspection. If we apply the first way to stack the chips one by one, the alignment accuracy after bonding would be better, but it costs much longer time for bonding process.

CONCLUSIONS

A TSV fabrication method with aspect ratio larger than 12 by bottom-up electroplating process is proposed and demonstrated in this paper. It has the advantages for lower seed layer deposition cost, shorter electroplating time, independent with the via shape, higher etching rate and the yield is very high from the x-ray image. By using the wafer thinning technology and the metal temporary bonding technology mentioned in this paper, the 3D stacked chip technology using bottom-up electroplated TSVs is also demonstrated.

In wafer thinning experiment, plasma is used for further reduce the wafer thickness after mechanical grinding down to 5μm in thickness in a 6 inch wafer. After dicing the wafer, the chip with 5μm thickness is successfully released from the 170°C thermal release tape.

Metal temporary bonding provide an alternative choice for temporary bonding field with high temperature stability up to thousands of Celsius degrees and excellent chemical resistance.

Four layers chip stacking with one reflow process is also demonstrated in this paper. The total thickness of the 4 stacked chips is less than 160μm and the Cu/Sn interconnection is used here.

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REFERENCES

1. F. Roozeboom et al., "3D Passive and Heterogeneous Integration Technology Options for System-in-Package," IEEE Workshop on 3D integration, Oct. 1-2, 2007, Munich, Germany (Invited).

2. Timothy S. McLaren and Yung-Cheng Lee, "Modeling and Evaluation Criterion for Thermocompression Flip-Chip Bonding," Transactions on Advanced Packing, VOL. 23, NO. 4, NOVEMBER, 2000.

3. C.F. Luk, Y.C. Chan and K.C. Hung, "Development of Gold to Gold Interconnection Flip Chip Bonding for Chip On Suspension Assemblies," Electronic Components and Technology Conferenc, 2001.

4. J. Charbonnier, D. Henry, F. Jacquet et al., "Wafer Level Packaging Technology Development for CMOS Image Sensors Using Through Silicon Vias", CEA-LETI, Electronics System-Integration Technology Conference, 2008.

5. H. H. Chang, Y. C. Shih, C. K. Hsu, Z. C. Hsiao, C. W. Chiang, Y. H. Chen, and K. N. Chiang, "TSV Process Using Bottom-up Cu Electroplating and its Reliability Test", Electronics System-Integration Technology Conference, 2008.

6. M. Jürgen Wolf, Thomas Dretschkow, Bernhard Wunderle, Nils Jürgensen, Gunter Engelmann, Oswin Ehrmann, Albrecht Uhlig, Bernd Michel, Herbert Reichl1, "High Aspect Ratio TSV Copper Filling with Different Seed Layers", Electronic Components and Technology Conference, 2008.

7. A. Jouve, S. Fowler, M. Privett, R. Puligadda, D. Henry, A. Astier, J. Brun, M. Zussy, N. Sillon, J. Burggraf, S.Pargfrieder, "Facilitating Ultrathin Wafer Handling for TSV Processing", Brewer science, Inc., CEA-LETI, EV Group, Electronics Packaging Technology Conference, 2008.

8. Kenji Takahashi, Yuichi Taguchi, Manabu Tomisaka, et al., "Process Integration of 3D Chip Stack with Vertical Interconnection," Electronic Components and Technology Conferenc, 2004.

9. C. A. Bower, D. Malta, D. Temple, J. E. Robinson, P. R. Coffman, M. R. Skokan and T. B. Welch, "High density vertical interconnects for 3-D integration of silicon integrated circuits," Electronic Components and Technology Conferenc, 2006.

10. Masahiro Sekiguchi, Hideo Numata, Ninao Sato, Tatsuhiko Shirakawa, Mie Matsuo, Hiroshi Yoshikawa, Mitsuhiko Yanagida, Hideo Nakayoshi and Kenji Takahashi, "Novel Low Cost Integration of Through Chip Interconnection and Application to CMOS Image Sensor," Electronic Components and Technology Conferenc, 2006.

11. W. C. Lo, et al., "Development and Characterization of Low Cost Ultrathin 3D Interconnect," Proc 55th Electronic Components and Technology Conf, 2005, pp. 337-342.

12. Lu, S. T., Lin, Y. S., and Huang , Y. C., "Low Temperature Bonding of Au-Au in Non-vacuum Environment Using Surface Activated Method", Pan Pacific Microelectronics Symposium, 2004, pp. 87-92.

13. Wei-Chung Lo, Shu-Ming Chang, Yu-Hua Chen, Jeng-Dar Ko, Tzu-Ying Kuo, Hsiang-Hung Chang, Ying-Ching Shih, "3D Chip-to-Chip Stacking with Through Silicon Interconnects", VLSI Technology, 2007.

Study of 15µm Pitch Solder Microbumps for 3D IC Integration

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ABSTRACT

Developments of ultra fine pitch and high density solder microbumps and assembly process for low cost 3D stacking technologies are discussed in this paper. The solder microbumps developed in this work consist of Cu and Sn, which are electroplated in sequential with total thickness of 10µm; The under bump metallurgy (UBM) pads used here is electroless plated nickel and immersion gold (ENIG) with thickness of 2µm. Accordingly, joining of the two Si chips can be conducted by joining CuSn solder microbumps to ENIG UBM pads or CuSn solder microbumps to CuSn solder microbumps. The first joining can only be done with chip to chip assembly whereas the second joining has the potential for chip to wafer assembly. Assembly of the Si chips is conducted with the **FC150 flip chip bonder** at different temperatures, times, and pressures and the optimized bonding conditions are obtained. After assembly, underfill process is carried out to fill the gap and a void free underfilling is achieved using an underfill material with fine filler size.

INTRODUCTION

To meet Tera-scale computing needs and to reduce power consumption for next generation information devices, short and high density interconnections between high-capacity memory chips and micro processor unit are required [1]. Advanced semiconductor circuit designs can contain more than 100 million circuits with interconnection densities in the range of 10^6 to 10^8 cm^{-2} [2]. Fine pitch solder microbumps are one of the key elements to form the high density interconnections with low cost. They are applicable in different advanced packaging technologies, from wire bonded chip stacking to chip stacking with through silicon vias (TSVs), from system in package (SiP) to 3D IC integration [3]. As a result, solder microbumps have attracted lots of attentions. In order to achieve interconnections with low resistance, most frequently used solder microbumps are made up of Cu and Sn. As to the assembly, different metallurgical bonding processes have been developed, such as solid-liquid-interdiffusion method [4] and thermal compression method [5, 6]. In IBM, S. L. Wright et al developed solder micro bumping technology (called C4NP). Different solder materials, such as e-PbSn and CuSn systems, have been studied. It was found that with good Ni barrier structures, CuSn bumps may have electromigration (EM) lifetimes similar to or greater than eutectic PbSn bumps [7, 8].

In this work, both CuSn solder microbumps and ENIG UBM pads with pitch as fine as 15 µm are fabricated on the 8" Si. Assembly of the Si chips is conducted with a SET FC150 flip chip bonder if the joining is formed between CuSn solder microbump and the ENIG pads; whereas if the joining is formed two CuSn solder microbumps, the two Si chips are temporally joined on FC150 first and then reflowed in a reflow furnace. In both cases, optimized bonding conditions are obtained and good joining without voids has been achieved.

PACKAGING STRUCTURE

Figure 1 shows a schematic drawing of 3D chip stacking. According to [1], chip 1 could be a memory chip whereas chip 2 could be a central microprocessor unit or logic chip. Solder microbumps are used to assemble these chips together. As mentioned, there are two types of solder joints discussed in this paper. First, the micro joints are formed between CuSn solder micro bump and the ENIG UBM pad; the second type is CuSn solder microbump joining to CuSn solder microbump. The designed pitch for both solder microbumps and the UBM pads are 15 µm. After assembly of the Si chips, they are joined onto a package substrate with a redistribution layer. The main focuses of this work is to demonstrate fabrication of CuSn solder microbumps and ENIG UBM pad and assembly processes.

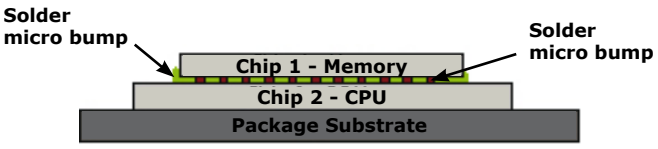

Figure 1 - Schematic drawing of 3D stacking of Memory+CPU package architectures [1] (not in scale).

DESIGN AND FABRICATION OF SOLDER MICROBUMPS

Figure 2 shows the process flow for fabrication of CuSn solder microbumps. The CuSn solder microbumps are fabricated on both of the Si chips at wafer level by electroplating method. The total thickness of the Cu and Sn are 10µm.

In order to achieve reliable joining, Sn solder must be thick enough so that after reflow, there is still pure Sn left for joining. As after 1 time reflow, the formed Cu_6Sn_5 intermetalic compound (IMC) thickness is about 1.5µm [9]. Therefore, it

is better to have the Sn layer thicker than 1.5µm. However, if Sn layer is too thick, sidewall wetting will happen, which results in dewetting issue because of shortage of Sn solder on top of the Cu pillar, or leads to bridging between the adjacent joints due to the ultra fine pitch. Either of these can damage the assembly. In this work, the Sn thickness varies between 1.5µm to 4µm.

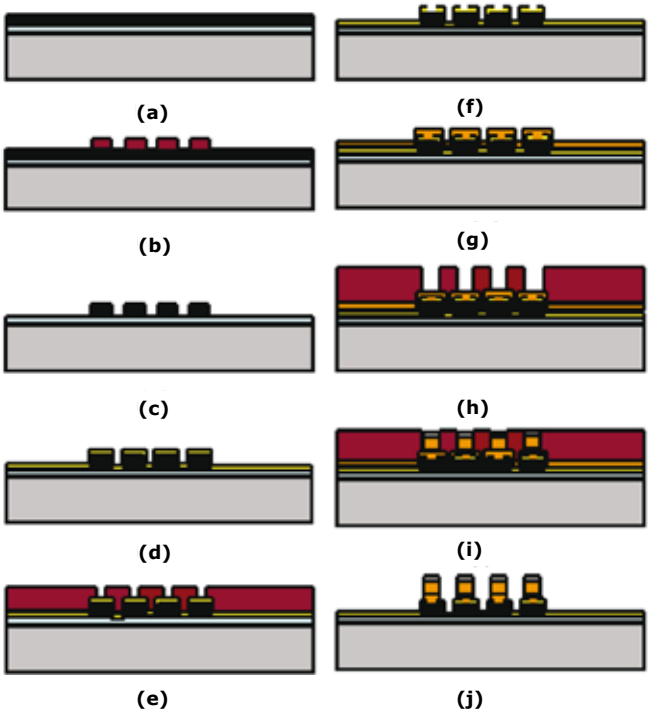

Figure 2 - Process flow for fabrication of CuSn solder microbump.

As shown in the fabrication process flow of Fig. 2, first, layers of SiO_2 and Al film with 1µm thick are deposited on the wafer (Fig. 2 (a)). Then a layer of 2µm thick photoresist is spin coated and patterned (Fig. 2 (b)). Then Al is etched to form the metal pad and the photoresist is removed (Fig. 2 (c)). Another passivation layer is deposited and patterned (Figs. 2 (d), (e) and (f)). Then Ta/Cu of adhesion layer and seed layer are sputtered. The thickness of Ta and Cu is 1000A and 500A, respectively. (Fig. 2 (g)). Then a thick layer of photoresist is coated and patterned as plating mold (Fig. 2 (h)). CuSn is then plated sequentially (Fig. 2 (i)) and the photoresist is stripped. After stripping of photoresist, first the Cu seed layer is etched away with wet etchant, then the Ta layer is dry etched with plasma.

DESIGN AND FABRICATION OF ENIG UBM PADS

For very fine pitch UBM pads, normal UBM metal films, such as TiCuNiAu or AlNiVCu etc, are difficult to pattern with traditional photolithography and wet etching process. Because the under cut caused by the wet etching process can damage the small UBM pads. ENIG formation does not require any high vacuum or photolithography equipments to form the metal stack on top of the bond pads, therefore it is a simple and low cost solution for high density and high pin-count build-up IC packages [10].

Figure 3 shows the process flow for fabrication of ENIG UBM pads. First, a layer of dielectric and Al thin film with 1µm thick are deposited on top of the wafer (Fig. 3 (a)). Then a thin layer of photoresist with 2µm thick is spin coated and patterned (Fig. 3 (b)). After that, the Al layer is etched and the photoresist is stripped (Fig. 3 (c)). After that, another layer of SiO_2 dielectric layer is deposited (Fig. 3 (d)). Then another layer of photoresist is spin coated and patterned (Fig. 3 (e)). Then the dielectric layer is etched to expose the Al pad (Fig. 3 (f)). At last, an Electroless Ni-P plating with 7% of P content and Electroless Au plating are applied to the exposed Al pad. The temperature for Electroless Ni plating is 90°C+/- 5°C (Fig. 3 (g)).

The thickness of the ENIG pad is also limited by the fabrication process. Assuming the plating of ENIG is isotropic [10], and the opening of Al pad (w as shown in Fig. 3) is 4µm, then the relationship between the thickness of the ENIG pads and the width of the ENIG pads (W as shown in Fig. 3) can be described as Fig. 4. From Fig.4, when the thickness of the ENIG pads is selected as 2µm, the width of the ENIG pads will be 8µm. As the pitch size is only 15µm, thicker ENIG pads may easily result in solder bridging of adjacent pads during assembly. Therefore, the ENIG UBM pad thickness is selected as 2 µm in this work.

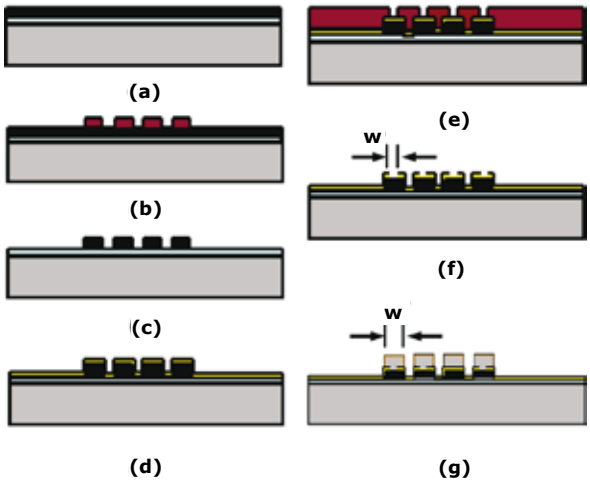

Figure 3 - Process flow for ENIG UBM pad plating.

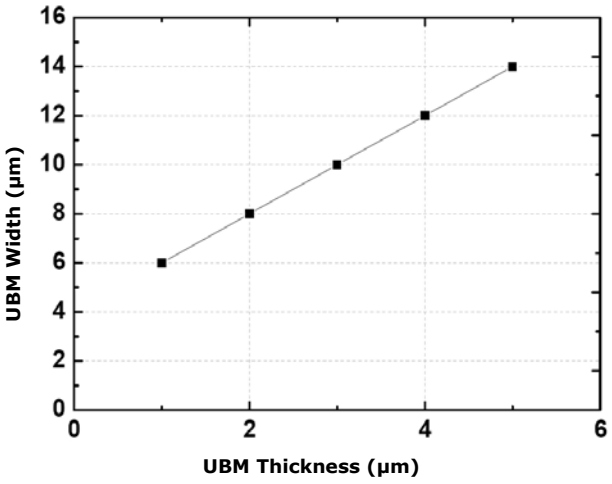

Figure 4 - Relationship between the ENIG UBM thickness and the ENIG UBM width (assuming ENIG plating is isotropic and the opening of the Al pad is 4µm.

FABRICATION RESULTS AND DISCUSSION

A) CUSN SOLDER BUMP FABRICATION RESULTS

In fabrication of CuSn solder micro bumps, most frequently used adhesion layer is Ti and after plating, this adhesion layer is etched away by wet etching method. However, it is found that if Ti is used as the adhesion layer and later etched away by wet etching method, then after wet etching, lots of solder microbumps are lost at the same time, as shown in Fig. 5 (a). The reason is that when using wet etching process to etch the Ti adhesion layer, under cut happens and since the diameter of the bump is only 8µm, most of the solder microbumps peel off. In order to solve this problem, Ta is used here as the adhesion layer and later is etched away with dry etch process. As a result, it can avoid peeling off of the solder microbumps, as shown in Fig. 5(b). Fig. 6 shows Scanning Electron Microscope (SEM) photos of the fabricated CuSn microbumps and Al pad. After plating, a reflow was performed to reshape the micro-bumps and uniform bump heights were obtained. The reflow temperature is 265°C.

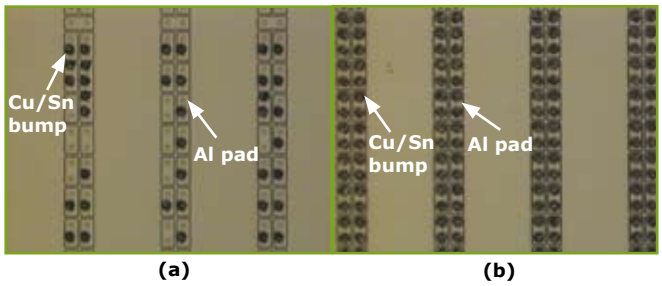

Figure 5 - (a) Fabrication results of Cu/Sn solder micro bumps with Ti used as seed layer and etched away with wet etching, lots of solder micro bump missed after fabrication; (b) Fabrication results of CuSn solder micro bumps with Ta used as seed layer and etched with dry etch process.

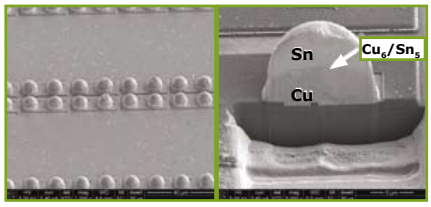

Figure 6: SEM images of Cu/Sn solder microbumps.

B) ENIG PLATING RESULTS

After Al pad formation and passivation opening on the Al pad, an Electroless Ni-P plating with 7% of P content and Electroless Au plating are applied to the exposed Al pad. The temperature for Electroless Ni plating is 90°C ± 5°C. Fig. 7 shows SEM pictures of ENIG on Aluminum electrodes.

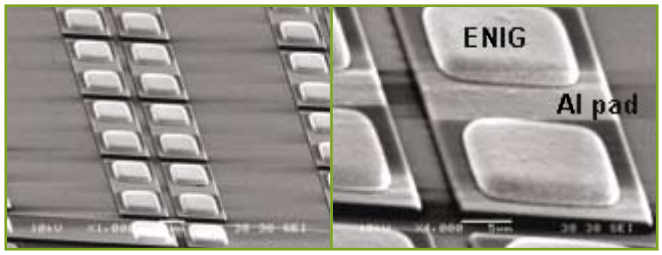

Figure 7 - SEM images of ENIG UBM pads.

ASSEMBLY

After fabrication of the CuSn solder microbumps and the ENIG UBM pads, the Si chips are joined together using FC150 flip chip bonder. The assembly process was a non-flux process because after joining, the gap between the Si chip and the Si carrier is only about 10 ~ 15 µm. Therefore if flux is used, it is very difficult to clean it and then after underfill process, a lot of voids are formed inside the gaps. As mentioned, on the Si chip 2, either ENIG or CuSn solder micro bumps are fabricated. Therefore, assembly are done by either joining CnSn solder microbump to ENIG pad or joining CnSn solder microbump to CnSn solder microbump.

A) ASSEMBLY WITH CUSN SOLDER MICROBUMP AND ENIG PAD

The first assembly is done with CuSn solder micro bump and ENIG UBM pad. The joining conditions are: pressure of 20MPa; bottom substrate temperature of 300°C up arm temperature of 350°C and time of 60 seconds.

Fig. 8 shows cross-section of micro joints with CuSn solder micro bump and ENIG pad jointed together. It can be seen that all the Sn is consumed.

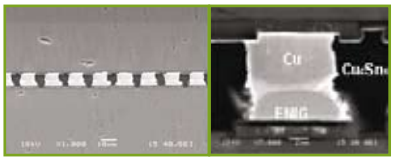

Figure 8: Cross-section of micro joints with CuSn solder micro bump joined to ENIG.

B) ASSEMBLY WITH CUSN AND CUSN SOLDER MICRO BUMPS

When assembly with CuSn solder micro bump and ENIG pad, both the Si chip and the Si carrier have to be kept at high temperature, therefore the joining has to be done one by one with chip to chip assembly.

The second assembly is done with CuSn solder microbump and CuSn solder microbump. The joining conditions are: pressure of 10MPa; bottom substrate temperature is room temperature; up arm temperature of 350°C and time of 30 seconds. This step is only for temporally joining. After that, the assembly is reflowed in a reflow oven with peak temperature of 265°C. Fig. 9 shows the reflow temperature profile used for reflow. Fig. 10 shows the cross-section of micro joints after reflow. It is found that there is still some Sn left.

In this method, the Si chip 2 is kept at room temperature. Therefore it is possible to do chip to wafer assembly, which means pre-joining the Si chip 1 to wafer of Si chip 2 on the SET FC150 bonder first, then do batch reflow at the same time in the reflow furnace.

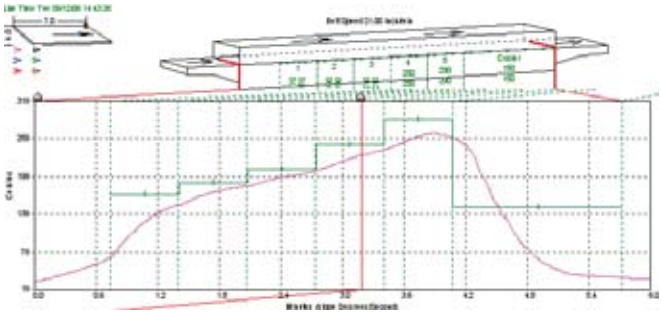

Figure 9 - Reflow temperature profile for final joining between CuSn solder microbumps to CuSn solder microbumps.

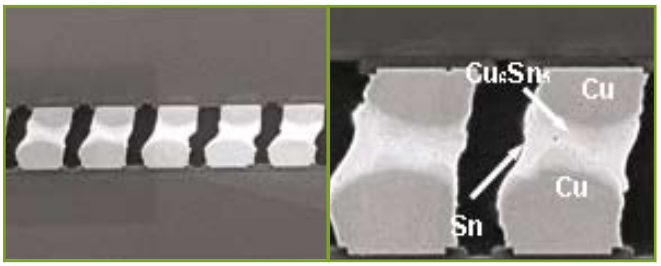

Figure 10 - Cross-section of micro joints with Cu/Sn solder micro bump joined to Cu/Sn solder micro bump.

EVALUATION OF UNDERFILL

As mentioned, the gap between the two jointed Si chips is very narrow; therefore it is important to evaluate the flowability of underfill and the void formation in underfill which contains silica-filler. Considering the fine chip to chip gap, fine filler size underfills were used to evaluate the underfill process. Fig. 11 shows cross-section image of the underfilled sample. It can be that good filling without any void can be achieved with underfill resin containing very fine filler.

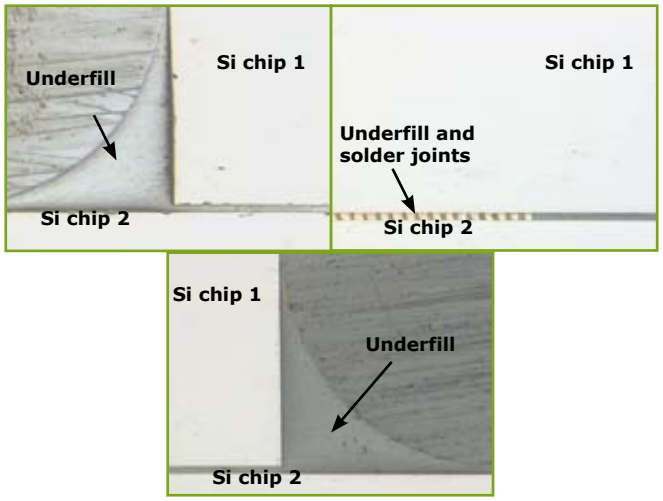

Figure 11 - Optical photo of cross-section of two chips with underfill in the gap.

CONCLUSIONS

The investigations of solder microbumps in 15µm pitch and their assembly process are reported in this paper. The fine pitch solder microbumps can be used for stacking of memory chip and microprocessor chip as well as other 3D systems in package. Some important results are summarized as:

1. For Cu/Sn solder microbumps with 8 µm in diameter and 15 µm in pitch, the thickness of the Sn cap should be thicker than 1.5µm and less than 4µm if the total bump height (Cu + Sn) is kept to 10 µm.

2. It is found that when the Ti is used as adhesion layer, during the wet etching process, lots of bumps are missing because of undercut. Therefore the adhesion layer is changed to Ta and is etched by dry etching process.

3. With optimized bonding conditions (bottom temperature of 300°C and upper temperature of 350°C, 60 second, 20 MPa), good joining can be achieved between CuSn microbumps and ENIG UBM pads.

4. Bonding of CuSn solder microbumps to CuSn solder microbumps (instead of ENIG UBM) also yields good results. The chips are temporally joining together first on the SET FC150 bonder (the joining conditions are: pressure ~ 10MPa; bottom substrate temperature ~ 25°C; upper arm temperature ~ 350°C and time ~ 30 seconds) and then reflowed in a reflow oven with a peak temperature of 265°C. This approach has the potential to perform chip to wafer assembly.

ACKNOWLEDGMENTS

The authors also want to thank Mr. Abdullah Zulkiflee and Ms. Ng Lee Kian from SPT lab and Nanda Su and Michelle Chew Bi-Rong from MMC lab of IME for their help in fabrication of the silicon chips.

REFERENCES

1. L. A. Polka, H. Kalyanam, G. Hu, and S. Krishnamoorthy "Package Technology to Address the Memory Bandwidth Challenge for Tera-scale Computing," Intel Technology Journal, Vol. 11, No. 3, 2007 pp.197-206.

2. J. U. Knickerbocker, P. S. Andry, L. P. Buchwalter, A. Deutsch, R. R. Horton, K. A. Jenkins, Y. H. Kwark, G. McVicker, C. S. Patel, R. J. Polastre, C. Schuster, A. Sharma, S. M. Sri-Jayantha, C. W. Surovic, C. K. Tsang, B. C. Webb, S. L. Wright, S. R. McKnight, E. J, Sprogis and B. Dang, "Development of next-gereration system-on-acage (SOP) technology based on silicon carriers with fine-pitch interconnection," IBM J. Res. Dev. Vol. 49, No. 4/5 (2005), pp. 725-754.

3. K. Sakuma, P. S. Andry, B. Dang, J. Maria, C. K. Tsang, C. Patel, S. L. Wright, B. Webb, E. Sprogis, S. K. Kang, R. Polastre, R. Horton and J. U. Knickerbocker, "3D chip stacking technology with low-volume lead-free interconnections," 57th Proceedings of Electronic Components and Technology Conference, 2007, pp. 627-632

4. H. Hübner, S. Penka, M. Eigner, W. Gruber, M. Nobis, G. Kristen, M. Schneegans, B. Barchmann, S. Janka, "Micro Contacts with Sub-30µm Pitch for 3D Chip-on-Chip Integration," MAM 2006, Grenoble, March 2006.

5. Y. Tomita, T. Morifuji, T. Ando, M. Tago, R. Kajiwara, Y. Nemoto, T. Fujii, Y. Kitayama, and K. Takahashi, "Advanced packaging technologies on 3D stacked LSI utilizing the micro-interconnections and the layered microthin encapsulation," 51st Electronic Components and Technology Conference, 2001, pp. 353-360.

6. K. Takahashi, M. Umemoto, N. Tanaka, K. Tanida, Y. Nemoto, Y. Tomita, M. Tage, and M. Bonkohara, "Ultra-high-density interconnection technology of three-dimensional packaging," Microelectronics Reliability, Vol. 43 2003, pp. 1267-1279.

7. S. L. Wright, R. Polastre, H. Gan, L. P. Buchwalter, R. Horton, P. S. Andry, E. Sprogis, C. Patel, C. Tsang, J. Knickerbocker, J. R. Lloyd, A. Sharma and M. S. Sti-Jayantha, "Characterization of Micro-bump C4 interconnects for Si-Carrier SOP applications," 55th Electronic Components and Technology Conference, 2006, pp. 633-640.

8. H. Gan, S. L. Wright, R. Polastre, L. P. Buchwalter, R. Horton, P. S. Andry, C. Patel, C. Tsang, J. Knickerbocker, E. Sprogis, A. Pavlova, S. K. Kang, and K. W. Lee, "Ph-free micro joints (50µm pitch) for the next generation microsystems: the fabrication, assembly and characterization," 56th Electronic Components and Technology Conference, 2006, pp. 1210-1215.

9. A. B. Yu, A. Kumar, S. W. Ho, W. Y. Hnin, John H. Lau, C. H. Khong, P. S. Lim, X. W. Zhang, D. Q. Yu, N. Su, B. R. Chew, M. C. Jong, T. C. Tan, V. Kripesh, C. Lee, J. P. Huang. J. Chiang, S. Chen, C.¬H Chiu, C.-Y Chan; C.-H. Chang, C.-M. Huang and C.-H. Hsiao, "Development of Fine Pitch Solder Microbumps for 3D Chip Stacking," 10th Electronics Packaging Technology Conference, 9-12, Dec., 2008. pp. 387-392.

10. K. Yokomine, N. Shimizu, Y. Miyamoto, Y. Iwata, D. Love and K. Newman, "Development of electroless Ni/Au plated build-up filp chip package with highly reliable solder joints," 51st Electronic Components and Technology Conf, 2001, pp. 1384-1392.

3D Stacked IC Demonstration using a Through Silicon Via First Approach

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ABSTRACT

We report for the first time the demonstration of 3D integrated circuits obtained by die-to-die stacking using Cu Through Silicon Vias (TSV). The Cu TSV process is inserted between contact and M1 of our reference 0.13µm CMOS process on 200mm wafers. The top die is thinned down to 25µm and bonded to the landing wafer by Cu-Cu thermo-compression. Both top and landing wafers contain CMOS finished at M2 to evaluate the process impact both FEOL and BEOL. The results confirm no degradation of the FEOL performance. The functionality of various ring oscillator topologies that include inverters distributed over both top and bottom dies connected through TSVs demonstrates excellent chip integrity after the TSV and 3D stacking process.

3D-SIC PROCESS

Recently 3D integration has gained a lot of interest due to its potential to alleviate some important performance limitations facing CMOS scaling [1-2]. Different approaches to 3D integration are reported depending on system level requirements [3]. Our 3D Stacked IC (3D-SIC) process [4-5] uses IC foundry infrastructure to create TSVs prior to BEOL processing. The TSV process sequence is summarized in figure 1.

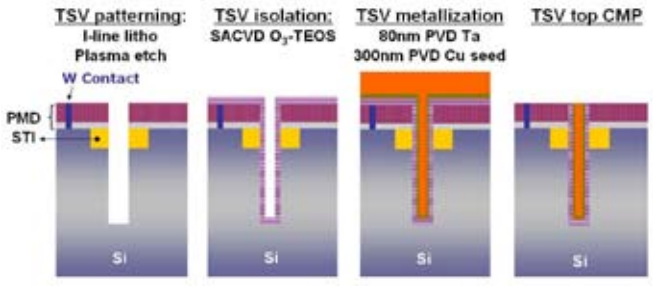
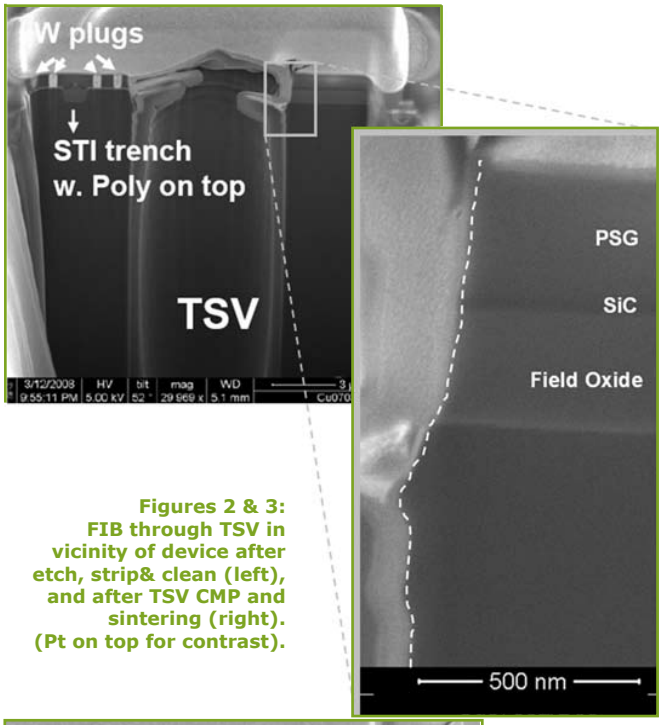
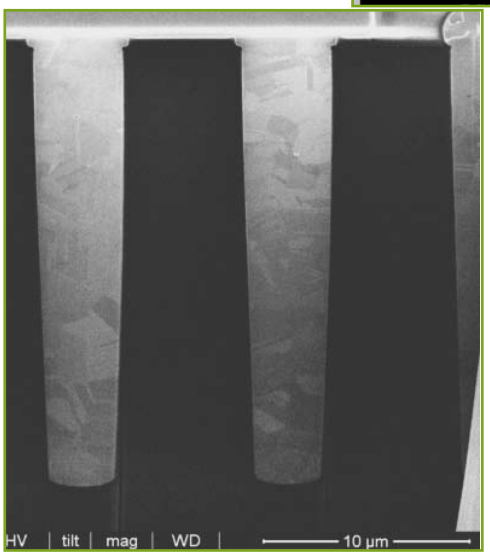


Figure 1 - Schematic of the 3D-SIC Through Silicon Via (TSV) module. Figure 2&3: FIB through TSV in vicinity of device after etch, strip & clean (left), and after TSV CMP and sintering (right). (Pt on top for contrast).

After processing of the CMOS FEOL and the PMD stack, we patterned TSVs with a diameter of 5µm and a pitch of 10µm using a 3µm thick I-line resist. We performed an undercut free, resist-based TSV etch (figure 2); undercut underneath



Figures 2 & 3: FIB through TSV in vicinity of device after etch, strip& clean (left), and after TSV CMP and sintering (right). (Pt on top for contrast).



the contact layer is avoided by pre-deposition of a polymer on the sidewall of the etched PMD/STI stack prior to the Si etch.

For electrical isolation, we deposit a 100nm SACVD O3-TEOS layer. The metallization sequence consists of applying a 80nm PVD Ta barrier and a 300nm PVD Cu seed followed by an ECD via fill using a 3-component plating chemistry. Finally the Cu overburden is polished in a top-side TSV CMP step. After this process, we apply a standard, 2 metal layer BEOL process to finalize the top Si-die. After wafer test, the wafer is mounted on a temporary carrier and thinned down to a Si-thickness of ~25 µm by a combination of grinding and CMP. In this process, the TSVs are exposed on the wafer backside. Next the Si is recessed by dry etching over a distance of ~700nm with respect to the copper TSV. In this work the dies were then stacked by Cu-Cu thermo-compression bonding in a Die-to-Die (D2D) fashion, although compatibility with Die-to-Wafer integration remains. Figure 4 shows a microscope view of the obtained 3D stack.

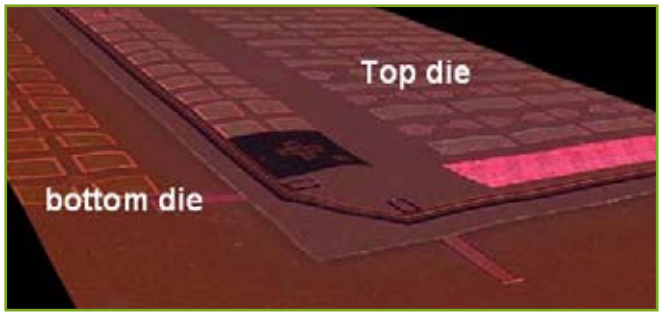


Figure 4 - Optical Micrograph of thinned top die stacked to a bottom die by Cu-Cu thermocompression bonding.

ELECTRICAL PERFORMANCE OF CMOS DEVICE

The impact of the reduction of substrate thickness, TSV integration and the stacking process on the electrical performance of both n- and p-type MOSFETs has been investigated in detail. Parameters like saturation threshold voltages (figure 5), intrinsic transistor performances (figure 6) of both n- and p-type MOSFETs have been monitored at various steps in the 3D-SIC flow.

Particular attention is given to the contacts to the active area and to polysilicon gate to insure the integrity CMOS FEOL after the TSV integration that follows the CMOS contact module (figure 7). Gate leakage was found to be unaffected (figure 8). The impact of grinding on the substrate regions has been evaluated previously [6]. Diode leakage currents, which can be taken as indicators for substrate damage and stress levels resulting from the thinning and stacking process by Cu–Cu thermocompression, do not show significant deviation from the reference performance (figure 9). No major disturbance has been observed on the electrical characteristics of n- and p- type devices for a TSV-device distance larger than 1.5µm (figures 10-12), consistent with the simulations of [7].

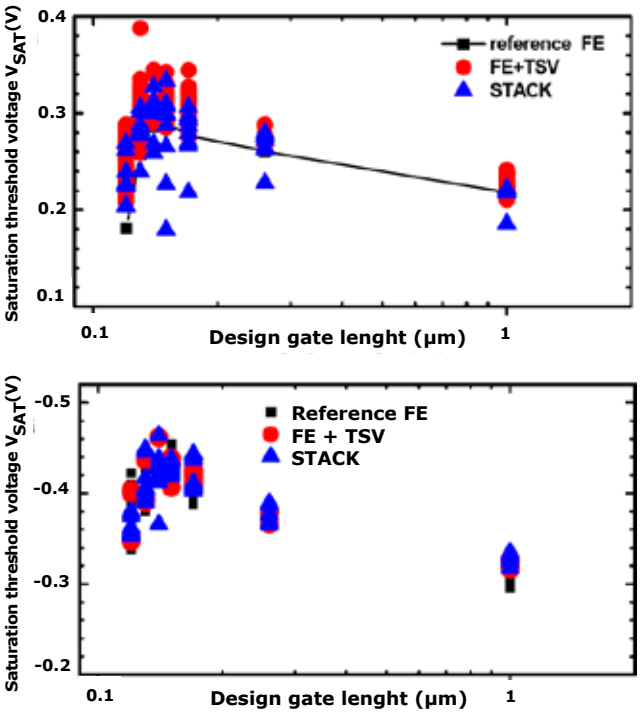


Figure 5 - Comparison of the saturation threshold voltage versus the design gate length for both n- (top) and p-MOSFET (bottom) on reference wafer (REF), a thinned front end wafer with TSVs (FE+TSV) and on top tiers of stacked dies (STACK).

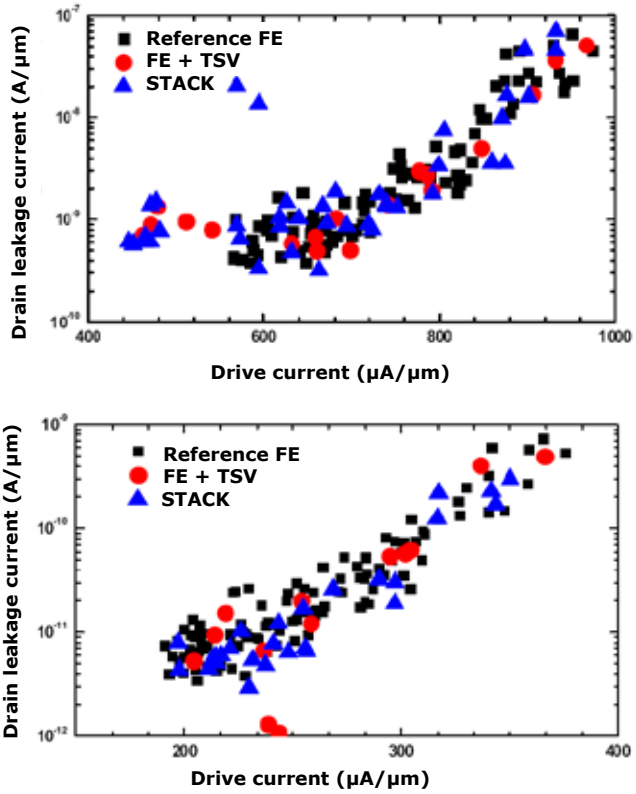


Figure 6 - Comparison of the intrinsic transistor performance for both n- (top) and p-MOSFETs (bottom) on reference wafer (reference FE), a thinned front end wafer with TSVs (FE+TSV) and on top tiers of stacked dies (STACK).

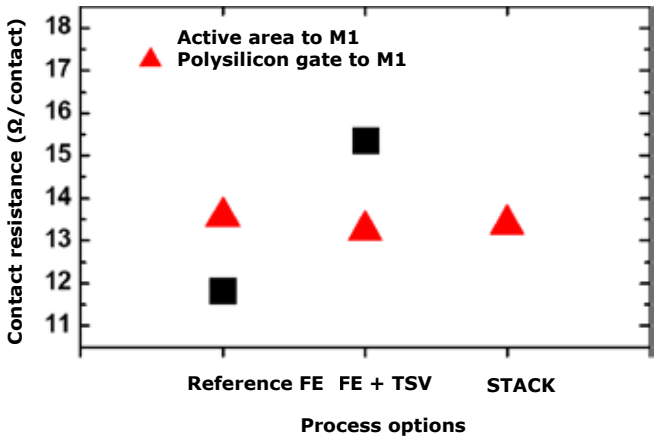
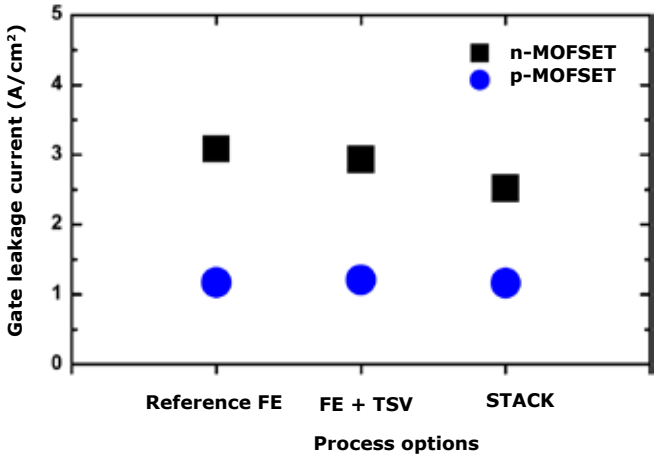
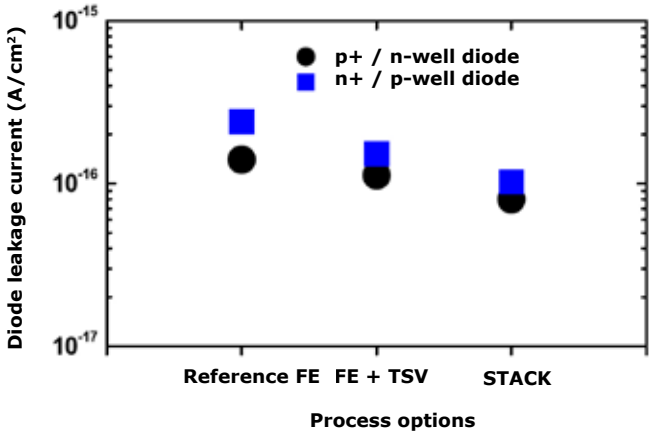


Figure 7 - Contact resistance for M1 toactive area and M1 to polysilicon gate on reference wafer (Ref FE), thinned front end wafer with TSVs (FE+TSV) and on top tiers of stacked dies (STACK).





Figures 8 & 9 - Comparison of the gate and diode leakage currents for both n- and p-type MOSFETs and p+/nwell and n+/pwell diodes on reference wafer (Ref FE), a thinned front end wafer with TSVs (FE+TSV) and on top tiers of stacked dies (STACK).

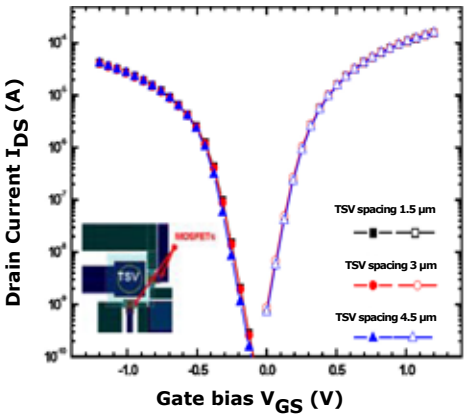
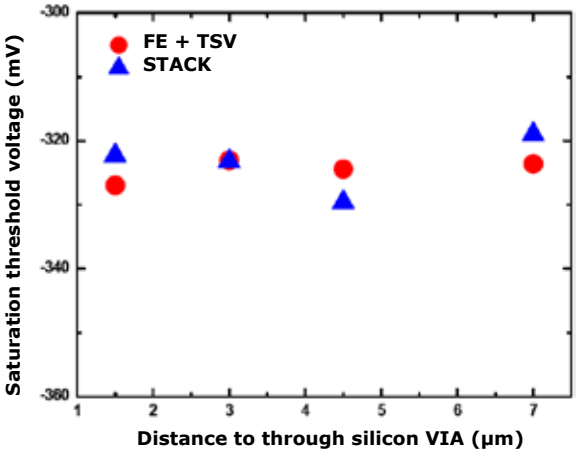
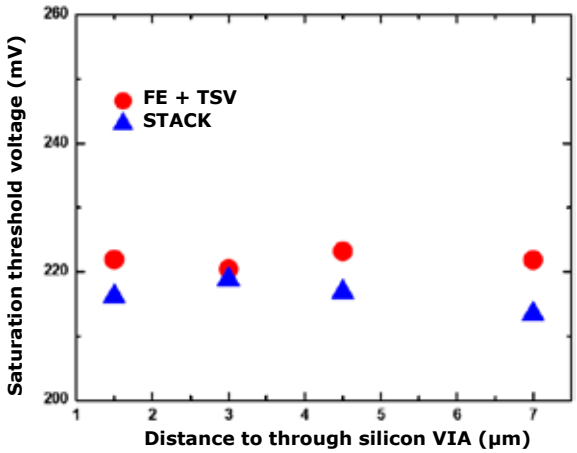


Figure 10 - Drain current versus the gate bias in saturation for both n- and p- type MOSFETs at different distances from a TSV.





Figures 11 & 12 - Comparison of the median saturation threshold voltage for both p- and n-type MOSFETs on a thinned front end wafer with TSVs (FE+TSV) and on top tiers of stacked dies (STACK) at different distances from a TSV.

RING OSCILLATORS

To gauge the performance of FEOL on top and bottom strata along with the TSVs, 41 stages Ring Oscillator (RO) with

varying configurations as shown in figure 13 are designed and fabricated. The FEOL on both top and bottom strata are 7.5µm away from the edge of the TSV (ϕ= 5µm). All ROs are followed by 8 frequency dividers (Divide by 256) and a buffer. RO without any load lying entirely on the bottom strata before stacking (RO_REF_STD) is taken as reference RO. Unloaded RO lying entirely on the top strata (RO_TOP_STD) and entirely on the bottom strata (RO_BOT_STD) measured after stacking have been compared with RO_REF_STD. Hybrid RO with 21 inverters on bottom strata and 20 on the top strata (RO_HYB_HalfBotHalfTop) connected through 2 TSVs at the end of top and bottom inverter chains have been compared with RO with one inverter at the bottom strata and rest of the inverter stages on top strata (RO_HYB_OneBotRestTop). Both designs consist of 2 TSVs interconnecting the inverters on top and bottom strata. Bottom ROs are designed such that they are measurable before as well as after stacking.

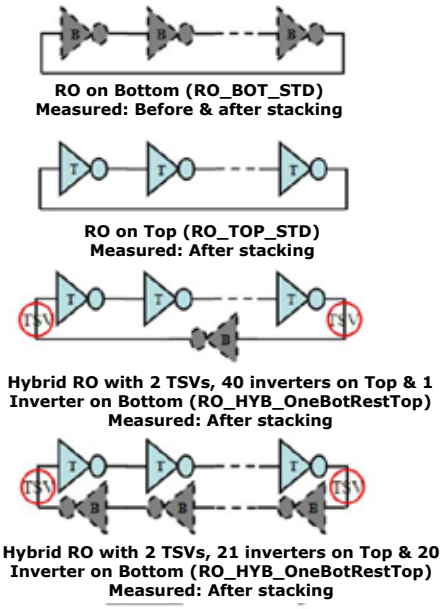


Figure 13 - Ring Oscillator (RO) Configurations.

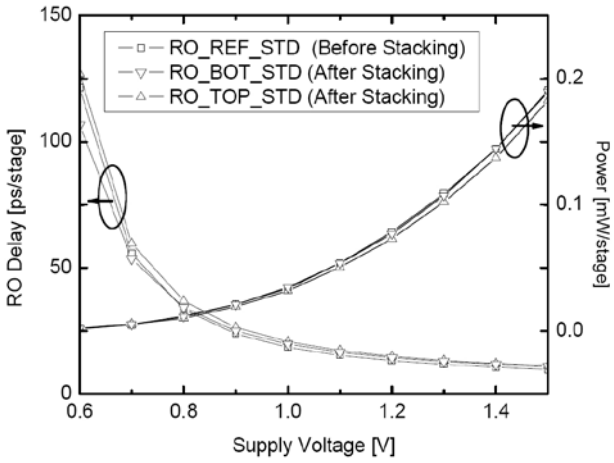


Figure 14 - Delay & Power comparison for Top & Bottom Standard ROs and RO reference.

RO Delay variation and power per stage for RO_TOP_STD and RO_BOT_STD after stacking are compared with the reference RO_REF_STD in figure 14. Both top and bottom ROs show comparable performances when compared to the reference RO. Figure 15 compares the delay variation & power per stage of the hybrid designs with the reference RO_REF_STD. As expected, the 2 TSVs cause larger delay in the ring oscillator operations. Moreover, irrespective of their positions in the design, delay and the power are comparable in both hybrid designs.

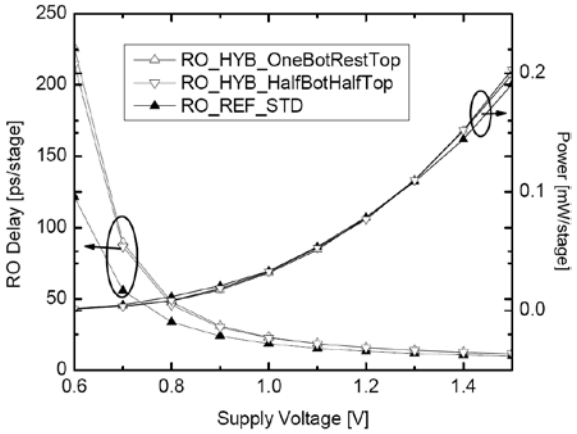


Figure 15 - Delay & Power comparison for Hybrid and reference ROs.

CONCLUSIONS

3D stacked Integrated Circuits with copper TSV First approach and D2D stacking process have been demonstrated. Integrity of top and bottom CMOS FEOL throughout the 3D-SIC flow has been proven. Impact of TSV proximity on active devices has been analyzed. Ring oscillator performance of the top, bottom and hybrid configurations before and after stacking confirm the communication between top and bottom dies interconnected through TSVs.

REFERENCES

[1] E. Beyne, Proceedings of ISSCC2004, pp.138-145.

[2] E. Beyne, Proceedings of the International Interconnect Technology Conference, IEEE – New Jersey, pp. 1-5.

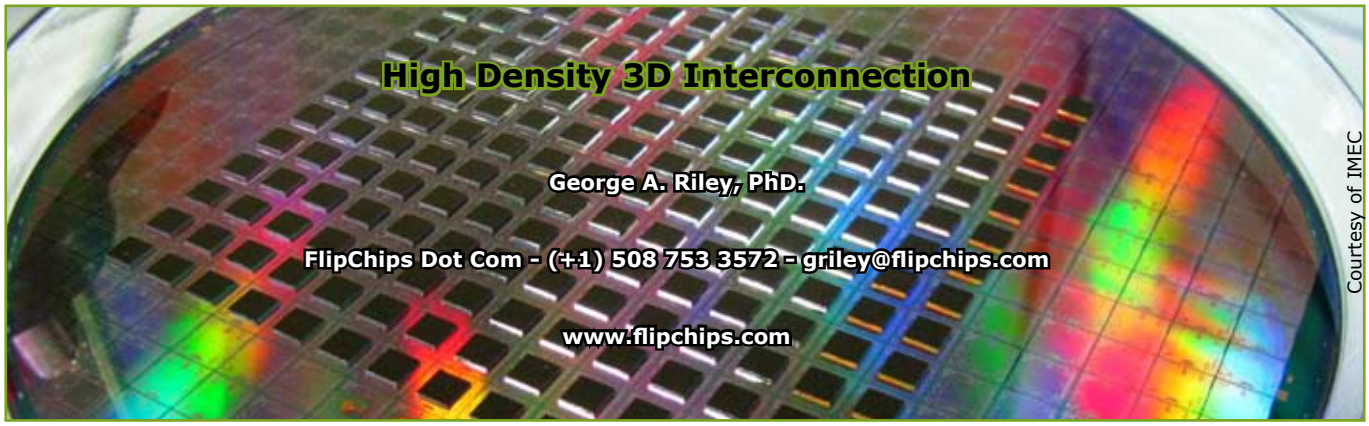
[3] E. Beyne, Proceedings 4th Int. Symp. Microelectron. Packag., Seoul, South Korea,Sep. 28, 2005.

[4] B. Swinnen et al., Proceedings of IEDM2006, pp. 371-374.

[5] A. Jourdain et al.,Proceedings of IITC 2007, pp.

[6] K. De Munck et al., IEEE Electron Device Letters, Vol.29, No.4, 2008.

[7] C. Okoro et al, Proceedings of IITC 2008, pp. 16-18.



High Density 3D Interconnection

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High density die-to-die 3D interconnection has been the moon-landing race of the past decade. As shrinking transistors approach scaling limits, 3D interconnection is a path to higher speed, higher density, lower power consumption, and lower cost. Memory die stacks with wire bonds have been available for years. However, their long interconnection paths slow down signals and consume power. Connection of circuit elements within a die directly to elements within a different die, with heterogeneous integration and partitioning, has been the long-term goal of the decade.

More than 50 companies are involved in some part of this activity. More than a dozen companies are reported to have set up pilot production lines to begin industrializing the laboratory results.

Through-silicon vias (TSVs) are now a proven part of the solution. TSVs are already in use in CMOS imaging arrays and silicon interposers. Finer-pitch TSVs could directly interconnect circuit functions within a die stack. As fine-pitch TSVs move from the laboratory to pilot production, the near-term focus becomes how to best handle, stack, and bond thinned TSV die and wafers.

A wide range of approaches is being investigated. While much early work concentrated on wafer-to-wafer interconnection, the die-to-wafer approach has shown significant advantages. Separately placing each die onto the wafer allows connecting only known good die, so that resources are not wasted. Die-to-wafer assembly readily accommodates heterogeneous mixes of die, including unequal die sizes within a stack. Die-to-wafer alignment distances are far shorter than for wafer-to-wafer alignment, allowing faster placement while reducing wafer coplanarity and thermal expansion concerns.

Wafer-to-wafer bonding has an advantage in throughput, since bonding, a time-consuming process, is simultaneous for all devices. However, advances in die-to-wafer allow all die to be placed and even stacked sequentially onto the wafer, followed by simultaneous bonding.

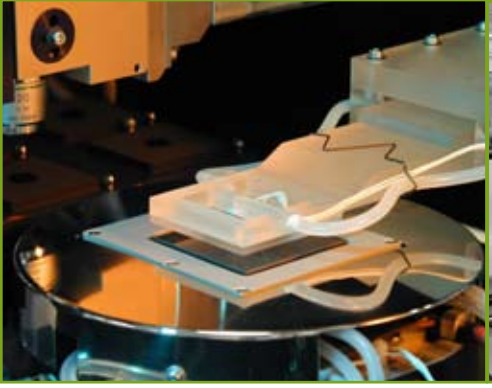
Laboratories focus on making functional devices. Factories focus on making large quantities of functional, reliable devices, at acceptable yields and costs. Open issues delaying the wider production of 3D assemblies include agreeing on common design tools and standards, resolving supply chain issues, and establishing long-term reliability. Simply adding 3D stacks to existing system designs does not take full advantage of 3D efficiencies. System redesigns will be required to take advantage of die-to-die connection and repartitioning. Standards will reduce the many proposed approaches to a reasonable number of common approaches.

The supply chain issue in the production process hinges on where TSVs should be created: at the front end of the line, as part of wafer fabrication; at the back end as part of assembly and test; or in the middle, between wafer fabrication and assembly/test? The location governs not only what fabrication methods may be used, but who will use them -- a wafer fabricator or a packaging house?

The reliability question highlights the different approaches of the participants. For example, in late 2008 one manufacturer announced abandoning copper-filled TSVs in favor of tungsten, because the differential thermal expansion of copper and silicon caused reliability problems, referred to as "copper pumping." A second group responded that copper-filling is reliable if the copper is properly post-processed after deposition. A third company replied that both copper and tungsten filling are reliable if properly designed and deposited, but that tungsten has shown higher reliability than copper. A fourth company pointed out the higher cost and the limitations of tungsten deposition.

Even the papers in this Technical Bulletin show some differing viewpoints. One paper favors eliminating adhesive layers to make thinner die stacks; another prefers the adhesive layers for stronger construction, and for pre-bond stacking. TSVs have been generally filled from the top down, but one paper shows the advantages of bottom-up filling. Cu/CuSn is identified as a better bonding method to compensate for surface irregularities, but Cu/Cu bonding has greater strength, a potential benefit in stacks that include heterogeneous die with differing thermal expansion coefficients. Progress is made by reconciling different paths.

The timetable for full task completion is not yet clear. Fully qualifying a completed line to begin volume production may take more than a year. Some independent assembly firms might offer customers a fast-track approach first, providing outsourced assembly with silicon interposers rather than with direct die-to-die connections. These are sometimes referred to as "2.5-D assemblies." What is clear is that the industry's "moon landing" at high volume, fine pitch 3D production will occur earlier, rather than later, in the new decade.



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