Die-to-Wafer bonding of thin dies using a 2-Step approach;

High Accuracy Placement, then Gang Bonding

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OUTLINE

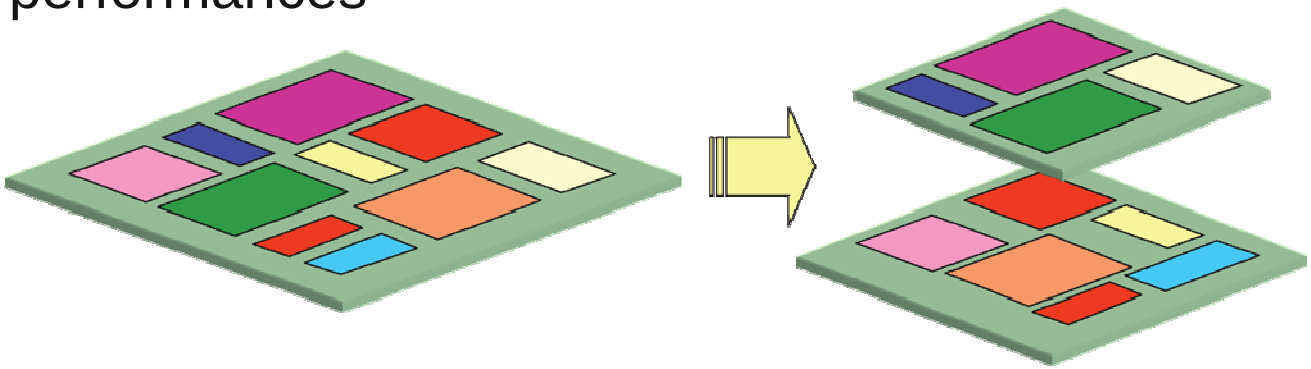
- **Introduction**
  - The push towards 3D
  - Wafer-to-Wafer Vs Die-to-Wafer
  - Die to Wafer Bonding Approaches
- **Demonstrator description**
- **Bonding process and results**
- **Summary**

3D ASSEMBLY BY CHIP OR WAFER STACKING

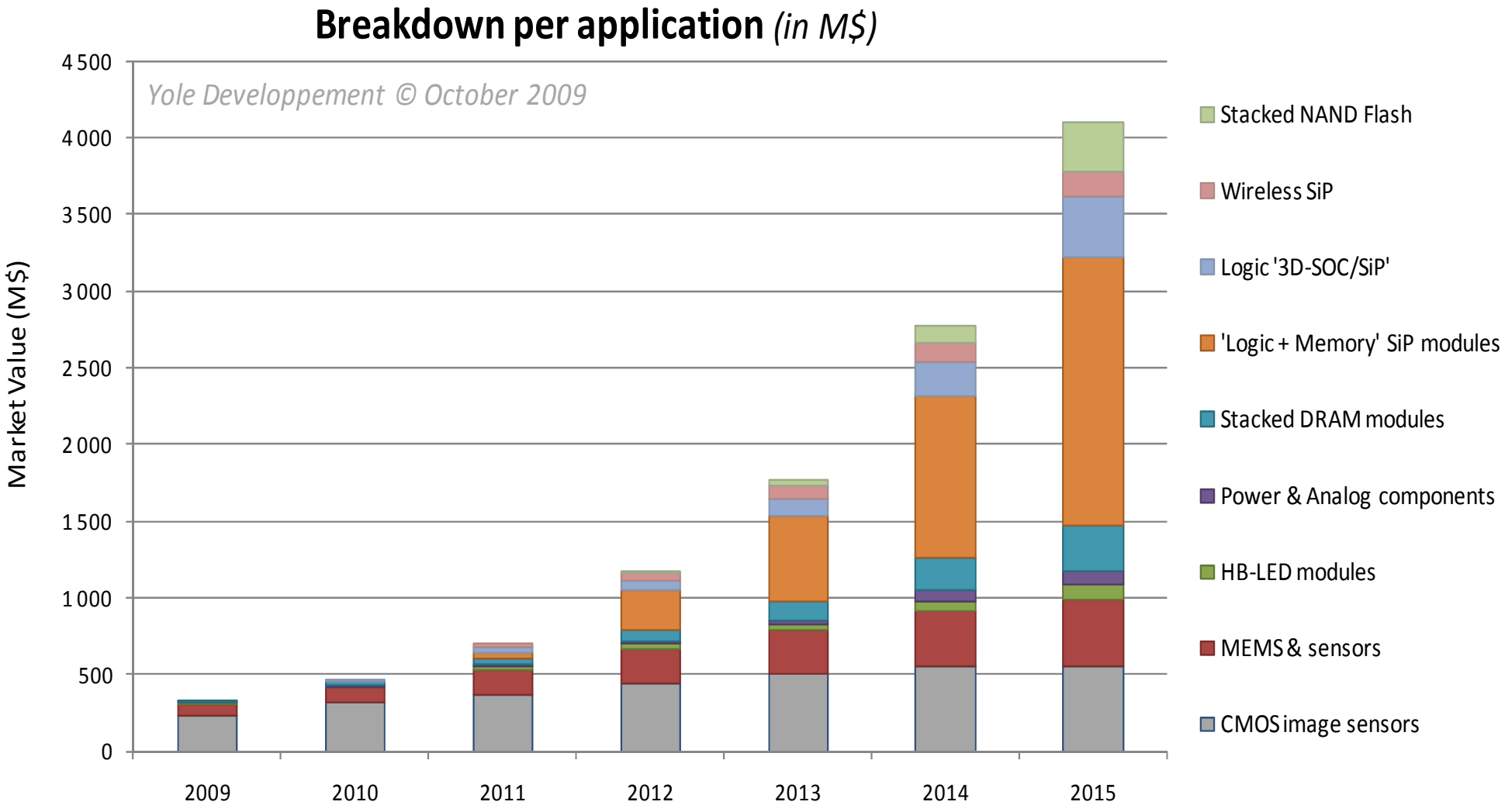
Higher density 3D die-to-die interconnection has been a major industry goal for the past decade

- **Multifunction Devices (heterogeneous integration)**
- **Higher Packaging Miniaturization**

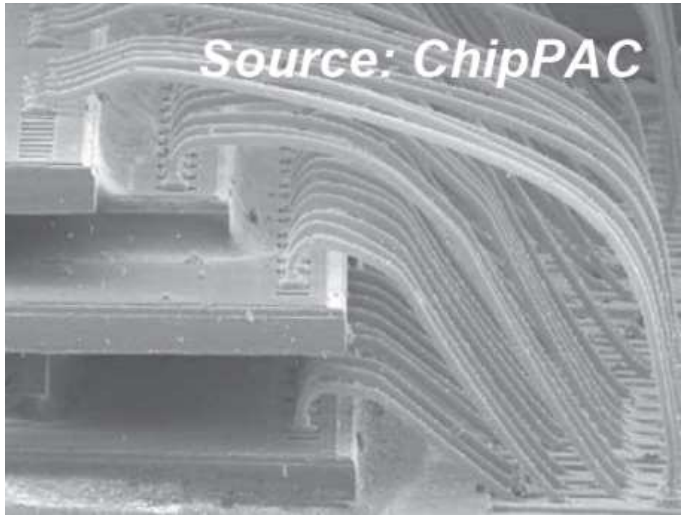
  Repartitioning
  - Reduces area of individual chips (Yield improvement)
  - Reduces number of mask levels per die (Cost reduction)
  - Results in much shorter global interconnect lines for better performances



3D-TSV PACKAGING FORECAST

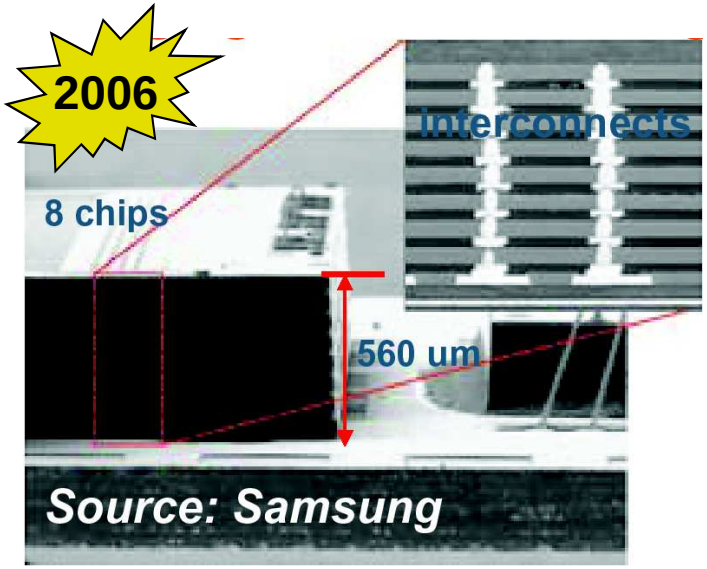


3D TECHNOLOGY EVOLUTION



- **Established 3D Technology**

  Stacked Dices interconnected using Wire bonding technology is widely used
  - Peripheral, Long wire bonds
  - Low-density interconnects



- **Memory stack with TSV**
  - Higher 3D-Interconnect density
  - Increased performance

    Shorter connection

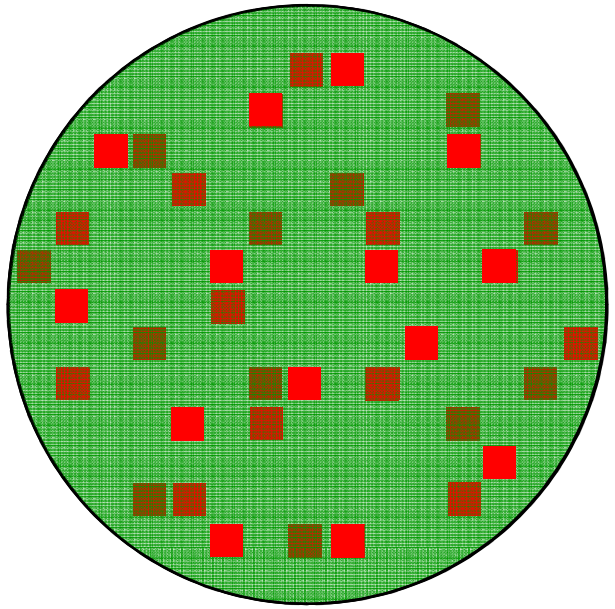
    Lower Capacitance and Inductance

PLACEMENT SCHEMES

- **Wafer-to-Wafer Bonding (W2W)**
- **Die-to-Die (D2D / C2C)**
- **Die-to-Wafer Bonding (D2W / D2W)**
  - In situ Bonding
  - Sequential placement followed by gang bonding

CHIP TO WAFER Vs. WAFER STACKING

- **WAFER STACKING**
  - ☺ High Throughput
    → Wafer Level
  - ☹ Component size must be identical
  - ☹ Yield ?



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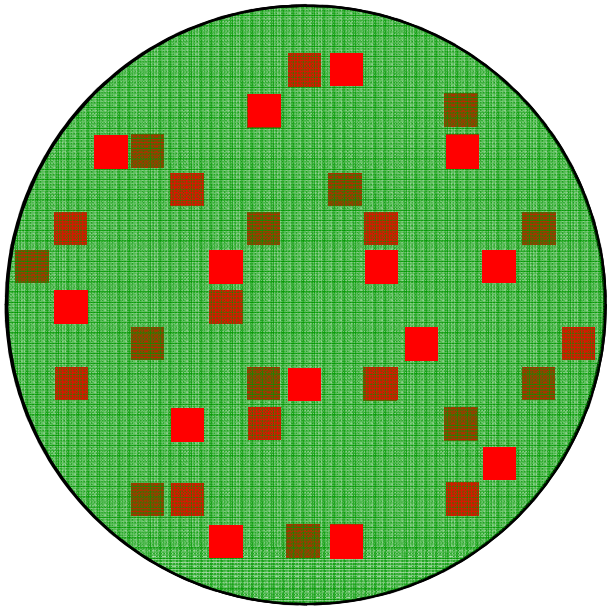
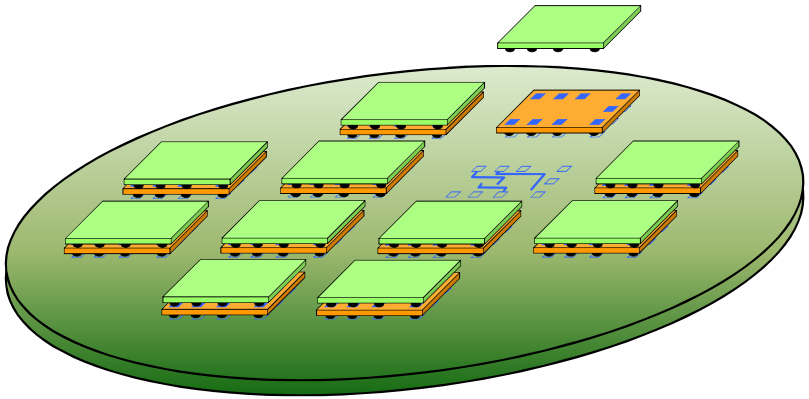
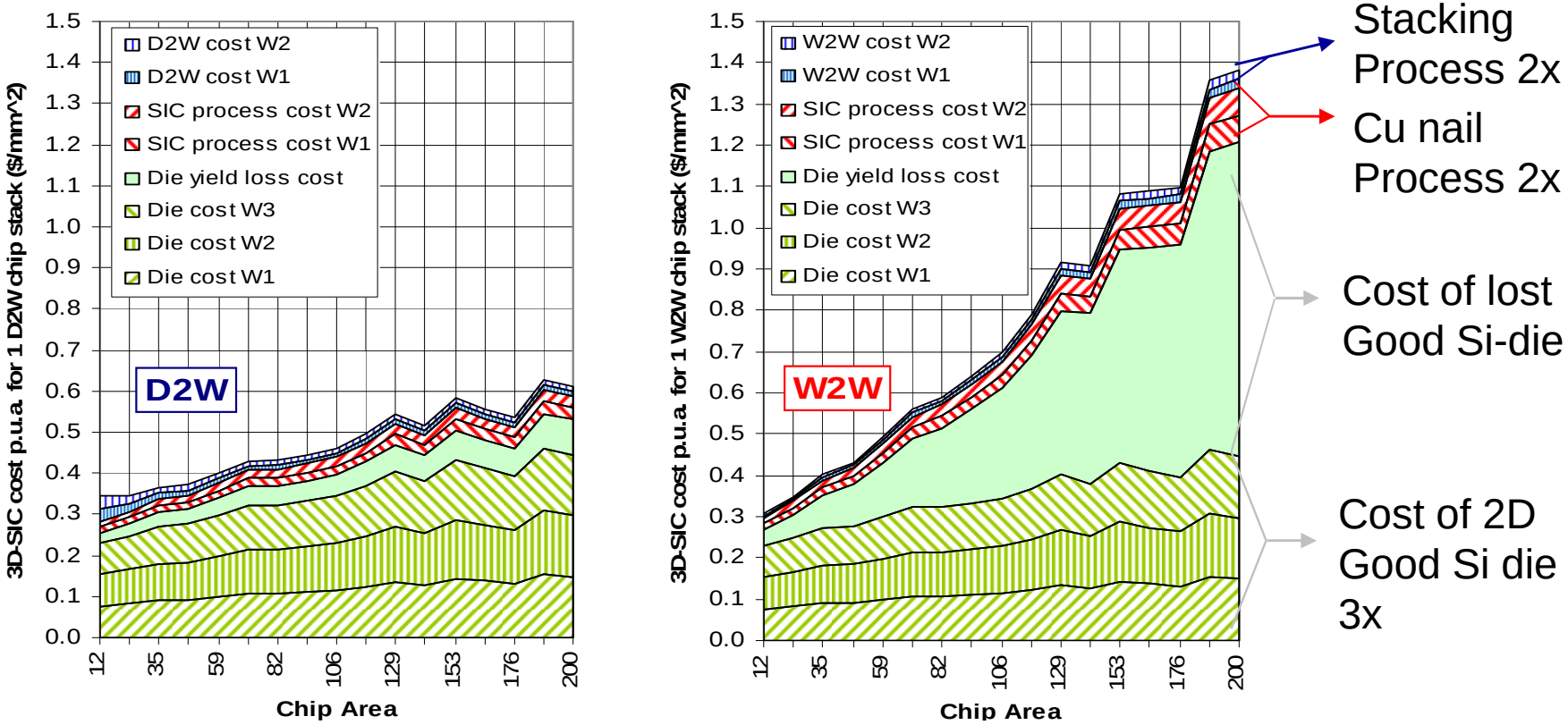


- **CHIP-TO-WAFER**
  - ☹ Lower Throughput
    - → Single Chip Placement
  - ☺ High Yield
    - → Known Good Die
  - ☺ Flexibility
    - → Component size
    - → Different Technologies



COST EFFECTIVE INTERCONNECT BONDING

- **W2W vs D2W bonding: trade-off between cost and alignment accuracy / TSV density requirements**



Assuming: Yield 1cm² die = 80%, Die yield Y = Ypua.A , Fault coverage KGD test = 90%, W2W and D2W have a 95% processing yield, Production volume 10^4 wafer stacks.

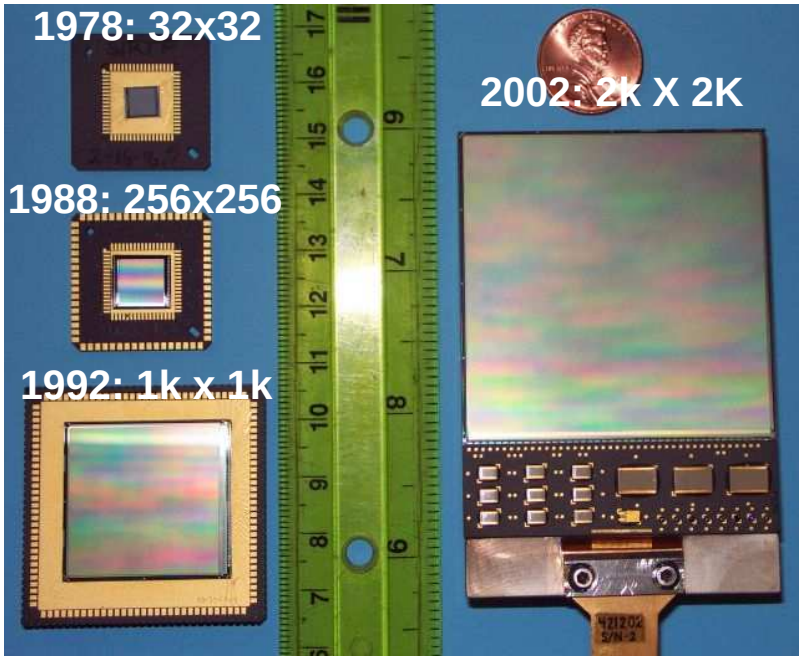
3D-SIC Cost p.u.a. = Stacked Wafer cost/(number of good 3D stacks x die area)

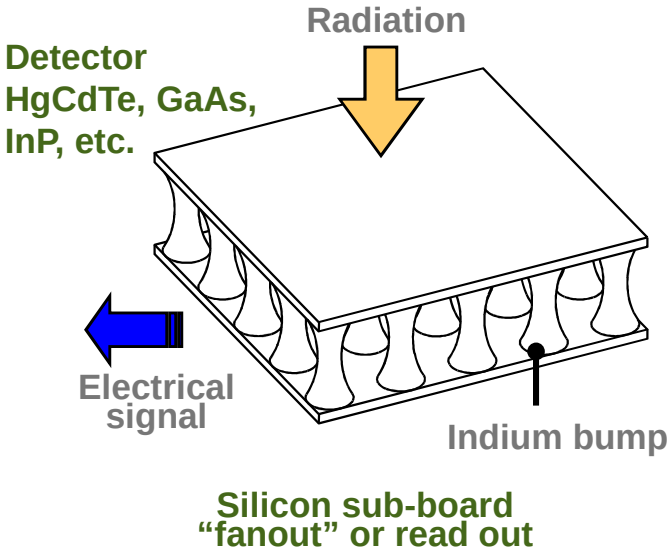
HIGH ACCURACY PLACEMENT

PIXEL DETECTORS: LONG HISTORY IN FINE PITCH DIE STACKING

- Small bumps (down to 5 µm)
- Fine Pitch (down to 10 µm)

→ High Accuracy Placement and Tight Parallelism Control



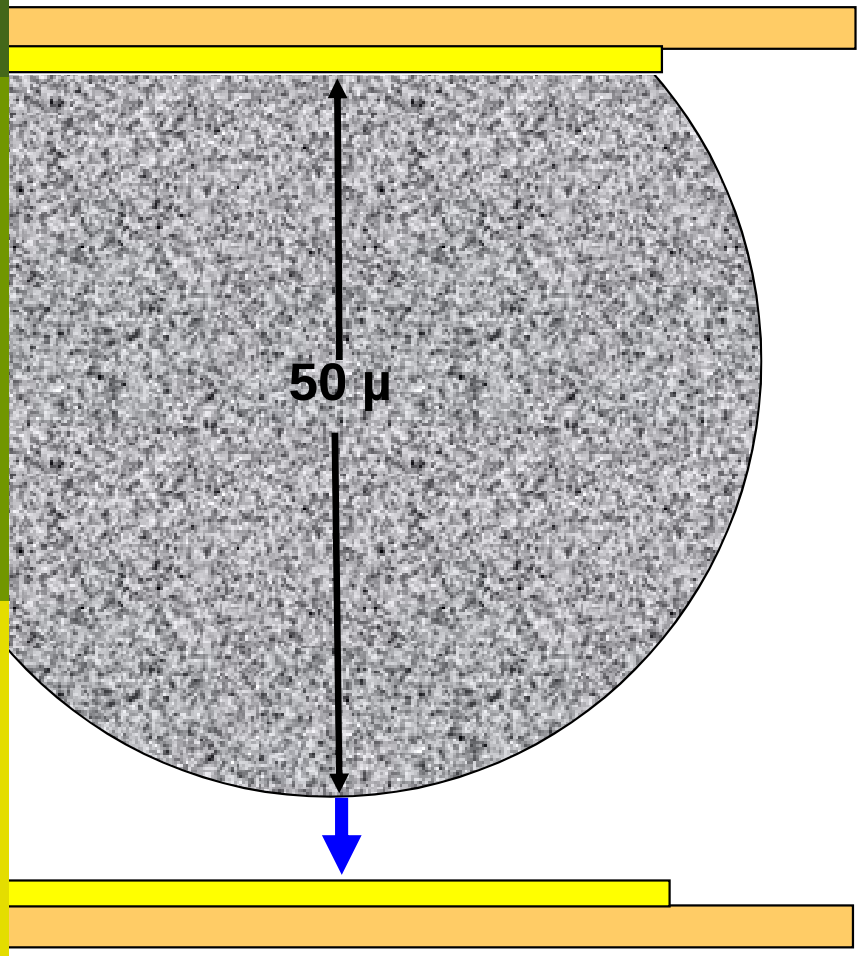


- For over 30 years, this application has demonstrated successful Heterogeneous Integration of Low Pitch devices with various bonding methods

3D-IC, ACCURACY REQUIREMENTS

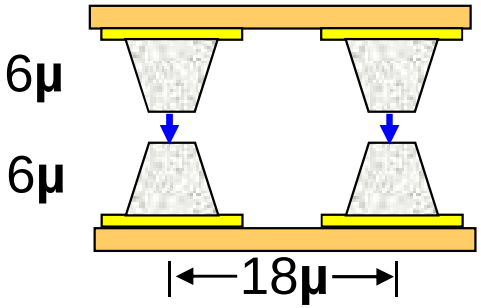
SIMILAR TO IR-FPA CHALLENGES: SMALL PIXEL/BUMP SIZE

Conventional flip-chip solder ball

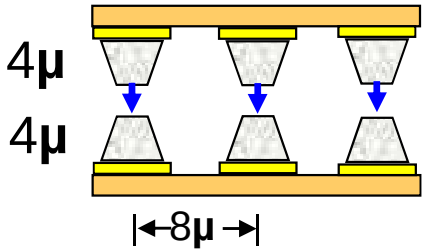


Indium-bumped IR-FPA

Today



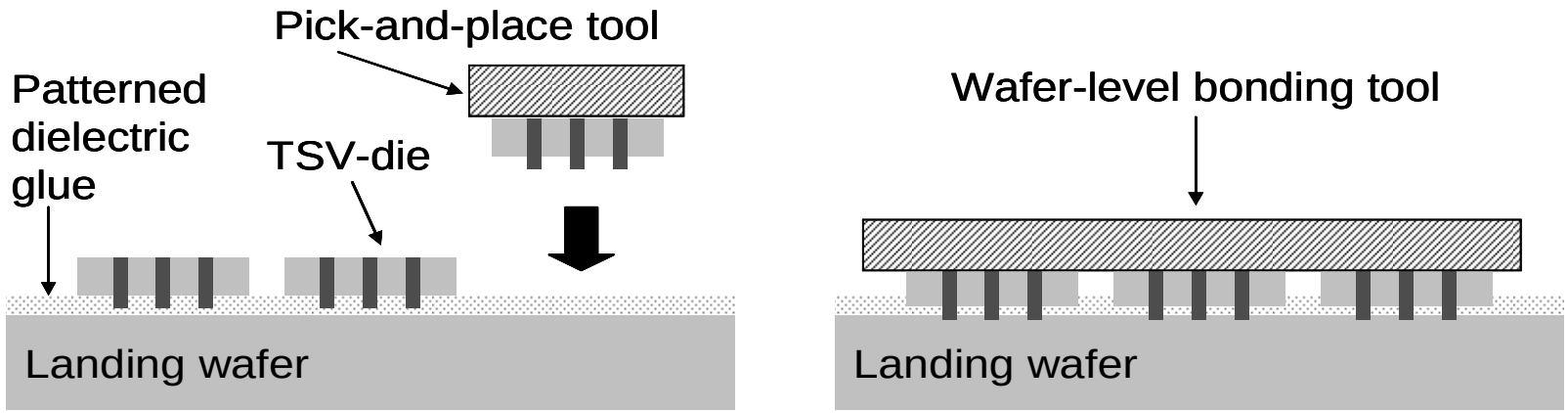
Tomorrow



- **3D Interconnect using High Density TSV technology converge with these assembly Requirements**
- **High Throughput Required for 3D-IC adoption, still need to be addressed**

COST-EFFECTIVE HYBRID D2W BONDING

- **Cost effective processing by segmentation of 3D assembly process into Pick-and-Place + Collective Bonding.**



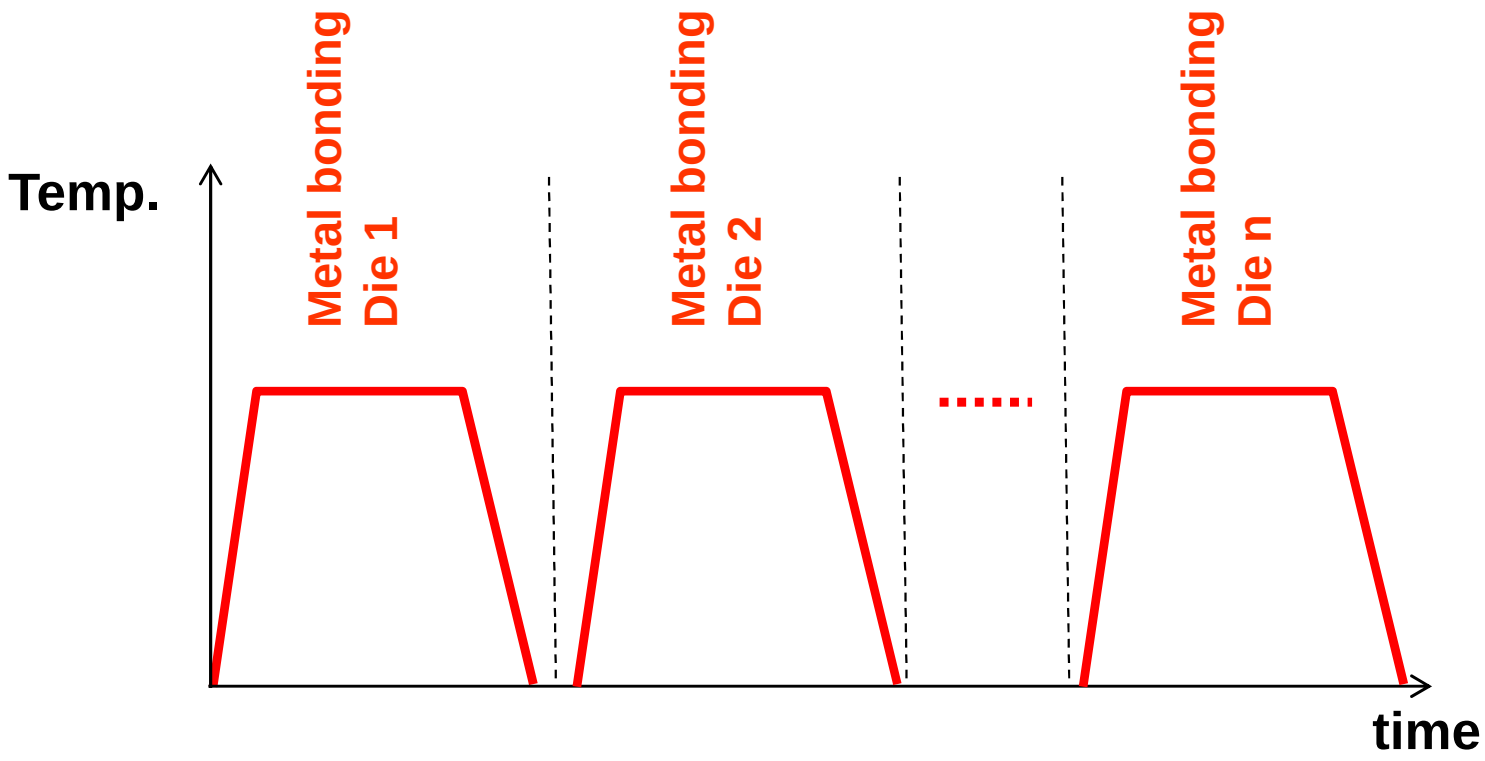
Die Pick and place ⇨ ***Collective bonding***

- **Enables:**
  - KGD selection
  - Increased efficiency of 3D assembly process

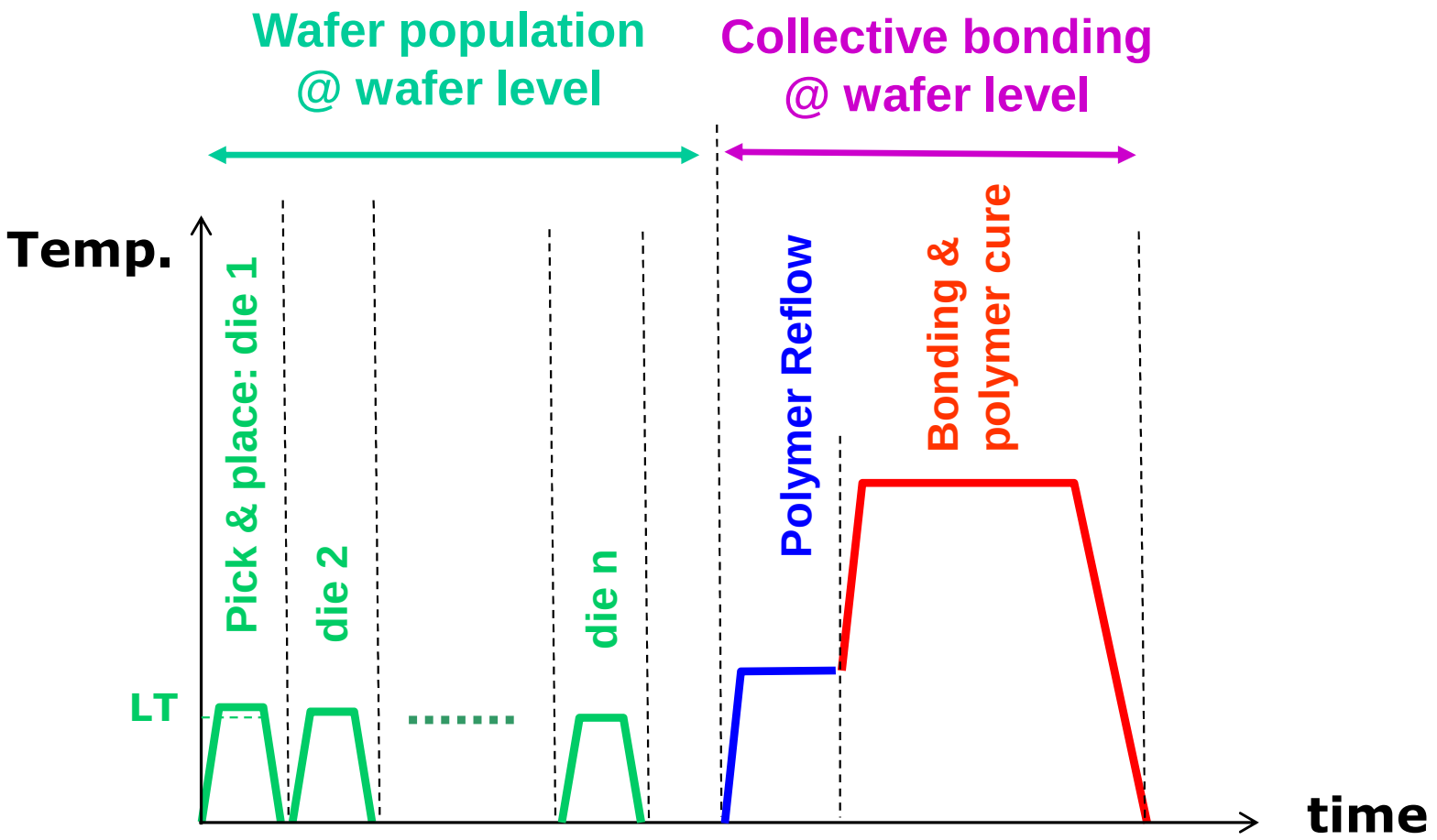
IN-SITU Vs HYBRID APPROACH
DIE-TO-WAFER BONDING, TEMPERATURE PROFILE

Sequential D2W bonding

- **Time consuming**
- **Landing wafer sees several bonding T-cycles**

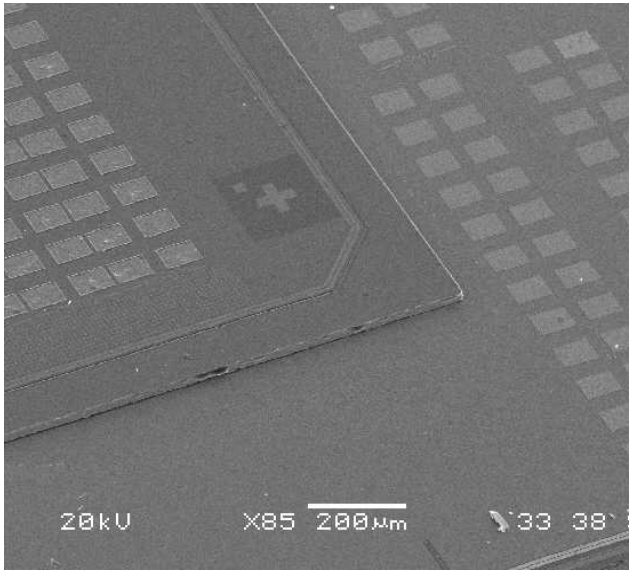


IN-SITU Vs HYBRID APPROACH
COLLECTIVE HYBRID BONDING, TEMPERATURE PROFILE



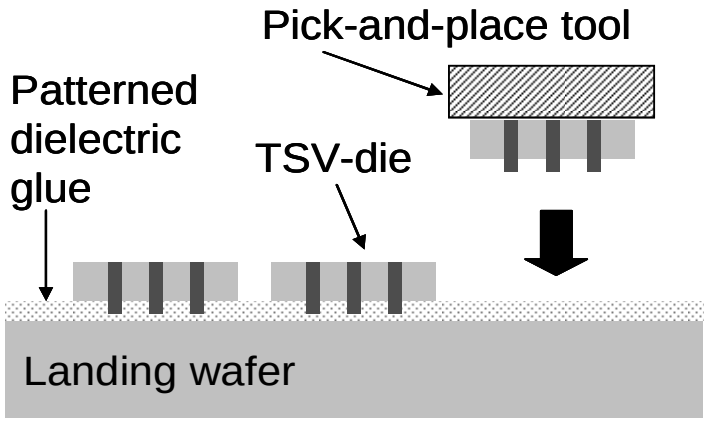
D2W BONDING WITH HYBRID APPROACH
IMEC DEMONSTRATOR

- **Top die: 25 um thick, mounted on thick carrier die**
- **Placement on a 200mm landing wafer covered by a patterned polymer acting as a temporary alignment holder using the SET High Accuracy Die Bonder model FC300 (± 0.5µm)**

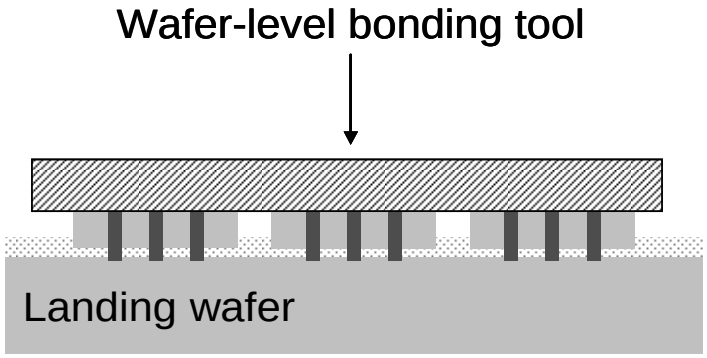


- **Bonding process: Cu/Cu (10µm pitch)**
- **Special test structure was designed on the landing die to electrically determine the alignment accuracy after bonding - both with respect to the X-Y alignment and the rotation**
- **Stacks are assembled by collective hybrid bonding process using wafer bonder**

D2W BONDING WITH HYBRID APPROACH
PICK AND PLACE

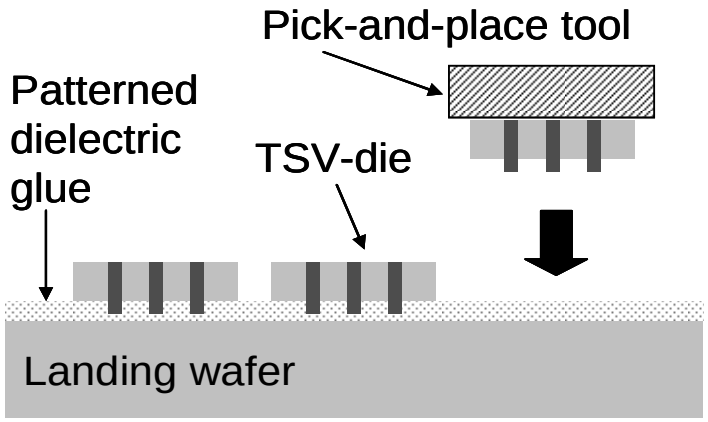


Die pick and place

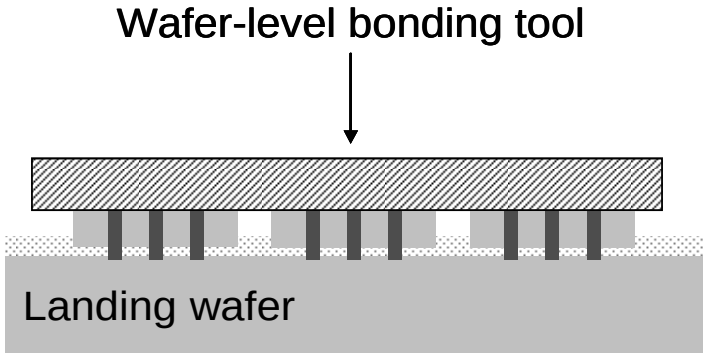


Collective bonding

D2W BONDING WITH HYBRID APPROACH
COLLECTIVE BONDING



Die pick and place



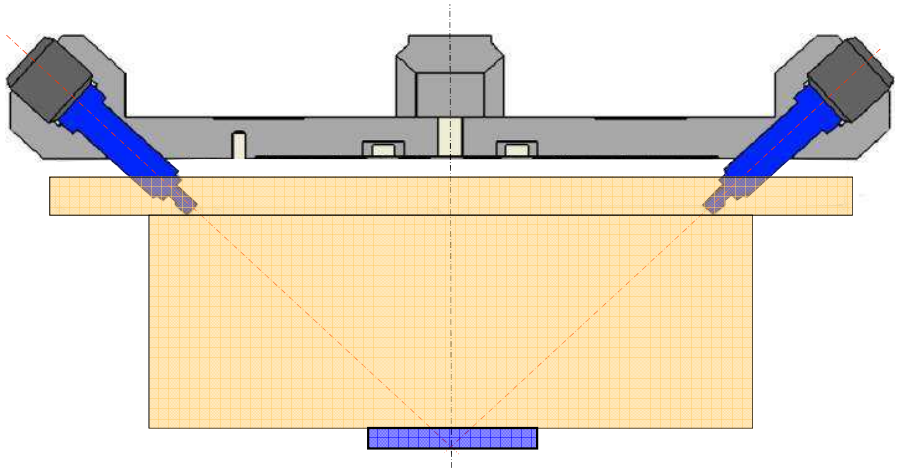
Collective bonding

PLACEMENT TOOL USED FOR THE EXPERIMENT
SET FC300 - HIGH ACURACY DEVICE BONDER

- **± 0,5 µm, 3σ Post-Bond Accuracy**
  (Process dependent)
- **Die Bonding, Flip Chip Bonding**
- **Large Device Bonding Capability**
  - Device up to Sq. 100 mm
  - Substrate up to Ø 300 mm
- **Process Flexibility**
  - Up to 400 kg Bonding Force
  - Up to 450℃ Heating
  - UV-Curing, Ultra Sonic

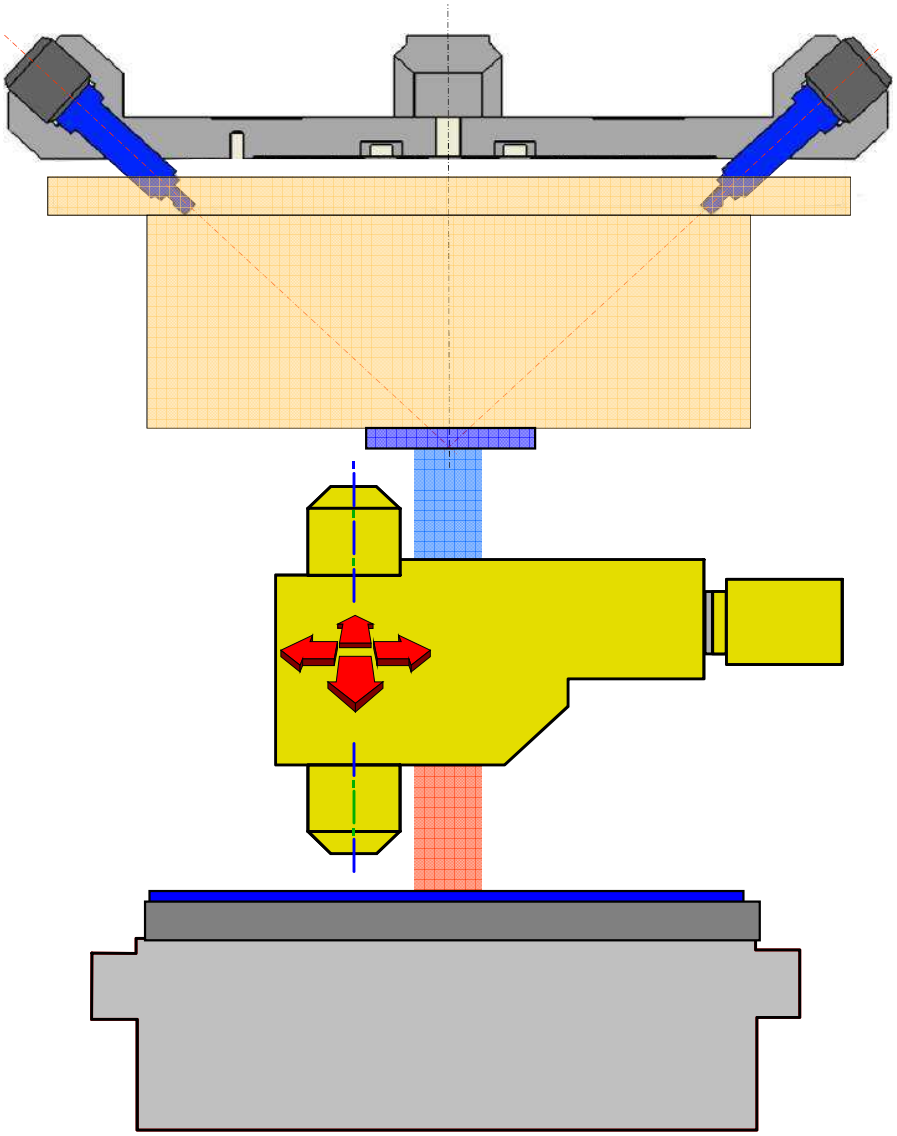
ALIGNMENT AND PLACEMENT SEQUENCE

- Die is vacuum-secured on a Silicon Carbide Pick Up tool



ALIGNMENT AND PLACEMENT SEQUENCE

- Die is vacuum-secured on a Silicon Carbide Pick Up tool
- Parallelism can be actively adjusted by motorized sphere coupled with an autocollimator



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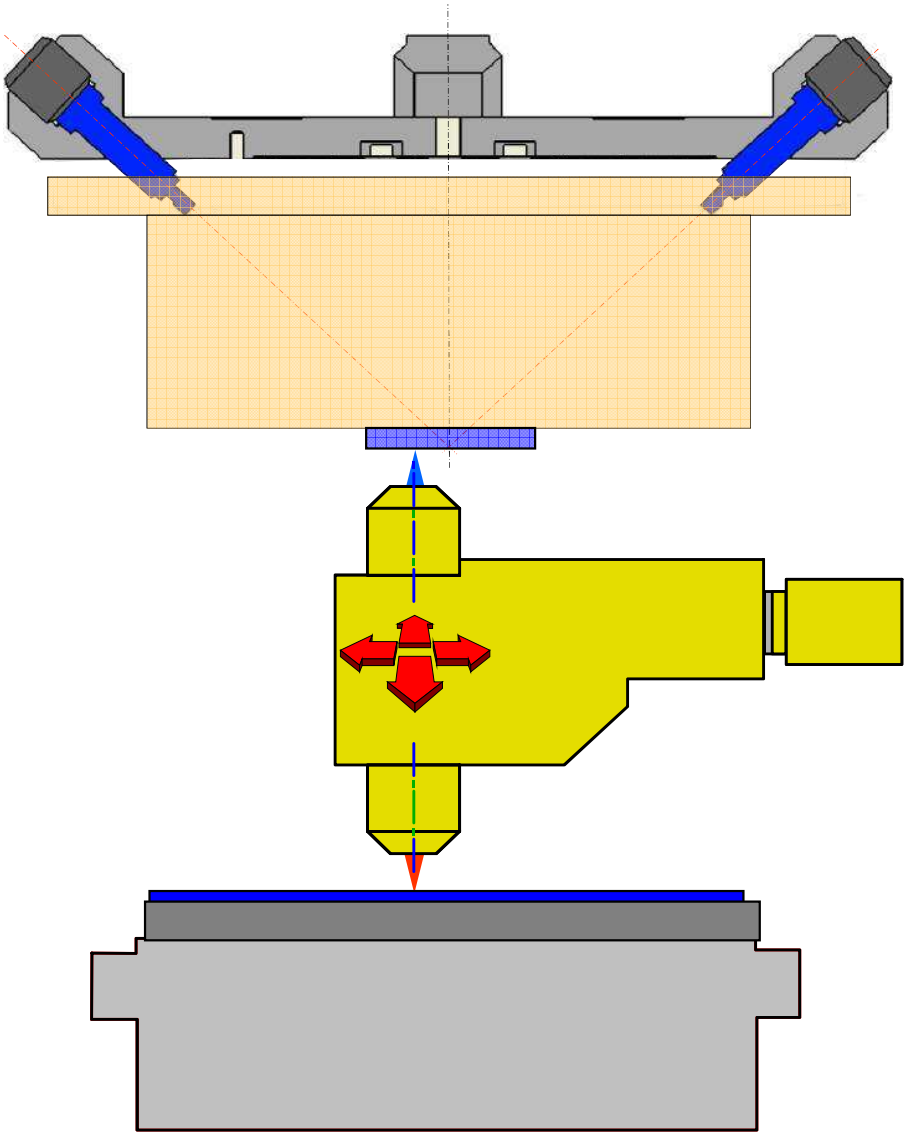
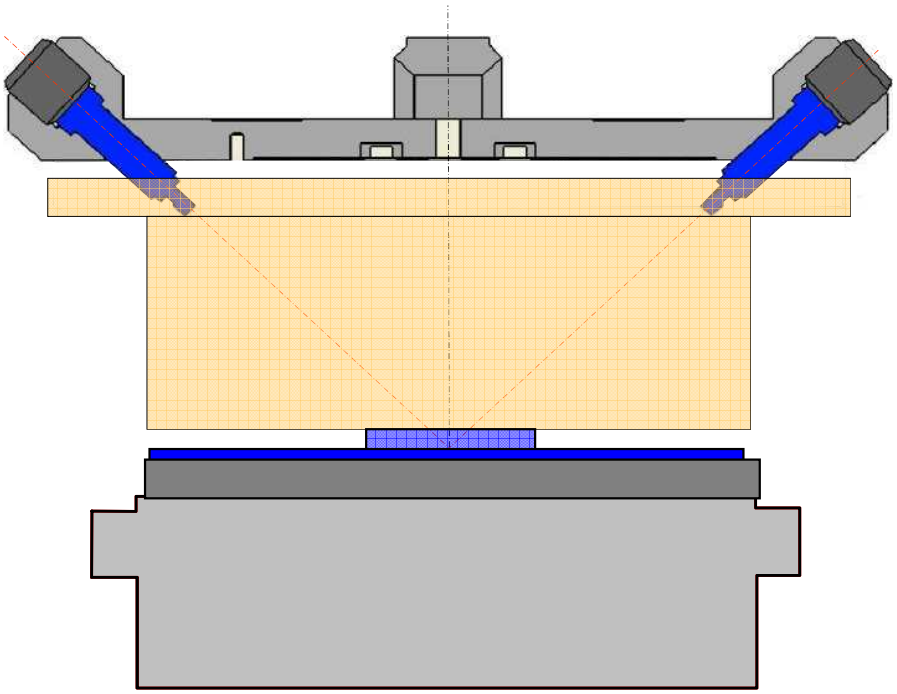
- XYθ Alignment is achieved by inserted microscope between the die and the wafer



ALIGNMENT AND PLACEMENT SEQUENCE

- Die is vacuum-secured on a Silicon Carbide Pick Up tool
- Parallelism can be actively adjusted by motorized sphere coupled with an autocollimator
- XYθ Alignment is achieved by inserted microscope between the die and the wafer
- For very large die, Parallelism can eventually be finalized by Self Leveling during the Placement sequence when parts are into contact



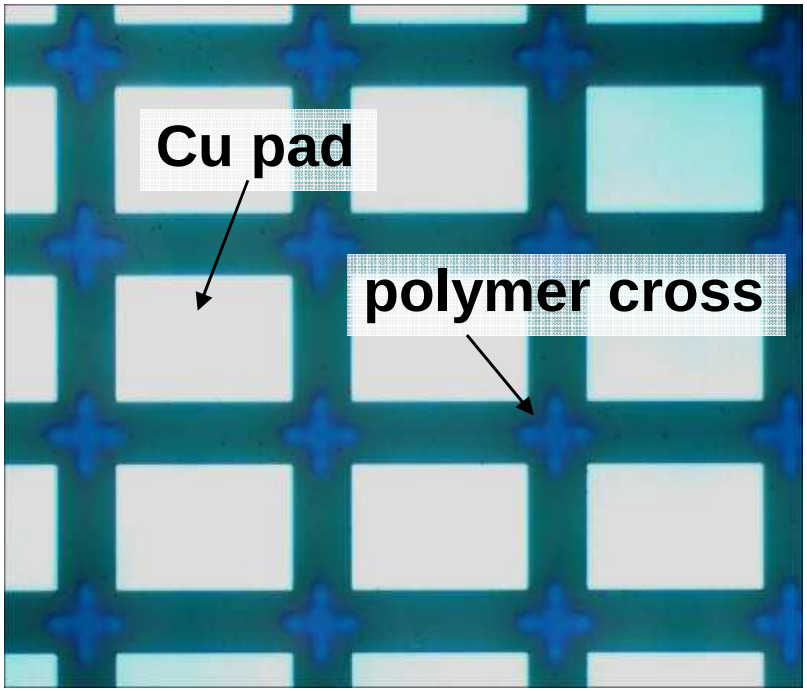
PICK & PLACE PERFORMANCE
TOOL AND MATERIAL REQUIREMENTS

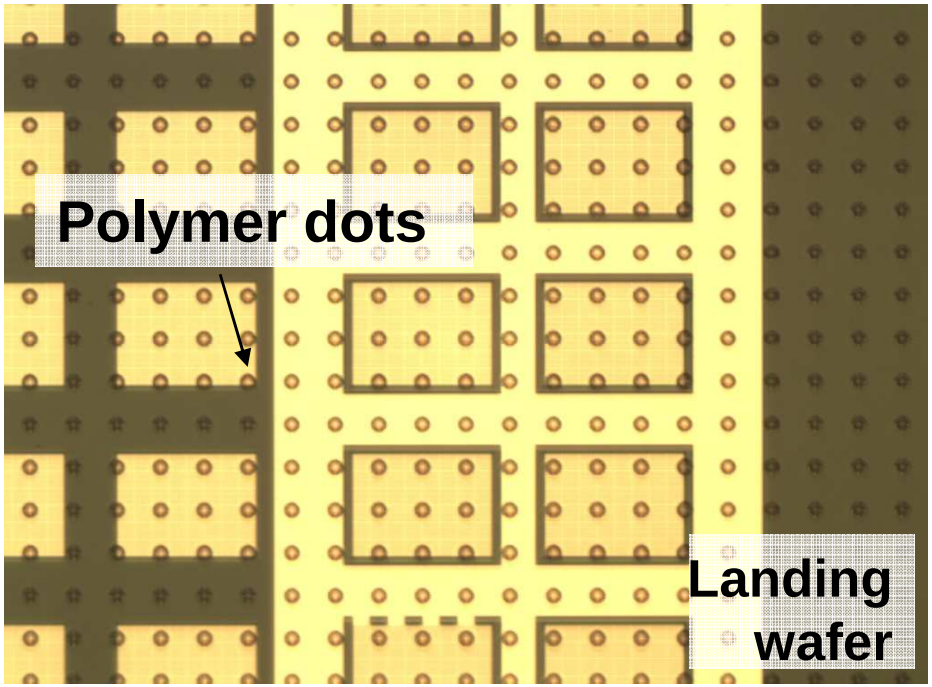
- **Assessing Pick-and-Place performance by assessing die sticking**
  - Top-die Pick-and-place temperature (landing substrate @ Room Temperature)
  - Minimal touch-down time
  - Minimal touch-down force
- **Polymer Requirements**
  - Photo-patterning ability
  - Adequate Adhesion to die after Photo Patterning
  - Good deformability of patterned polymer during bonding
  - Compatible with Cu-Cu bonding T (> 250℃)

POLYMER SELECTION
PATTERNING PROPERTIES

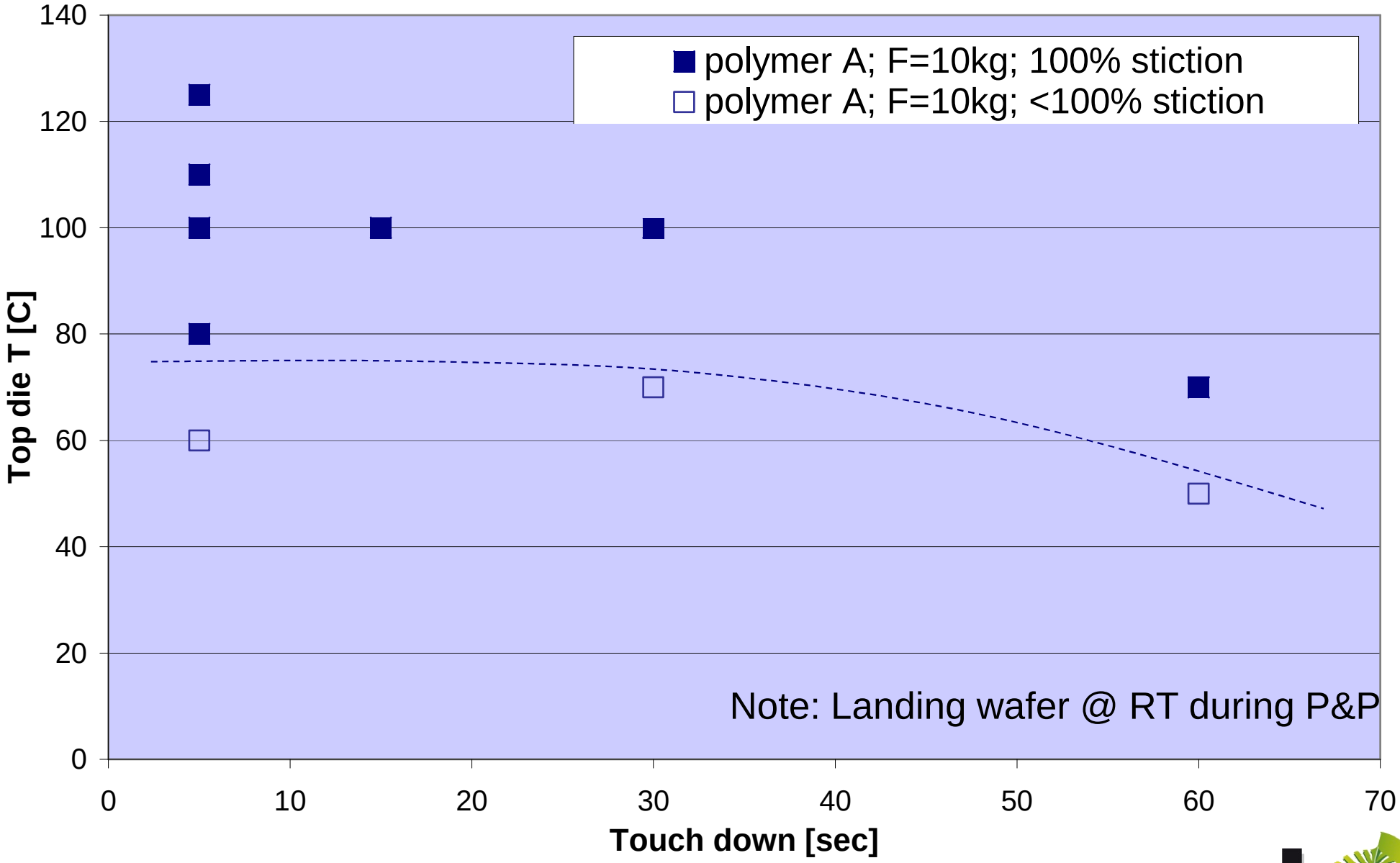
Polymer patterning:

- Using 1X aligner
- Typical cross or dot patterns
- Two different polymers were tested (A, B), they perform similarly





POLYMER SELECTION
PICK AND PLACE PROCESS WINDOWS



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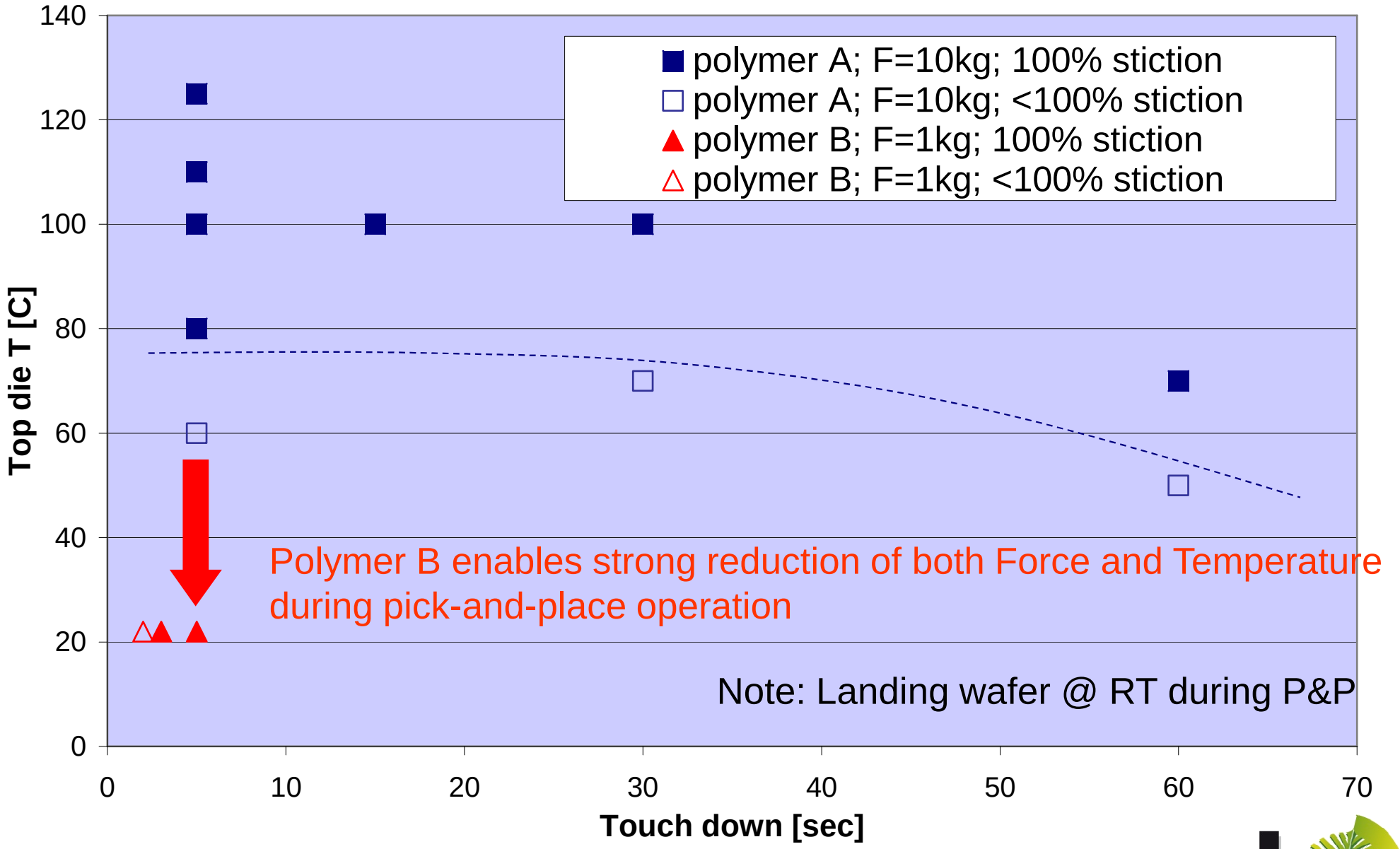


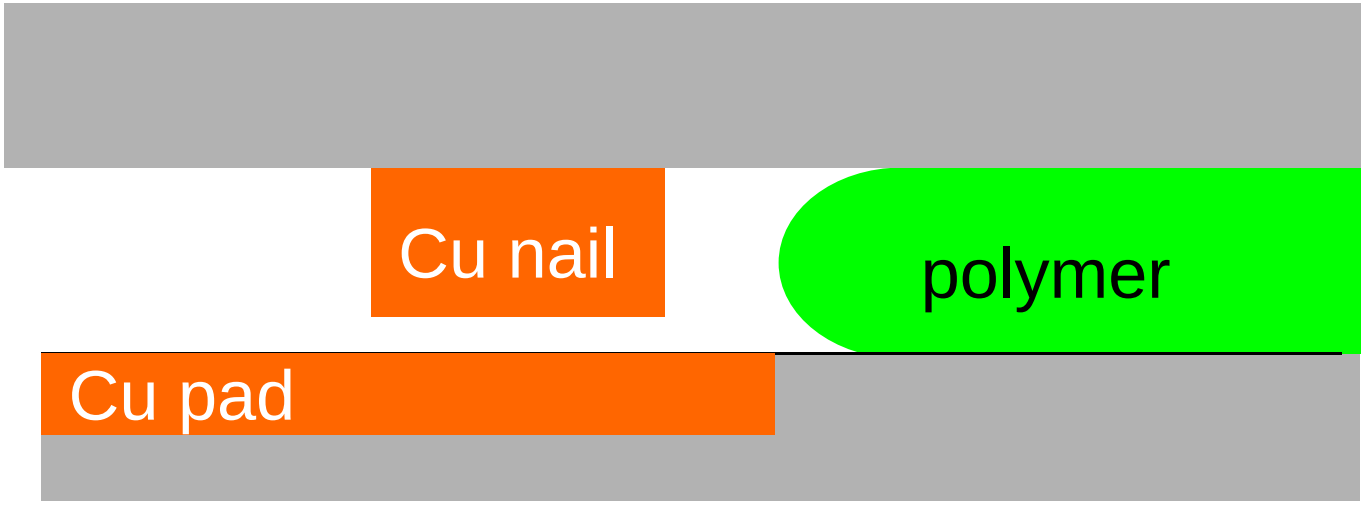
COLLECTIVE BONDING
BONDING CONDITIONS

Temperature (T) and time (t) as optimized for applied polymer

- **Bonding**
  - Temperature = 300℃
  - time = 15 min
  - Force ~ metal area to bond

PICK AND PLACE AND COLLECTIVE BONDING

- **Die placement is performed in the SET-FC300 Die Bonder**
  Die is picked, aligned and Placed on the wafer, secured by the Polymer

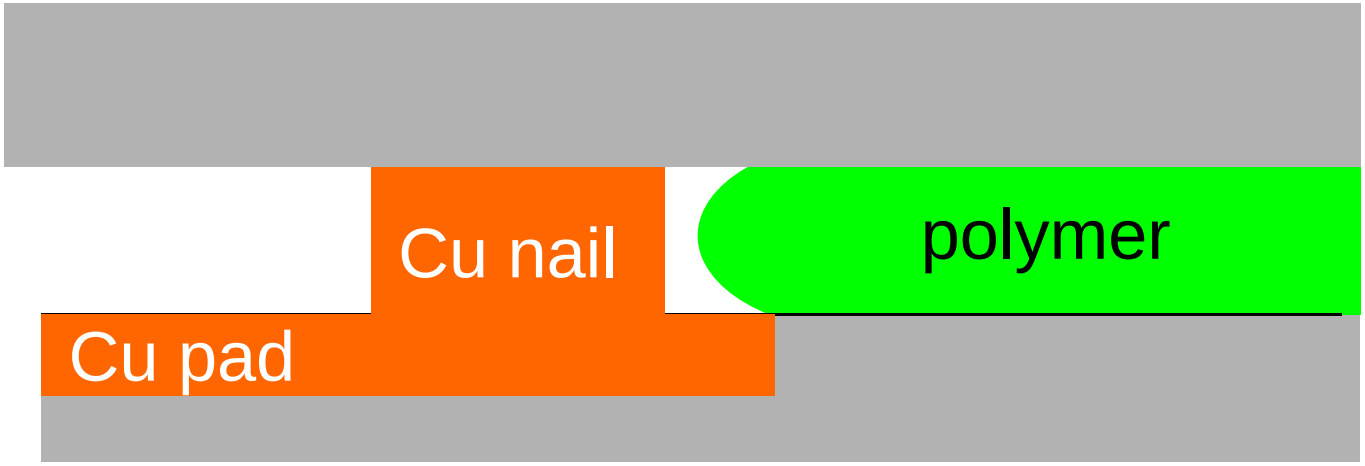


PICK AND PLACE AND COLLECTIVE BONDING

- **Die placement is performed in the SET-FC300 Die Bonder**

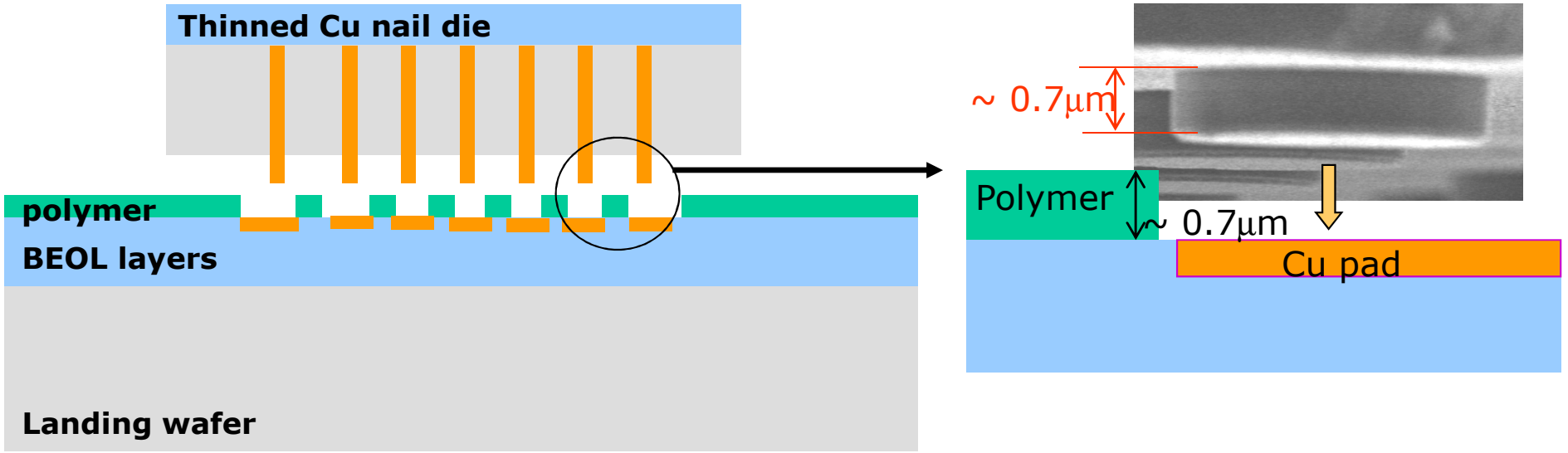
  Die is picked, aligned and Placed on the wafer, secured by the Polymer

- **Gang Bonding is performed in a wafer Bonder**
  - The Polymer is reflowed while the force is increased
  - It is a critical step as die shifting might appears

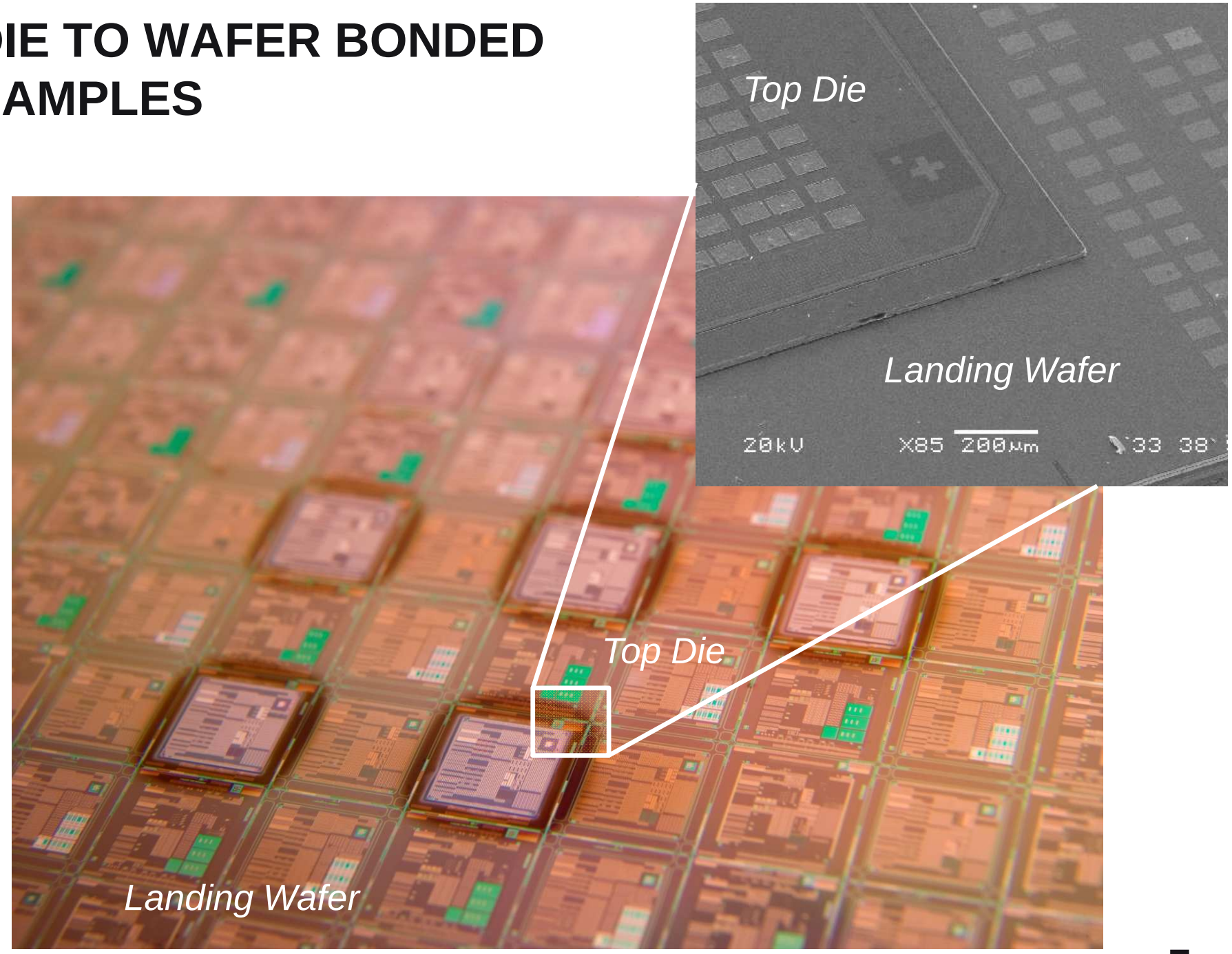


CASE STUDY: DIE TO WAFER PICK & PLACE FOR Cu-Cu HYBRID BONDING

- **Application: Hybrid Cu-Cu bonding for 3D stacking**
- **Principle: Simultaneous Metal / Dielectric Bonding**
- **Inclusion of Polymer dielectric**
  - Decreases sensitivity to particle inclusion
  - Provides mechanical stability in areas with low TSV Density



DIE TO WAFER BONDED SAMPLES



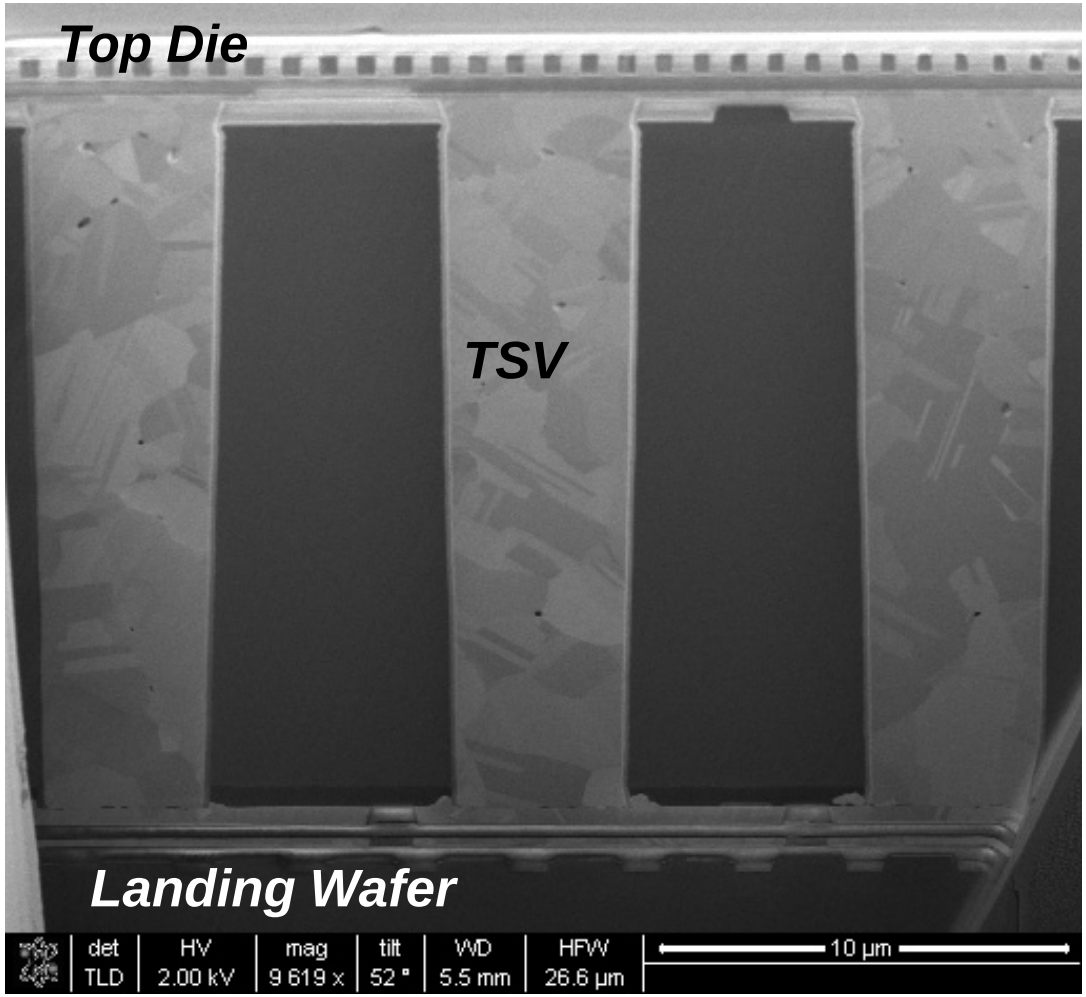
ALIGNMENT ACCURACY RESULTS

- **Alignment accuracy result combines Pick &Place and Gang Bonding steps**

  1.75 μm ± 1 μm

- **Measured Interconnect resistance**

  < 50 mΩ



SUMMARY AND ACKNOWLEDGMENTS

Summary

- Higher density 3D die-to-die interconnection has been a major industry goal for the past decade and is now moving to production
- D2W bonding with a 2-Step Hybrid Approach is a cost effective, high yield and flexible solution for 3D-IC assembly
- The very low TSV – pad interconnection resistance indicates that the process is suitable for 3D stacking applications

Acknowledgments

- Thank you to the Imec Team who ran the experiments
- Special thanks to Philippe Soussan for his help in putting together this presentation