FLIP CHIP DIE BONDING: AN ENABLING TECHNOLOGY FOR 3DIC INTEGRATION

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ABSTRACT
3-Dimensional Integration of Integrated Circuits is a method to build greater functionality into ever-smaller spaces for electronic circuitry, wherein dice of varying sizes, materials, or even application types are electrically and mechanically bonded together. As chip sizes increase and packaging bump sizes decrease, a wide variety of difficulties has arisen in the areas of bonding materials, methodologies and equipment.

This paper will explore some of these new challenges, highlighting the inherent advantages and implications of various options. Specifically, the methodologies of chip-to-chip, chip-to-wafer, and wafer-to-wafer bonding will be examined, followed by discussions of some material choices and the associated bonding techniques such as in-situ reflow or thermocompression. Depending on the interconnect density and the selected bonding technology, either pick-and-place or high accuracy die bonders can be employed for attachment of the dice to the substrate, each with its own tradeoffs. Finally, a method of first placing the chips with high accuracy, followed by collective bonding will be explored for a customer application, including electrical and alignment test data.

Each scenario places special requirements on the bonding tool, so incremental modifications and enhancements to the flip chip bonding platform will be outlined and explored to gauge their impact in enabling 3DIC integration. In particular, hardware and materials to reduce oxides on the bonding surfaces will be highlighted.

Keywords: 3D Integration, TSV, Bonding, Oxide Removal, KGD

INTRODUCTION

In commodity-level chips, functionality has approximately doubled every two years; this trend is labeled Moore's Law after the Intel co-founder who first described it [1]. Historically, the route to providing this increased functionality has been centered on scaling chips to smaller dimensions for higher density and higher performance, but the continuation of this trend is becoming prohibitively expensive, primarily due to lithography costs. Technology is also hitting a scaling wall as costs to fabricate tiny circuit elements become prohibitive, and as conventional electronics approach their fundamental scaling limits.

Various methodologies have been proposed in recent years for increasing computing density, typically utilizing shorter interconnection paths by means of chip stacking, using the Z dimension as an alternative to only printing smaller features on the chip [2]. 3-Dimensional Integration has emerged as a prime route to shortening these connections. In this new methodology, circuit fabrication and packaging steps are leveraged to create new types of vertical interconnects which provide circuit paths not within the chip, but from one chip to another [3].

These direct connections are intended to provide greater functionality within smaller spaces, at higher operating speeds and lower overall costs than competing methods. Yole Développement, a respected market research firm, has highlighted 3D Integration with Through-Silicon Vias (TSV's) as a major growth opportunity for the semiconductor industry, as seen in Figure 1.

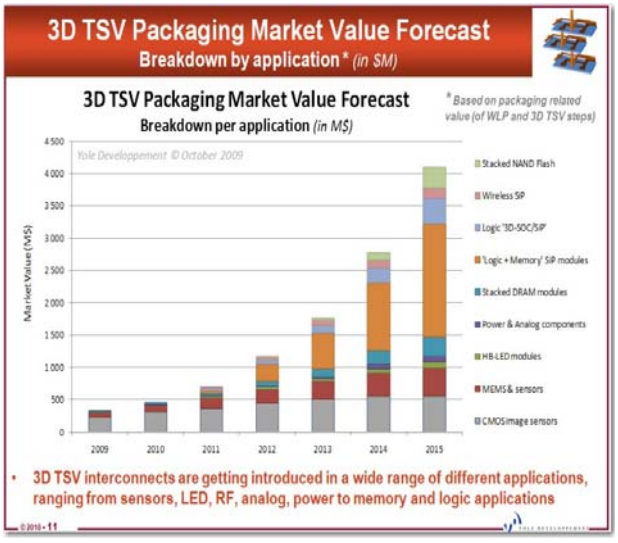


Figure 1. TSV Market Forecast Histogram from Yole Développement, Lyon, France.

To create these vertical interconnects, a TSV is etched completely through the silicon substrate, after which it is filled with a conductive material such as copper or one of its alloys. After the dielectric and metal patterns have been formed, substrates are thinned to some fraction of their original thickness, then the substrates are bonded together to form one electrical entity. A representative process flow to create and fill TSV's is shown in Figure 2.

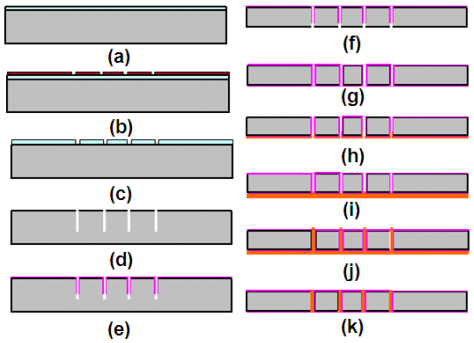


Figure 2 TSV fabrication and Cu fill as seen by wafer. First, a layer of SiO2 is deposited on the wafer as hard mask (a). Then thin layer of photoresist is spin coated and patterned (b). After SiO2 etch and photoresist stripping (c), TSVs are etched to the desired depth and SiO2 hard mask is removed after etching (d). After that, a layer of plasma-enhanced tetraethylorthosilicate (PETEOS) is deposited on the front side for sidewall passivation (e). Then the wafer is thinned down to expose the backside of the TSV (f). In order to fully passivate the side wall of the TSV, another layer of SiO2 is deposited on the back side of the wafer (g) and then a layer of Ti/Cu is sputtered at the back side of the wafer as seed layer (h). Figure and description courtesy of A. Yu of IME Singapore.

3D Integration has of course created a new set of challenges, though many of its core elements and processing steps are based on established front-end unit processes such as lithography, etching, depositions, and the use of various materials and combinations. This paper will explore solutions in 2 particular areas: the removal of oxides prior to metal-metal bonding, and the proposal of a collective hybrid bonding method to optimize accuracy and throughput between chip-level or wafer-level bonding methodologies.

OXIDE REMOVAL PRIOR TO BONDING

In a typical process flow for 3D Integration, TSV's are etched into the substrate, then filled with various conductive or dielectric materials. Numerous pure metals and alloys have been pursued for this conductive fill material, most notably Cu and its alloys. Numerous papers in the literature have cited the advantages of Cu-based systems, including ease and familiarity of processing, mechanical and electrical integrity, and scalability [4-7]. For these and other reasons, Cu has become a major focus as an interconnect material for 3D integration. A representative TSV structure for 3D chip stacking is shown in Figure 3.

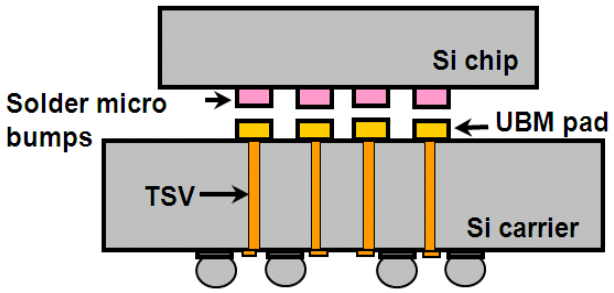


Figure 3. Schematic drawing of 3D stacking of the Si chip/Si carrier with TSV (not to scale). Image courtesy of A. Yu of IME Singapore.

To join the circuits together vertically, the exposed Cu surfaces are bonded together using either chip-to-chip, chip-to-wafer, or wafer-to-wafer bonding. Some technical and economic elements of these three methodologies are discussed later in this paper. In any case, the Cu surfaces likely have oxides present which compromise the thermocompression bonding results.

Oxidation of metal surfaces is a persistent problem in device bonding. Because oxides generally adhere poorly to other metals or oxides, the bonding force must penetrate the oxide, literally breaking through to achieve metal-to-metal cohesion. Not only does this increase the required bonding force, but the oxides may also raise the electrical resistance of the joint. Even after the device has been bonded, existing oxides may provide a convenient site for further oxidation, leading to reliability and performance problems. [6]. For this reason, high quality and reliable bonding would benefit from a controlled environment to either prevent oxide formation during the bonding sequence or to remove oxides previously formed. The requirements for an oxide removal process include:

- Fast, effective removal of oxides
- Inert to other surfaces
- Minimal or non-existent residue
- EHS compliant
- Sufficient duration of effect
- Cost-effective

Historical methods for removing or inhibiting oxides have included mechanical scrubbing during the bonding process, using an acid dip prior to bonding, or using oxide-reducing flux. Though these methods have worked for larger feature sizes, they can create misalignments, add processing steps, or in the case of flux, can lead to reliability or performance problems if flux residues are not completely removed.

A new method to remove oxides is proposed, wherein a local confinement chamber is formed on the bonding tool, using reducing gasses such as forming gas or formic acid

vapor to safely reduce the oxides immediately prior to bonding. The confinement chamber is created by using a non-contact virtual seal between the bonding head and the substrate chuck, ensuring gas collection and preventing oxygen intrusion. This setup is shown schematically in Figure 4 and enables gas confinement for chip-to-chip or chip-to-wafer bonding under controlled atmosphere while preserving the alignment of the device with respect to its substrate.

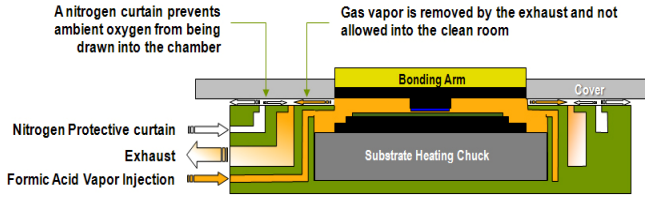


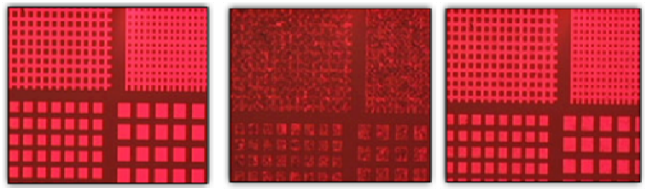
Figure 4. Schematic of local confinement chamber.

As noted in Figure 4, the process gas is injected through horizontal nozzles towards the device being bonded; an exhaust ring removes the process gas from the micro-chamber and sends it into the gas exhaust line, keeping the gas out of the machine and the clean room. A nitrogen curtain is formed around the exhaust, ensuring that ambient air is not entrained into the micro-chamber by the Venturi effect, while a cover attached to the bond head creates the confined micro-chamber. This configuration operates with either inert gasses to prevent oxide formation on bonding surfaces during the bonding sequence, or with reducing gasses such as forming gas to remove and prevent oxides. Photos of local confinement chamber hardware are shown in Figure 5.

(a) (b)

Figure 5. Photos of the confinement hardware looking down at the bonding chuck (a) or up at the bonding head (b).

To qualify the confinement chamber's performance, a chip with copper test patterns was heated to 350C for 30 seconds in the bonding position while formic acid vapor flowed into the chamber at 8 SLPM. All oxides were presumably removed and the copper surface was highly reflective. Next, formic acid vapor flow was terminated, and the copper surfaces oxidized rapidly at 350C with ambient air, producing a mottled appearance in less than 5 seconds. Following this, the formic acid vapor was reinstated and the copper returned to its reflective state within a few seconds, indicating that oxide removal was effective and rapid. Quantitative tests with electrical and/or bonding data are ongoing and are very positive, showing effective removal of oxides at 250-350C. Figure 6 indicates the testing of the copper coupon as described.



(a) (b) (c)

Figure 6. Copper patterns on test chip (a) after 30 seconds of formic acid vapor, (b) after a few seconds of atmospheric ambient, and (c) after formic acid flow is reinstated, showing the rapid reduction of the oxides.

COLLECTIVE HYBRID BONDING

Three methodologies have historically been used for joining of devices: die-to-die (DtD), die-to-wafer (DtW), and wafer-to-wafer (WtW). There are many issues to weigh and consider when choosing between these, including:

- CTE mismatch between materials
- Die size
- Yield and use of known-good-die (KGD)
- Overall cost

Die-to-die (DtD) bonding effectively addresses the issues of CTE mismatch between substrate types, the potential mismatch in die size between device types, and also offers the advantage of bonding only good die. The methodology has been in use for many years for high-performance chips such as infrared imaging devices. Because of the high resolution imaging requirements, these imaging devices have extremely high bump counts (> 10 million), necessitating the use of very precise and often time-consuming bonding processes. Though DtD will continue to play a role in certain markets, it is a slow and therefore expensive methodology which will likely be relegated to low-volume applications.

Developed and used extensively for MEMS processes where a cap wafer was required, wafer-to-wafer bonding (WtW) has likewise been in use for some time. More recently, it has been applied to 3D Integration due to its inherent high throughput and process simplicity. But since 3D Integration is specifically intended to bond various device types of widely different sizes and materials, WtW bonding may be attractive only when joining smaller, higher-yielding devices, and where dice and wafers are equally sized.

Die-to-wafer (DtW) bonding is a very promising assembly strategy which may capture the best of the two previous methodologies, but very long bonding processes can also limit its cost-effectiveness. It offers high yield due to using only known-good-dice, high flexibility allowing heterogeneous integration, and high accuracy placement potential by means of the flip chip device bonding technique. This method might suffer from potentially lower throughput since each die is aligned and bonded or placed

individually. However, this drawback is offset by the benefit of bonding only known-good-dice to known-good bonding sites of the wafer, increasing the final yield and therefore cost-effectiveness. DtW bonding is also compatible with multiple bonding process flows and metallurgies, including reflow, thermocompression of copper and other metals, thermosonic bonding, adhesive and fusion bonding, as illustrated in Figure 7. The roadmap for 3D Integration calls for increasing density of TSV's and related elements, necessitating ever-tighter alignment and control, and driving a move toward DtW bonding [9, 10].

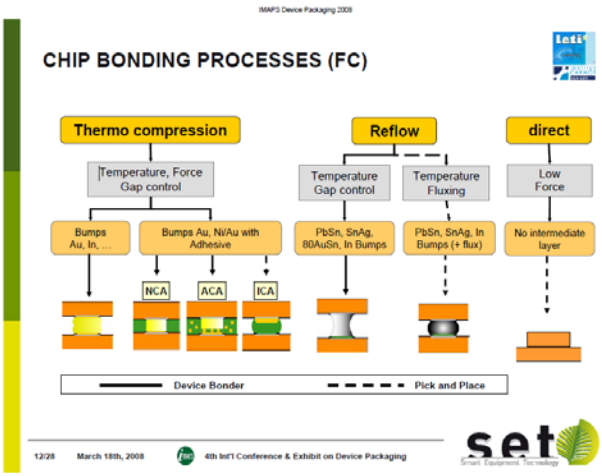


Figure 7. Matrix of chip bonding processes.

A new method has been applied in which singulated dice are initially bonded or tacked to a wafer in DtW fashion, then the bonding process is completed in a wafer bonder tool. Intended to address the issues of CTE mismatch and bonding KGD of various sizes, yet with the cost effectiveness and throughput of a WtW scheme, this method has been referred to as collective hybrid bonding and is illustrated in Figure 8.

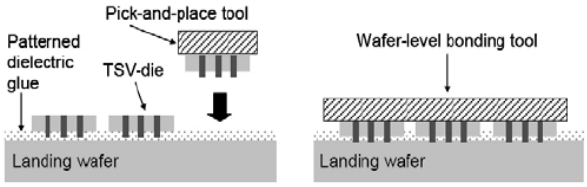


Figure 8. Illustration of Collective Hybrid Bonding, where accurate placement of TSV die is followed by gang bonding of all dice to complete the bonding process. Courtesy of Anne Jourdain of IMEC.

In one application of this collective hybrid bonding strategy, a patterned dielectric adhesive was used to populate a wafer in DtW fashion [11]. The author notes the inherent flexibility of DtW for 3D Integration, particularly for heterogeneous integration, as it allows varying die sizes and is compatible with the selection of known-good-dice. Following the DtW placement step, the populated wafer was further bonded in a two-step process in a wafer bonder wherein reflow of the polymer pulled the Cu TSV's into mechanical and electrical contact with the Cu landing pads. For this process, 2 different polymers were used; electrical results are shown in Figure 9 and indicate yields of 80+% for daisy chains up to 1000 TSV's in length.

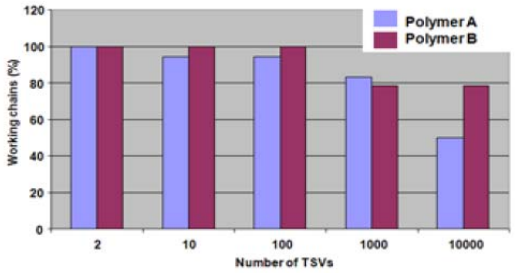


Figure 9. Electrical yield on 1000 TSV daisy chain structures with collective hybrid bonding method. Courtesy of Anne Jourdain of IMEC.

In another study, test dice with Cu-Cu and Cu-Sn TSV's of 10µm and 40µm pitch, respectively, were tacked with high accuracy onto a 300mm landing wafer using a similar polymer. [12]. After tacking and final bonding performed in a wafer bonder, electrical test structures indicated all sites aligned to within about 1.5µm, with maximum die rotation of 0.03 degrees observed.

CONCLUSIONS AND RECOMMENDATIONS

Two key areas of 3D Integration have been explored, namely the removal of metal oxides prior to bonding, and the use of collective hybrid bonding to optimize accuracy and throughput. Solutions have been integrated using a flip chip bonder platform, with a view toward creating technically effective and manufacturable processes. Hardware and methodology have been successfully installed and implemented at customer sites, with plans in place to apply and optimize these solutions in new and existing product lines.

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