Three Chips Stacking with Low Volume Solder Using Single Re-Flow Process

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Abstract

Miniaturized 3D package with shorter distances between chips are needed for the mobile and high frequency applications. Chip-to-chip stacking for 3D packaging using conventional assembly method and single step reflow attachment is the most cost-effective. But fine pitch micro-joints of stacked chip by single re-flow attachment is challenging due to chip movement during stacking processes, which lead to poor assembly yields. This paper reports a method of stacking chips by thermal tacking and permanent joints are formed simultaneously by single re-flow step. Three chips of 12mm x 12mm size with micro bumps at 100um pitch have been assembled using this approach. Low volume of lead free solder (Sn) has been chosen for the micro-bump interconnections between the chips. The thermal tacking conditions and flip-chip assembly process have been studied in details. The micro-joints quality and reliability have been assessed and reported.

Introduction

As the demands for higher wiring connectivity and shorter distances between chips have increased, 3D packaging by stacking the chip one over other is needed. Figure 1 shows the evolution of packaging technology from 2D to 3D.[1] Wire bonding is the most popular method for low-density connections of less than 500 I/0 per chip. However, it will become difficult to meet the increasing frequency requirements and higher I/O connectivity by the peripheral wirebond design for multiple chip packages. 3D packaging using micro bumps and Through Silicon Vias (TSV) is emerging packaging technology to overcome the shortcoming. [2,3]

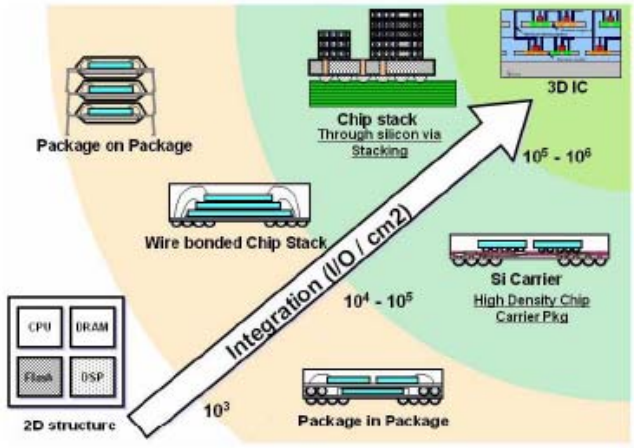


Figure 1: Evolution of Packaging technology

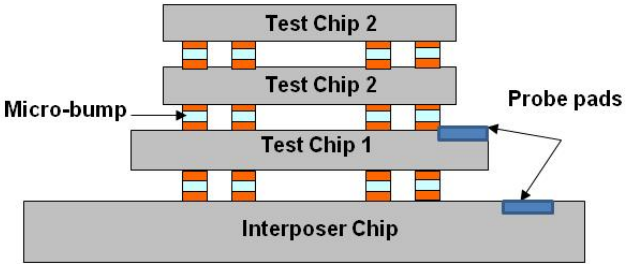
Chip-to-chip stacking using conventional package assembly method / tools is the most cost-effective way of making 3D-Packages. But fine pitch (100um) and low stand-off interconnections between multiple-chips by single re-flow is challenging. Multiple chips can be stacked one over other by sequential manner, but the throughput is an issue. Also the bottom chips experience multiple times of higher temperature, which makes the solder joint with different inter-metallic composition in each stack. Also the joint formed previously melts during the second and third re-flow steps lead to die shift and solder bridging.

Yoichiro Kurita et al reported stacking of 8 chips by thermo-compression method.[4] In this approach, each chip is bonded with the chip below by applying heat and pressure for longer time using low volume of solder. The solder is completely converted into Inter-Metallic Compound (IMC) by the thermo-compression bonding. The IMC doesn't melt during the subsequent bonding. This approach is a sequential process which has a drawback of low throughput. Single step bonding method is desirable for higher thorough put. But the chips are required to be tacked or temporarily bonded with the landing chip or substrate. Then the chip is bonded using a wafer bonder.[5, 6] But this approach require a special material as adhesive layer and wafer bonder to press all the chips to make good contact with the pad and form permanent joints.

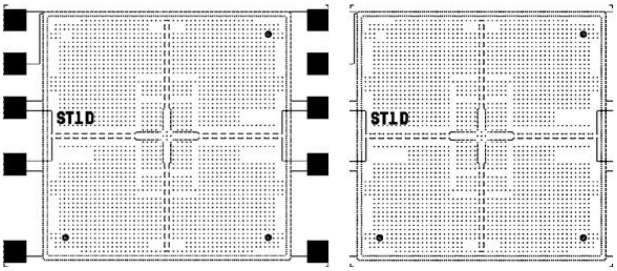
This paper describes a method to stacking three chips by thermal tacking the chip with one another by applying heat & pressure for a short time. The tacking forms a weak joint and hold the chip in place. Then permanent joints are formed by single step re-flow process using five-zone convection re-flow oven. The micro-joint quality and reliability have been evaluated and discussed in this paper.

Test Vehicle Design

A test chip was designed with full array of bumps. All the peripheral bumps and bumps at the critical locations are connected by daisy chain structures to monitor the micro-joint integrity and assembly process. The chip size is 12mm x 12mm x 200um thick with 2714 micro-bump. In general the bump pitch is 100 um except for parts of the inner rows in which the pitch is 200 um. The micro-bump structure is mini-cu pillar of 15um height with 2-4 um of Sn solder cap. Two types of test chip have been designed viz. Test chip 1 with probing pad on the side of the chip to check micro-joint interconnections (15mm x 12mm) and Test chip 2 is 12mm x 12mm. A stack of three chips (one piece of test chip 1 and two pieces of test chip 2) was assembled on an interposer chip. A schematic of the stack is shown in Fig 2.



a. Schematic of the chip stacking



b. Test chip 1 c. Test chip 2

Figure 2: Test vehicle design and stacking arrangement

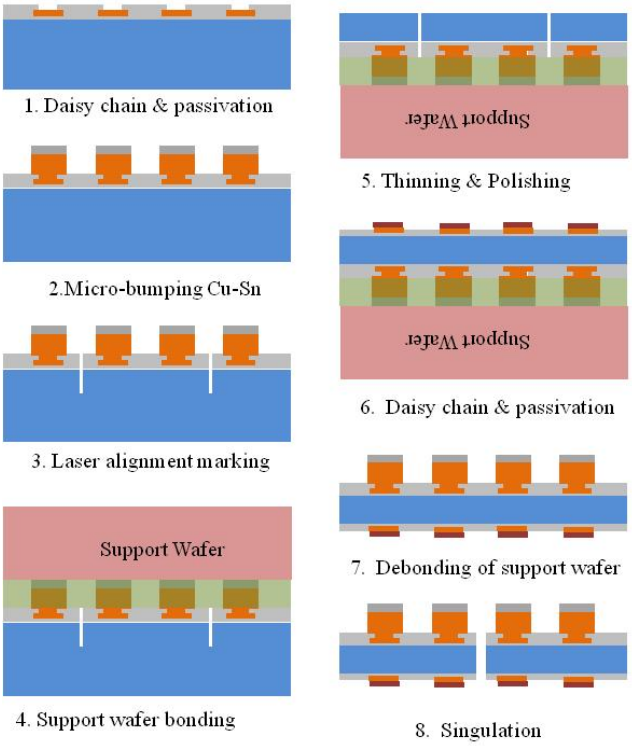


Figure 3: Test chip fabrication process flow

Test Chip Fabrication

The chips were fabricated on 200 mm p-type silicon wafer using a re-distribution and bumping process line. Typical process flow for the test chip fabrication is shown in Fig. 3. One micron thick undoped silica glass (USG) dielectric layer was deposited and followed by Aluminum metal deposition to form daisy chain structure. A final passivation layer of USG/Silicon nitride was deposited. Then microbumps (15um thick Cu and 2um Sn) were electroplated using thick photo-resist. Wafer front to back alignment marks were formed using laser micro-machining. Then wafer was bonded with a 700um thick Si wafer (support wafer) using temporary adhesive from Brewer Science WaferBOND (TM). The test chip wafer was thinned to 200um using a backgrinder and wafer alignment marks were revealed. A dielectric layer was deposited over the back surface of the wafer and patterned. A copper metal layer was electroplated forming complementary daisy chain pattern to the wafer front side. Second passivation layer was deposited, followed by a UBM layer of 4-6um Sn was deposited by electroplating. After the backside processes, the wafer was heated to 200 ºC to soften the temporary adhesive and the wafer was removed from the support wafer. Finally the wafer was diced into individual chips.

Chip to Chips Stacking Approach

We developed a method for stacking multiple chips by temporary thermal tacking and permanent joints formed by convection re-flow process. The chip stacking was done using a Flip-chip bonder (FC150). The chip was pick & placed, then the chip was temporarily tacked to the bottom chip by applying heat & pressure. This approach doesn't require additional step / material compared to other approaches reported using adhesive/glue tacking. Design of experiment was performed to optimize the thermal tacking conditions.

The flip-chip operation was recorded using a high speed video camera. The flip-chip M/C bond head picks up a chip after dipping the bump into flux and align with the interposer chip. The bond head moves and touch-down on the interposer chip. Then heat & pressure was applied on the chip. After the chip placement, the head & table moves up to certain distance slowly, followed by vacuum release and fast retraction of the head to the initial position. The vacuum release after the pick& place introduced disturbing forces on the chip. We observed movement of the chip on lateral direction by 10um to 15um without any holding forces (no flux or tacking) based on the high speed video frame analysis. This study showed that stacking of two or more chips requires additional force to hold the bottom chip in place. The thermal tacking holds bottom chips in the stack during the pick & place operation.

The tacking parameters were evaluated based on the holding force and tacking duration. Longer tacking duration affects the assembly through-put. We evaluated with 5 sec or 10 sec as tacking duration. Samples were prepared by tacking one chip on the interposer chip. The tacking temperature was varied from 240 °C to 280 °C. A sample without tacking (only flux to hold the chip) was prepared as a controlled sample. The thermal tacking forms a weak joint between the chips due to reaction of the Sn on the bump with the pad. The weak joint helps to prevent the chip movement during pick& place operation of the second chip and third chip. Most of the flip-chip bonders available in the market have thermo-compression option, which can be used for the thermal tacking.

The strength of tacking has been evaluated by die shear using Dage 4000. The speed of the shear tool was 100

um/sec. The die shear value with different tacking condition is given in Fig. 4. The die shear value of the controlled sample (without tacking) is only 7.3 grams, which is very low to hold the chip in place during stacking operation. The chip holding force increases with higher tacking temperature and tacking time. Our experimental trials show tacking force of 100grams or above was needed for the three chips stacking. Tacking conditions of 270ºC is selected for the chip stacking.

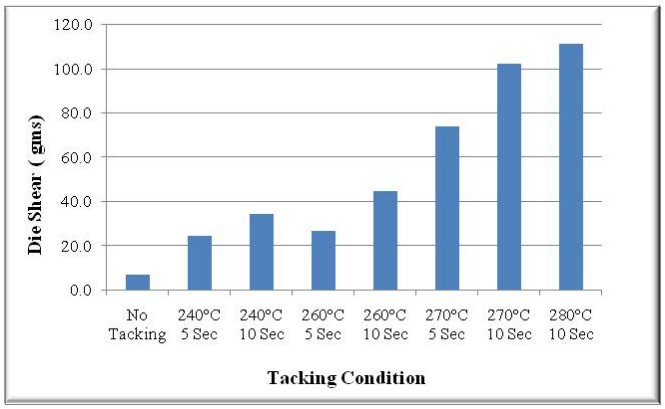


Figure 4: Thermal tacking evaluation results

The bump surface after the die shear was analyzed using SEM and optical microscope. SEM images of the bump are shown in Figure 5. The sheared bump surface with tacking condition of "A" shows no sign of reaction. The sheared bump surface with tacking condition of "B" shows clear sign of shear mark. About 10% of the bump surface at the center has reacted with the pad. Deng et al has reported, time dependent contact angle variation of SnAg solder melted at 270°C has deeper slope compared to the solder melted at 260 °C [7]. Our experiments also show tacking at 270°C shows 2X higher shear value than tacking at 260°C, therefore this has been chosen for this work.

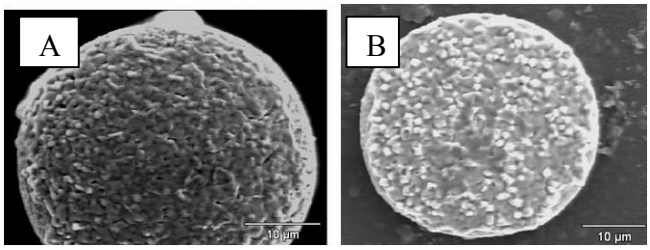


Figure 5: A.) Sheared bump after tacking at 240°C, 10 Sec. B.) Sheared bump after tacking at 270°C, 10 Sec

The FC150 flip-chip bonder has provision to heat chuck and the bonding head. If this approach is extended to chip to wafer assembly, pick & place operation of multiple chips on the entire wafer require longer time. Prolonged heating of the landing wafer lead to pad oxidation or solder reaction with the pad. Therefore we decided to perform thermal tacking only heating the bond head and the chuck is maintained at 50 °C.

Three chips were thermally tacked one over the other and permanent joints were formed by re-flow the stack in a five – zone convection re-flow oven. The re-flow condition was set at 260°C peak temperature for 60 sec above the Sn melting point. The micro-joint electrical continuity was measured and the joint formed between the chips were found good. Also the stacked module was cross sectioned and observed good joints formed in the three stacks as shown in Fig 6. Electrical resistance of the micro-joint was measured using probe station. The electrical resistance of single joint with connecting metal is < 50 m-ohm with 100 mA current. The micro-joint quality was assessed by die-shear test. Samples were prepared with one chip and hot die shear was performed at 200 ºC. The micro-joint after the hot shear was studied and found following failure modes

1. Shear along the inter-metallic of the joint
2. Bump pealing from the chip

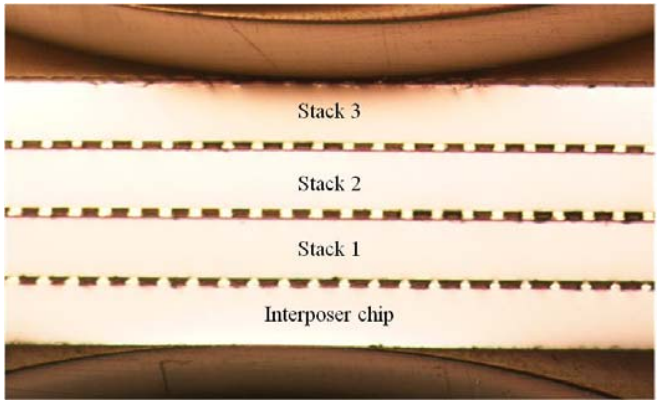
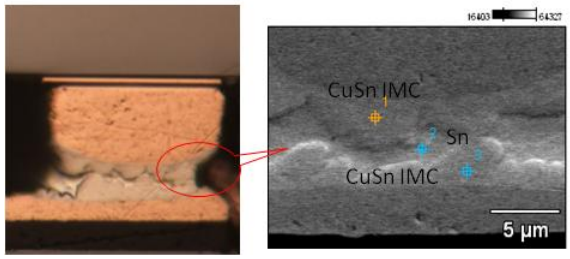
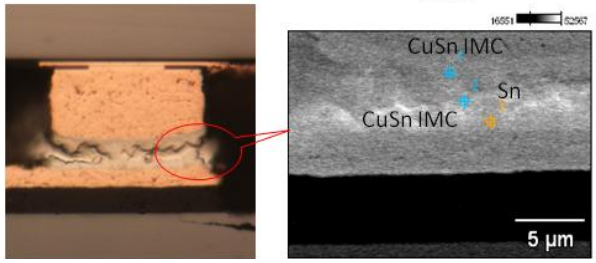


Figure 6: Cross section of three chips stack using thermal tacking and single step re-flow process

The stacked module had been cross sectioned and the micro joint intermetallic was analyzed. More than 50% of the Sn in the joint was converted into IMC. Optical images of the micro-bump show uniform micro-joints in all the three stacks. Elemental composition analysis was performed by EDX and found two phases of CuSn IMC present in the joint. Fig 7 shows micro-joint of stack 1 and stack 3.



a. Cross section of micro-joint in stack 1



b. Cross section of micro-joint in stack 3

Figure 7: Cross section of the Cu-Sn micro joints

Thermo-Mechanical Analysis of Micro Joints

Thermo-mechanical analysis was performed to estimate the stress in the micro-joints. Also the analysis was carried out to determine the effect of joint composition (% Sn & % IMC) on bump stress. The stacking method by single re-flow results in 50% Sn & 50% IMC, but chips stacking by thermo-compression method results in100% IMC. The following assumptions are made in the analysis.

1. Silicon and IMC are not strained beyond their elastic zone.
2. Cu and Sn undergo elastic deformation, followed by plastic deformation.
3. Chip and micro-joints are stress free at 125ºC.

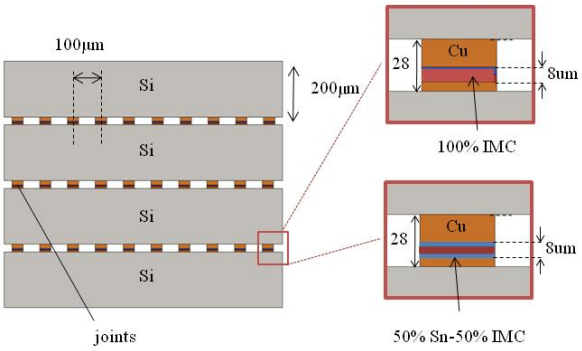


Figure 8: Schematic of the mechanical model structure

A static temperature ramp down analysis from 125ºC to 40ºC was carried out to simulate the thermal-cycle test condition. The material properties used for the analysis are shown in Tables 1.

Table 1 Material properties

Material	Silicon	Sn	IMC	Cu
Young's Modulus (GPa)	130	50	119	130
Poisson Ratio	0.28	0.3	0.309	0.34
CTE (ppm/°C)	2.9@ 25ºC	22	16.3	18
Plastic properties (MPa)	35@ 0ε			137.9 @ 0 ε 271.5 @ 0.1ε

The micro joints were stressed during the temperature ramp down as a result of the different coefficients of thermal expansion of the materials that make up the joint (i.e. Cu, Sn and IMC). The stress contours of single joints from the models are shown in Fig. 9. The highest stress is located at the corner of the IMC in the micro-joint. There is higher stress at the top of the IMC region of the joint (compared to the bottom) because the top Cu post being thicker, which contracts more than the bottom Cu UBM. Failure is expected to initiate at this interface between the Sn and IMC. The maximum shear stress for 100% IMC joint is 79Mpa and 50% IMC joint is 78MPa. The IMC volume in the micro-joint is small compared to the entire joint and no thermal mismatch between the chips, which resulted in comparable shear stress for both the methods.

Model	100% IMC	50% IMC
Max S12 (MPa)	79	78

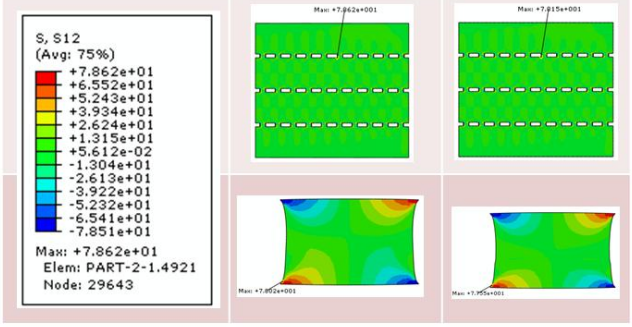


Figure 9: Stress contours in the chips stack

Micro-Joint Reliability Assessment

Samples of three chips stack without underfill were prepared for micro-joint reliability evaluation. We subjected the samples to thermo-mechanical stressing test of thermal cycle (-40 ºC to 125 ºC). The interconnect daisy chain resistance was monitored at regular intervals and one sample failed after 500 cycles. Table 3 shows the electrical resistance of the chip 1 daisy chain in thermal cycle test

Table 2: Thermal cycle reliability test results

Sample no.	250 cycles	500 cycles	750 cycles	1000 cycles
1	5.9	6.1	7.3	16.2
2	7.9	open	open	open
3	9.2	9.3	9.3	9.4
4	8.5	8.6	10	10

Figure 10 shows the cross section of the failed sample. The failed micro- joint shows large voids present in the joint compared to the adjacent joint. The time zero void present in the joint reduced the joint cross section and thermo-mechanical stress during the thermal cycle test caused the joint failure. We observed non uniform bump height / shape after the plating. Micro-bump assembly using low volume of solder with non-uniform bump height / shape is tending to form void due to insufficient solder to accommodate the variation. It is recommended to control the bump variation or planarize the bump especially for the micro-joint with low volume solder for better assembly yield.

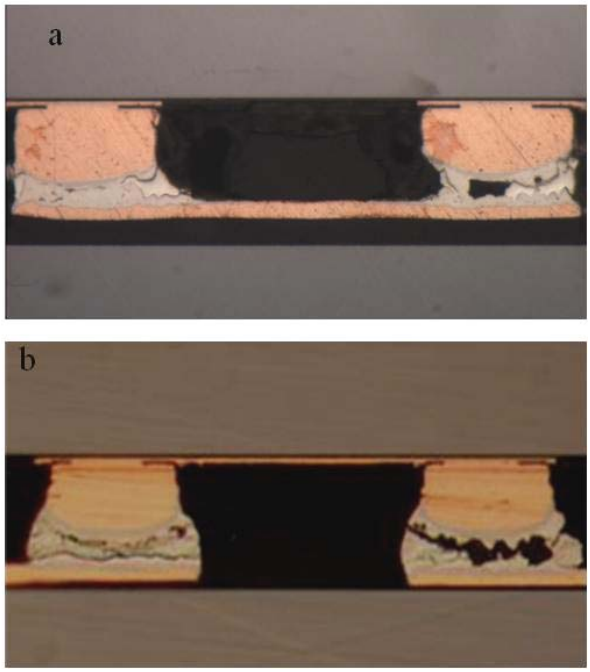


Figure 10: Micro-joint cross section: a.) Micro-Joint after assembly showing void due to irregular bump, b.) Failed bump after the TC test

The Cu-Sn micro-joint was subjected to high temperature (150 ºC) for 1000 hrs to assess the intermetallic growth. The solder pad on the chip is 5um thick Cu with 4um thick Sn layer. There is no Ni barrier layer between the Sn and the Cu pad. Therefore prolonged reaction of Sn with the Cu pad converted the pad completely into IMC. But the bump side has sufficient Cu after 1000 hrs of high temperature storage test. Fig 11 shows the micro-joint after re-flow attachment and after 1000 hrs. of high temperature storage.

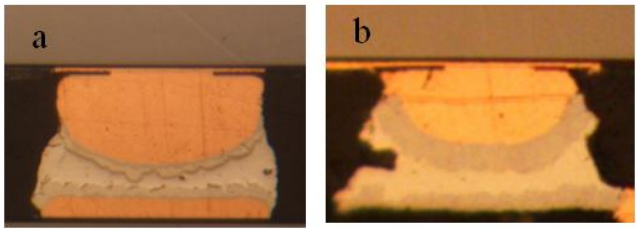


Figure 11: Micro-bump intermetallic growth: a.) Micro-joint after assembly, b.) Micro-joint after 1000hrs of high temperature storage at 150 ºC

Conclusions

This work has developed an assembly method for stacking three chips using thermal tacking and single step re-flow attachment. The method reduces the process cost compared to sequential chip attachment method / gang bonding method. This approach doesn't require special tool or material. The thermal tacking conditions have been evaluated and an optimum tacking temperature 270 ºC was selected for the chip to chip stacking. Demonstrated micro-bump interconnections (1880 bumps/ cm^2) at 100um pitch using Cu-Sn. Micro-joint electrical resistance, joint quality have been characterized. The micro-joint reliability in thermal cycle test condition has been studied.

Acknowledgments

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