Low Temperature Bonding of High Density Large Area Array Interconnects for 3D Integration

Jason D. Reed, Matthew Lueck, Chris Gregory, Alan Huffman, John M. Lannon, Jr., and Dorota S. Temple

Center for Materials and Electronic Technologies, RTI International

Research Triangle Park, NC 27709 USA

(919) 248-9217 desk, (919) 672-5031 cell, jareed@rti.org

Abstract:

The results of bonding and stress testing of Cu/Sn-Cu bonded dice and Cu-Cu thermocompression bonded dice at $10\mu m$ and $15\mu m$ pitch in large area arrays are shown. The interconnect bonding process pressure and temperature required for the formation of low resistance (< $100~m\Omega$), high yielding (99.99% individual bond yield), and reliable interconnects is described. In the case of Cu/Sn-Cu, use of a mechanical key was found to improve yield. A run of 22 consecutive bond pairs was made with the mechanical key, resulting in 98% aggregate channel yield at $10\mu m$ pitch in area arrays containing 325,632 individual bonds per die to achieve an interconnect density of 10^6 / cm². SEM cross sections of Cu/Sn-Cu and Cu-Cu bonded samples and EDS analysis of Cu/Sn intermetallic compounds both before and after stress testing are presented. The results of thermal cycling and humidity-temperature testing on electrical yield and resistance are presented for Cu/Sn-Cu with underfill. Comparison of the electrical and shear test performance of Cu/Sn-Cu and Cu-Cu is made. Low temperature bonding (at 210° C, below the melting point of tin) is demonstrated to produce high electrical yield, high shear strength and similar intermetallic compound formation to devices bonded at 300° C. The low temperature process may prove useful for integrating IC devices that have low thermal budgets.

Keywords: 3D IC thermocompression bonding, high-density die-to-die interconnect.

Introduction

High density interconnects enable further miniaturization, reduced power consumption and functionality microsystems. of Heterogeneous technologies such as sensors, imaging arrays and others can be implemented in their optimal process flows and then integrated using the high density interconnects. Several research groups have presented work in the area of metal-metal interconnects [1-4]. In this paper we review the status of the development of high yield bonding at 10µm pitch, highlighting the use of a mechanical key to prevent misalignment and slippage during thermocompression. These results represent an order of magnitude increase in density (10^6 interconnects per square centimeter) as compared with the state-ofthe-art in traditional flip-chip bonding.

Design and Fabrication

In this work, three test vehicle devices were fabricated, based on the following approaches:

- 1. Cu/Sn Cu bonding without a mechanical key.
- 2. Cu/Sn Cu bonding with a mechanical key (explained below) on one of the dice to prevent

misalignment and slippage during bonding. The keys also prevent Sn from potentially bridging across bonds, an issue noted in previous work [5].

3. Cu - Cu thermocompression bonding with chemically-mechanically polished (CMP'd) Cu bond pad surfaces and with CMP'd Cu to as-plated Cu bond pad surfaces. The as-plated Cu pads also had a mechanical key.

These approaches were designed to be compatible with post-CMOS processing on 200mm wafers. To test these bonding approaches, RTI fabricated test vehicles containing 512 x 640 area arrays of bond pads with 10µm pitch on 200mm diameter wafers. Each test vehicle provided 256 daisy chain channels, with 1272 individual chip-to-chip bonds per channel, giving good spatial resolution of potential defects.

For the Cu/Sn-Cu vehicle without a mechanical key, the bottom routing layer was formed using lithography, Ti/Cu/Ti evaporation and liftoff. Oxide was deposited by plasma enhanced chemical vapor deposition (PECVD) and patterned by reactive ion etching (RIE). Bond pads were formed by the combination of seed layer sputtering, lithography,

electroplating and seed layer etching. The seedlayer etching was done with an ion mill. The top die consisted of $4\mu m$ diameter Cu pads plated $4\mu m$ thick. The bottom die consisted of $6\mu m$ diameter pads plated with $4\mu m$ of Cu and $2\mu m$ of Sn.

For Cu/Sn-Cu with a mechanical key, the top die was fabricated in a process similar to the one described above, with $4\mu m$ diameter pads plated with $3.5\mu m$ of Cu and $2.5\mu m$ of Sn. The bottom die consisted of metal links terminated with $6\mu m$ diameter pads that were plated with $4\mu m$ of Cu and then coated with BCB. Vias were etched in the BCB to create openings for bonding to the bottom pads. The BCB sidewalls created a mechanical key to prevent lateral slippage during bonding. The fabrication sequence is depicted in Fig. 1.

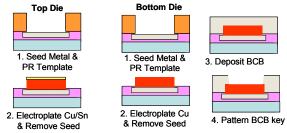


Fig. 1. Schematic diagram of top die (left) and bottom die (right) used to fabricate mechanically keyed Cu/Sn-Cu interconnect test vehicles with 10µm pitch in area arrays of 512 x 640.

An SEM of an individual Cu/Sn pillar, an SEM of the $10\mu m$ pitch array and a scaled schematic diagram of the top dice pillars are shown in Fig. 2.

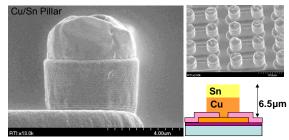


Fig. 2. (left) SEM of top die pillar after tin plating, (above right) SEM of the top die 10µm pitch array, (below right) scaled drawing of Cu/Sn pillars (3.5um copper and 2.5um tin).

For Cu-Cu thermocompression bonding of CMP'd Cu surfaces, the top and bottom pads were formed in 5μ m thick SiO_2 by RIE, filled with Cu by Ti/Cu seed sputtering and Cu blanket electroplating and then planarized with CMP to remove the Cu overburden. Pad diameters for top and bottom die were 4μ m. After CMP, the oxide was partially etched (recessed) to expose the tops of the pillars for bonding. As noted above, in this vehicle the Cu bonding surfaces are both produced by CMP. A

schematic diagram of the fabrication sequence is depicted in Fig. 3.

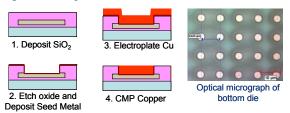


Fig. 3. Schematic diagram of top and bottom dice (left) and optical microscope image (right) used to fabricate Cu-Cu thermocompression test vehicles with 10µm pitch in area arrays of 512 x 640.

For Cu-Cu thermocompression bonding with CMP'd Cu to as-plated Cu, the top die was formed by CMP as above. The bottom die consisted of metal links terminated with 6μm diameter pads that were plated with 4μm of Cu and then coated with BCB. Vias were etched in the BCB to create openings for the top pads to bond to the copper bottom pads. After fabrication, roughness and uniformity were characterized as reported in [6].

Sample bonding was performed in a Suss Microtech FC150 precision bonder with split optics, allowing for alignment in "cold placement" with accuracy of $\pm 1~\mu m$.

Cu/Sn-Cu Bonding Temperature Optimization

Prior to bonding, the Cu bottom pads were stripped of copper oxide with a dilute acid solution. The Cu/Sn top pads were fluorine plasma treated with the PADS process (Plasma Assisted Dry Soldering), which enables fluxless bonding [7]. The tin pads were flattened using an in situ coining process. A schematic diagram of the top and bottom dice in position for bonding is shown in Fig. 4.

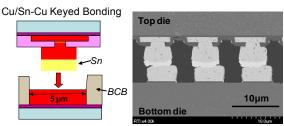


Fig. 4. Schematic diagram of die in position for bonding (left) and bonded die (right) used to fabricate mechanically keyed Cu/Sn-Cu interconnect test vehicles with $10\mu m$ pitch in area arrays of 512×640 .

For Cu/Sn-Cu dice without mechanical key, six consecutive die pairs with pads on $15\mu m$ pitch were bonded using 275° C bonding temperature for 180s and bonding pressure of 5×10^6 kg/m². All six pairs exhibited electrical opens. Die shear and inspection revealed that the top pads had slipped laterally off the

bottom pads during bonding. This result confirmed the expectation that without mechanical keying, the Cu/Sn bonding process will be difficult to scale to pitch dimensions below approximately 20 μ m due to slippage during bonding [8].

For Cu/Sn-Cu dice with a mechanical key, the effect of bonding temperature was studied on samples at 10 µm pitch. The bonding process was performed using a pressure of $5*10^6$ kg/m² at a temperature of 275 and 300°C for 180s under N₂ purging. Electrical testing showed high channel yields were achieved at both 275°C and 300°C bonding temperature. Average channel yield (each channel contains 1272 bonds) was 93% and did not depend strongly on bonding temperature. The parts bonded at 300°C had similar median resistance (103 mΩ/bond, with standard deviation of 8mΩ) to those bonded at 275°C (96 mΩ/bond, with standard deviation of 15mΩ). Resistances include the wiring and pad structures. The two results are within one standard deviation.

Cu/Sn-Cu Bonding Qualification Run

To demonstrate the repeatability and test the robustness of the Cu/Sn-Cu bonding process with mechanical keying, a qualification of 22 bonding runs at $10\mu m$ pitch was done. This run used standard bonding conditions: in situ coining of the Sn, followed by bonding at 275° C for 180s at a pressure 5×10^6 kg/m² (32.2kgf) over an array of pads 512 x 640 on a $10\mu m$ pitch.

After bonding, electrical testing on the 22 bonded pairs was done and the median channel yield was 98.4% and the median channel resistance was 65 Ω . These results are plotted in Figs. 5 and 6. Each channel contains 1272 interconnections in a daisy chain format. The average resistance of each interconnect including the wiring and pad structures was <100 m Ω .

The wiring and pad structures were modeled and their calculated resistance was subtracted from the raw resistance value to give approximately $20m\Omega$ per bond and a contact resistance of 5×10^{-8} Ohm-cm². This result is compared with Cu-Cu bonding in the Comparison of Electrical Results Section.

A yield map of six consecutively bonded Cu/Sn-Cu 10µm pitch dice is shown in Fig. 7. The blue lines mark the channels that were electrically open after bonding. The location of defects is not random, with most defects clustered near the device edges. The opens are most likely due to handling damage.

Aside from the edge defects, assuming that each open channel is caused by a single open bond, then the individual bond yield is >99.99%.

Samples were cross-sectioned for SEM and energy dispersive spectroscopy (EDS) analysis. SEM analysis of cross-sections was done with a

backscattered electron detector. Quantitative EDS was performed to identify intermetallic phases at the bondline (indicated in Fig. 8). The IMC is the Cu_3Sn phase. This phase is thermodynamically stable up to $650^{\circ}C$. There was no Cu_6Sn_5 or unreacted Sn.

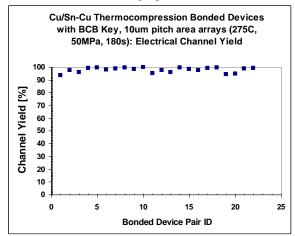


Fig. 5. Channel yield for consecutively bonded Cu/Sn-Cu dice. Median channel yield was 98.4%.

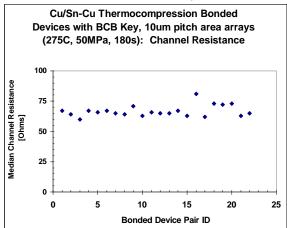


Fig. 6. Graph of median channel resistance (includes bonds, link wiring and probe pads) for 22 consecutively bonded Cu/Sn-Cu devices. Median channel resistance was 65 Ω .

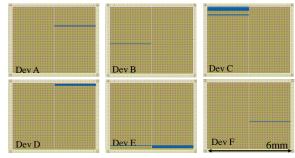


Fig. 7. Graphical map of defective channels in six consecutively bonded $10\mu m$ pitch samples. Blue lines show electrical opens. Individual bond yield is >99.99%.

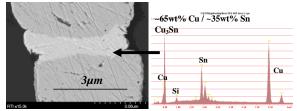


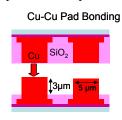
Fig. 8. Cross sectional SEM of the $10\mu m$ pitch Cu/Sn-Cu die pairs after bonding. EDS was performed in the marked region to identify the IMC as Cu₃Sn. There was no unreacted Sn or Cu₆Sn₅ present.

The BCB mechanical key was important for achieving high yield by constraining slippage during bonding. The presence of the Sn layer was important for achieving high yield by accommodating the non-planarity of the bonding surfaces through in situ coining prior to bonding.

Cu-Cu Bonding (CMP'd Cu to CMP'd Cu)

CMP'd Cu to CMP'd Cu bonding was performed with varied mechanical pressure and temperature. Typical bonding conditions were a temperature of 325° C and a pressure of 32.2 kgf, equivalent to 5×10^{6} kg/m². As with the Cu/Sn-Cu test vehicle, this vehicle had 512×640 array of pads on 10μ m pitch for an interconnect density of 10^{6} /cm², as shown schematically in Fig. 9.

Electrical measurement of bond chains gave a resistance of 95.9 m Ω and 44.5% channel yield (1272 daisy chained connections per channel). This channel yield was much lower than the yields achieved with Cu/Sn-Cu bonding primarily due to non planarity of the Cu pillars as a result of dishing during the CMP planarization process.



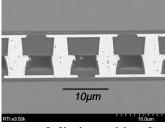


Fig. 9. Schematic diagram of die in position for bonding (left) and bonded die (right) used to fabricate Cu-Cu thermocompression bonded interconnect test vehicles with $10\mu m$ pitch in area arrays of 512×640 .

The amount of non planarity of the Cu pillars was measured after CMP. For the corner pillar, the average dishing was $0.35\mu m$ below the die center. The minimum value observed was $0.20\mu m$ and the maximum was $0.60\mu m$. The corner pillar exhibited a larger amount of dishing because it is the most exposed pillar in the die during CMP. The amount of

edge pillar and corner pillar dishing did not depend on wafer location to a significant degree.

The non-planarity reduced bonding yield by preventing physical contact of edge pillars during the thermocompression process. The effect of the nonuniformity can be seen in Fig. 10 which shows CMP Cu to CMP Cu at $10\mu m$ pitch at the center of the die (left image) and the edge (right image). At the center the Cu to Cu thermocompression bond has been made, but at the edge the nonuniformity in the copper pillar created a gap between the Cu surfaces.

Prior to bonding, the oxide on the bottom die was recessed by $3\mu m$ to expose the copper pillars, and the oxide on the top die was recessed to expose the copper pillars by $0.2\mu m$. During the bond process at $325^{\circ}C$, copper oxide forms on the exposed surfaces, visible in the image. Optical images of these oxidized surfaces after shear testing are shown in the Shear Testing results section.



Fig. 10. SEM cross section thermocompression bonded sample with CMP Cu top die and CMP Cu bottom die.

The recess (or dishing) occurred during the CMP process and may be reduced by adding dummy features or pillars outside the active die area. The lack of dummy features caused the outer rows of Cu pillars to recess more than the inner rows, resulting in a non planar bonding surface.

The majority of the bonds formed were good in each channel, as confirmed by cross-sectional SEM, but the links at the die edge were electrically open due to the edge dishing. This was confirmed by optical inspection after shear testing (see Shear Testing section).

Cu-Cu Bonding (CMP'd Cu to as-plated Cu)

In part to try to achieve higher channel yield with Cu-Cu, devices with CMP'd Cu on the top die were bonded to devices with plated Cu and BCB mechanical key on the bottom die. This process is shown schematically and with SEM in Fig. 11. This approach was taken because by mating the CMP Cu die with the plated Cu die, the non-uniformities in thickness were expected to offset partially. The CMP Cu pillars are lower at the die corners due to CMP dishing, whereas the plated Cu pillars are higher at the corners.

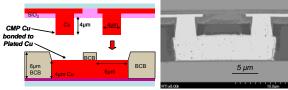


Fig. 11. Schematic and SEM cross-section of CMP Cu to Plated Cu metal bonding at 15µm pitch.

Typical bonding pressure was 10.5 kg/m^2 (30 kgf) for the 15µm pitch samples. Samples were bonded at 325°C for 900s. Electrical measurements gave 94.8% channel yield with median resistance of 62 Ω , for a resistance of 73 m Ω per bond and routing segment. An SEM cross-section is shown in Fig. 12.

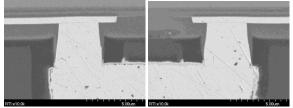


Fig. 12. Cross section of CMP'd Cu to as-plated Cu bonded device with 15µm pitch.

Underfill

Cu/Sn-Cu parts were underfilled with epoxy to prevent oxidation of exposed copper surfaces and increase bond strength. The epoxy (LORD Exp A) was unfilled, with low viscosity (5600 cPs at 25°C) and low Young's Modulus (0.2 GPa at 100°C). Seven Cu/Sn-Cu bonded samples were underfilled. The underfill process consisted of a vacuum-assisted application of the epoxy at 60°C to promote capillary flow, followed by oven cure (1hr at 180°C).

Reliability Testing

The Cu/Sn-Cu devices with underfill were subjected to 100 thermal cycles (+125°C to -40°C) and re-probed, and then 100 hours 85% RH / 85°C stress testing and reprobed. The results are shown in Table I. There were no significant changes in the electrical yield or channel. The average yield was 93% before and after stress testing and the average resistance was 156 Ω before and after stress testing.

Table I: Electrical performance of $10\mu m$ pitch Cu/Sn-Cu bonded devices before and after 100 thermal cycles (-40°C to +125°C) and 100 hours 85% RH / 85°C stress testing.

Electrical Connectivity (% cha			% channels)	nnels) Median Channel Resistance (Ω)			
Sample	As-Bonded	Post Thermal Cycling	Post 85/85 Stress Testing	As-Bonded	Post Thermal Cycling	Post 85/85 Stress Testing	
66	93	92.6	92.6	150	146	146	
71	89.5	89.5	89.1	155	151	150	
72	94.1	94.5	94.5	138	137	141	
73	96.5	96.5	96.5	151	152	153	
75	92.6	92.6	92.6	157	158	155	
78	93.4	93.4	93.4	172	176	176	
79	89.1	89.1	89.1	168	169	173	

After stress testing, samples were cross-sectioned for SEM and EDS analysis. EDS was used to quantify the elements in the IMC phase at the bonding interface, as marked in Fig. 13. The IMC is the Cu_3Sn phase. There was no Cu_6Sn_5 or unreacted Sn. There was no visible corrosion on underfilled devices and the bondline has not changed significantly after stress testing.

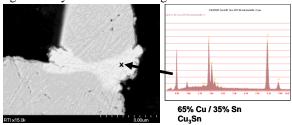


Fig. 13. IMC composition has not changed after 100 thermal cycles (- 40° C to + 125° C) and 100 hours 85% RH / 85°C stress testing.

Comparison of Electrical Results

Table II summarizes and compares the electrical resistance results for three types of metal to metal bonding: Cu/Sn – Cu, CMP Cu – CMP Cu, and CMP Cu – Plated Cu. As expected the contact resistance of the Cu-Cu bonded samples was lower because there is no intermetallic compound formed. The Cu/Sn intermetallic increases the bond resistance by a factor of approximately three compared with CMP'd Cu-Cu. The total bond resistance for Cu/Sn-Cu bonding remains less than $100 m\Omega$ per bond.

Table II. Contact resistance comparison of three metal to metal bonding types.

tin ce metar to metar bonding types.						
Bond Type	Array size	Bond Diameter	Bond Temp	Bonding Pressure	Yield	Contact resistance
		(um)	[°C]	[MPa]		(10 ⁻⁸ Ω–cm ²)
Cu/Sn to Plated Cu w/ BCB key	640x512 10 um pitch	4	275	50	98% channel 99.99% ass. point defects	4.7
CMP Cu to CMP Cu	640x512 10 um pitch	4	300	50	44.5% channel.	1.5
CMP Cu to Plated Cu w/ BCB key	430x344 15 um pitch	4	325	100	94.7% channel 99.99% ass. point defects	2.7

Comparison of Shear Testing Results

Table III summarizes and compares the bond strength results for the three types of metal to metal bonding in this study: Cu/Sn – Cu, CMP Cu – CMP Cu, and CMP Cu – Plated Cu. Die shear strength was measured using a Royce 550 instrument with maximum range of 10kg. The devices were not underfilled for this test. All three types of samples exhibited a bond strength of approximately 8kg +/-1kg. For this die size, the minimum shear strength specified in MIL-STD-883E is 2.5kg. Failure occurred at the bond interface, as shown in Figs. 14 and 15.

Table III. Comparison of the bond strength as measured by shear testing for three types of metal to metal bonding: Cu/Sn - Cu, CMP Cu - CMP Cu, and CMP Cu - Plated Cu.

Bond Type	Array size	Bond strength	
Cu/Sn to Plated Cu w/ BCB key	640x512 10 um pitch	Die shear strength of 8.54 kg (median). Min = 3.34kg; Max > 10kg (n=6)	
CMP Cu to CMP Cu	640x512 10 um pitch	Die shear strength of 8.53kg (median). Min = 5.63kg; Max > 10kg (n=4)	
CMP Cu to Plated Cu w/ BCB key	430x344 15um pitch	Die shear strength of 8.7kg (median). Min = 7.4kg; Max > 10kg (n=2)	

Cu/Sn-Cu Shear Testing

Fig. 14 shows representative top and bottom die surfaces from a Cu/Sn-Cu part after shear testing. The bottom die, right, shows the mechanical BCB key (dark circles around copper landing pads). Sn is visible on the copper pads and it can be seen to be offset towards the upper right corner, where further slippage was restrained by the BCB mechanical key. Shear failure occurred in the Cu/Sn IMC. The shear strength was above 10 kg.

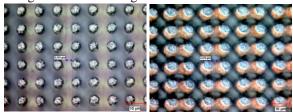


Fig. 14. Optical micrographs of a 10µm pitch die after shear test. Left: Top die. Right: Bottom die.

Cu - Cu Shear Testing

Fig. 15 shows representative top and bottom die surfaces from a CMP Cu – CMP Cu part after shear testing. The shear test result was 6 kg. All of the pads in this photo show unoxidized copper at the Cu-Cu bond. Shear failure occurred at the bondline.

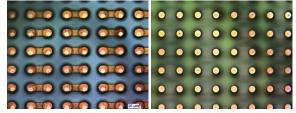


Fig. 15. Optical micrographs of a typical plated Cu (bottom die, left) to CMP Cu (top die, right, same scale) after shear testing.

Fig. 16 shows the bottom die surface for a Cu–Cu part after shear testing, revealing that the corner and edge pads on the device did not bond, as shown by the surface oxidation on the pads. The lack of metal-

metal bonding was caused by the within-die nonuniformity caused by dishing during CMP.



Fig. 16. CMP Cu – CMP Cu device after shear testing, showing oxidized bond pads along the edges and corner of the Plated Cu bottom die after shear testing.

Low (210°C) Temperature Bonding at 25µm Pitch

To explore the feasibility of low temperature bonding, a set of devices was bonded at 210°C and compared with a set of devices otherwise similar but bonded at standard temperature (300°C). These devices were similar in design to the devices tested for reliability above (325,632 interconnects in area array format) but were 25 μm pitch instead of 10 μm . The devices were measured for electrical yield, shear strength, and were cross sectioned for SEM and quantitative EDS analysis.

For both 300°C and 210°C bonding, electrical testing showed high channel yields were achieved. A summary of the electrical results is shown in Table IV. Average channel yield (each channel contains 1272 bonds) was 87%. The median resistance per bond was 127 m Ω /bond which includes the wiring and pad structures.

Table IV. Comparison of electrical yield and resistance of Cu/Sn-Cu devices bonded at standard temperature (300°C) and at 210°C.

standard temperature (500°C) and at 210°C.					
	Devices Bonded at 300°C	Devices Bonded at 210°C			
Sample Size	6	7			
Electrical Channel Yield	87.7%	86.9%			
Median Channel Resistance [Ω]	162	167			
Standard Dev. of Resistance $[\Omega]$	54.0	57.9			

In terms of yield and resistance the electrical behavior of the two sample sets was not significantly different. Graphical maps of the Cu/Sn-Cu electrical yield show a random distribution, indicating a lack of misalignment, across-die nonuniformity or other systematic defects. Opens are most likely due to point defects. Individual bond yield is higher than 99.99%. Fig. 17 shows a graphical map of the open channels on typical devices bonded at 300°C and 210°C. Horizontal black lines mark channels that were open after bonding.

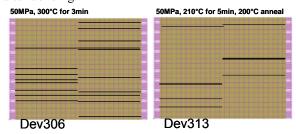
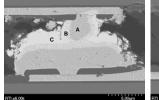


Fig. 17. Graphical yield map of electrically open channels on standard (300°C) bonded device (left) and low temperature (210°C) bonded device.

Fig. 18 shows cross-sectional SEMs of dice bonded at 300°C and 210°C. The 300°C bonded sample used the standard process conditions described above. The 210°C sample was bonded at 210°C for 5 min using 50MPa of pressure and then oven annealed at 200°C for 20 minutes in $N_{\rm 2}$ atmosphere without pressure.



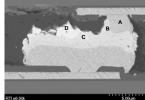


Fig 18. SEMs of samples bonded at 300°C (left) and 210°C (right). Region D above right marks the location of unreacted Sn.

Quantitative energy dispersive x-ray spectroscopy (EDS) was performed on cross-sections to identify the different Cu/Sn intermetallic compounds that are present in the bonds. The four different material regions, labeled A, B, C, and D in Fig. 18 above, were analyzed by EDS.

The sample bonded at 300° C did not exhibit unreacted Sn, whereas the sample bonded at 210° C exhibited a region of unreacted Sn (region D in Fig. 18). The Cu₃Sn phase (B) and Cu₆Sn₅ phase (C) are present in both. In the 210° C sample, the Cu₃Sn phase on top and bottom Cu pillars is separated by a thin $(0.2\mu\text{m})$ Cu₆Sn₅ intermetallic.

Shear testing of the 300°C and 210°C bonded devices was performed. The shear test result was \geq 10 kg for both types.

Low (210°C) Temperature Bonding at 10µm Pitch

To demonstrate the repeatability and test the robustness of the low temperature Cu/Sn-Cu bonding

process at $10\mu m$ pitch, a qualification of seven bonding runs was done. This run used the low temperature bonding conditions: in situ coining at room temperature with 40kgf force, bonding at 210°C for 180s at 5×10^6 kg/m² pressure (32.2kgf) over a 512×640 array on $10\mu m$ pitch. Post bond annealing was performed at 200°C for 20 minutes.

After annealing, electrical testing on the seven bonded devices was done and the median channel yield (1272 daisy chained interconnects/channel) was 92.2% and the median channel resistance was 86 Ω . These results are plotted in Figs. 20 and 21. The average resistance of each interconnect including the wiring and pad structures was 68 m Ω .

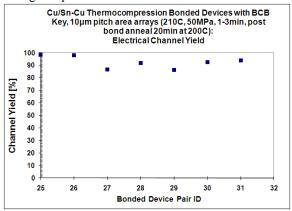


Fig. 20. Graph of channel yield for 7 consecutively bonded Cu/Sn-Cu dice at 210°C at 10μm pitch. Median channel yield was 92.2%.

Fig. 22 shows a cross-sectional SEM of a 10μm pitch device bonded at 210°C showing similar structure to devices bonded at 300°C. Quantitative energy dispersive x-ray spectroscopy (EDS) was performed on the cross-section to identify the Cu/Sn intermetallic compound present in the bond.

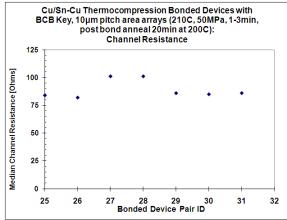


Fig. 21. Graph of median channel resistance (includes bonds, link wiring and probe pads) for 7 consecutively bonded Cu/Sn-Cu dice at 210°C.

EDS spectra and quantitative results for $10\mu m$ pitch bonded sample, at the bondline, showed 61% wt. Cu and 39% wt. Sn, indicating the Cu_3Sn intermetallic phase. There is no Cu_6Sn_5 intermetallic phase or unreacted Sn present.

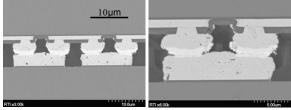


Fig 22. Cross-sectional SEM of sample with 10 μ m pitch bonded at 210°C.

Shear Testing of Cu/Sn-Cu Bonded at 210°C

Fig. 23 shows representative top and bottom die surfaces from a Cu/Sn-Cu part at 10μm pitch bonded at 210°C after shear testing. The bottom die, right, shows the mechanical BCB key (dark circles around copper landing pads). Cu/Sn intermetallic is visible on the copper pads. Shear failure occurred in the Cu/Sn IMC. The shear strength was 6.0 kg, exceeding the 2.5kg specification without underfill.

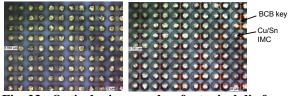


Fig. 23. Optical micrographs of a typical die from the qualification group (Device 501, 10μm pitch Cu/Sn-Cu bonded at 210°C) after shear testing. Left: Top die. Right: Bottom die.

Conclusion

We have demonstrated a high yielding bonding process for the fabrication of die-to-die interconnects in dense area arrays at 10µm pitch. Fabrication and bonding are post-CMOS compatible. The process is based on Cu/Sn-Cu solid liquid diffusion bonding and was performed at a temperature of 275°C. Use of a mechanical key created by patterning an overcoat of BCB was found to improve yield. Bonded samples, underfilled with epoxy to prevent oxidation of Cu pads, were subjected to thermal cycling and humidity-temperature testing. No significant changes in performance occurred as a result of the test

Cu-Cu thermocompression bonding resulted in demonstrated high yield on individual devices, but not on long runs of consecutive bonds. The lower average yield is due to the dishing obtained during the CMP of Cu pads. This dishing while difficult to eliminate completely can be reduced by laying out the bond pad arrays such that the area density of metal changes gradually between the array and field

regions. Comparison of the electrical and shear test performance of Cu/Sn-Cu and Cu-Cu bonds shows that highly conductive ($<100 \text{m}\Omega$) and mechanically strong (8kg for \sim 6 mm x 5 mm die) bonds can be achieved in both metal systems.

Low temperature bonding in Cu/Sn-Cu devices (at 210°C, below the melting point of tin) was demonstrated to produce high electrical yield, high shear strength and similar IMC formation to devices bonded at 300°C. Such a process may prove useful for bonding dice that have low thermal budgets such as memory or detectors.

Acknowledgments

The authors gratefully acknowledge the financial support of DARPA. The authors thank RTI staff Scott Anderson and Targia Green for lithography, Dana Fox for cross-sectioning and SEM/EDS and Matt Fabean for electrical testing. The authors thank Russ A. Stapleton of LORD Corporation for underfill materials and discussions.

References

- [1] 1. K. Tanida, M. Umemoto, Y Tomita, M. Tago, Y Nemoto, T. Ando, and K. Takahashi, Proc. of 2003 Electronic Components and Technology Conference, New Orleans, May 2003, pp. 1084-1089.
- [2] A. Klumpp, R. Merkel, R. Wieland, and P. Ramm, Proc. of 2003 Electronic Components and Technology Conference, New Orleans, May 2003, pp. 1080-1083.
- [3] S. Pozder, A. Jain, R. Chatterjee, Z. Huang, R. Jones, E. Acosta, B. Marlin, G. Hillman, M. Sobczak, G. Kreindl, S. Kanagavel, H. Kostner, S. Pargfrieder, Proc. of 11th IITC 2008, pp 46-48.
- [4] J. Lannon Jr., C. Gregory, M. Lueck, A. Huffman, and D. Temple, Proc. of 2009 Electronic Components and Technology Conf., San Diego, May 26 - 29, 2009.
- [5] A. Huffman, M. Lueck, C. Bower, D. Temple, Proc. 2007 Electronic Components and Technology Conference, Reno, NV, May 29 -June 1, 2007.
- [6] J. Reed, M. Lueck, C. Gregory, A. Huffman, J. Lannon, and D. Temple, Proc. 2010 Electronic Components and Technology Conference, LV, NV, June, 2010.
- [7] A. Huffman, J. Lannon, M. Lueck, C. Gregory, and D. Temple, Materials and Technologies for 3D Integration, MRS Symposium Proceedings, Vol. 1112, Boston, December 2008, pp 107-120.
- [8] J. Reed, M. Lueck, C. Gregory, A. Huffman, J. M. Lannon, Jr., and D. Temple, Proc. of 13th IITC San Francisco, June 2010.