Electrical characterization of high count, 10 µm pitch, room-temperature vertical interconnections

François Marion, Damien Saint Patrice, Manuel Fendler, Frederic Berger, Hervé Ribot *
Gilbert Lecarpentier, Joseph Macheda **

** CEA, LETI, MINATEC, F38054 Grenoble, France*
*** SET S.A.S. (Smart Equipment Technology), 131 Impasse Barteudet, 74490 Saint Jeoire, France*

Abstract

In order to increase the format of heterogeneous staring arrays to 2Kx2K pixels or even larger complexities, limited substrate size and cost reduction considerations make mandatory the reduction of the pixel size, but the mastering of ultra-fine pitch and high count flip chip bonding technology represents a challenge [1,4].

To overcome the planarity and thermal mismatch issues while reducing the bonding thermo-compression forces and the hybridization temperature, a new room-temperature insertion technology has been proposed and developed [2,3,4].This study gives first measured interconnection yield and serial access resistance of 2Kx2K, 10µm pitch hybridized arrays fabricated using this technique. A comparative study proves that parallelism during insertion is a key parameter. The micro-tube insertion technique is scalable to complexities of over four million connections, with pixel pitches down to 5µm. Hence, a derivative low temperature insertion concept could possibly be applied to 3D interstrata interconnections solving the cumulative high temperature cycles issues encountered when using more conventional high temperature processes.

1. Introduction

Two main families of flip-chip joining techniques (fig1a, fig1b) are commonly in use for the fabrication of heterogeneous imaging arrays [5].

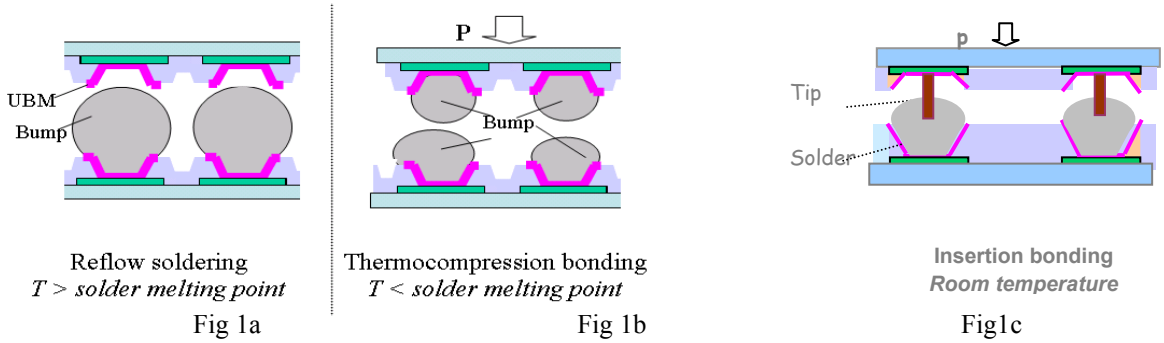


Fig 1a Fig 1b Fig1c

Fig. 1: Flip-chip techniques (imaging arrays)

When high pin count (i.e. 10k connections /mm2) and low pitch (i.e. <10µm) complexity is required, classical C4 type reflow soldering techniques (Fig. 1a) do not allow the balancing of chip planarity defects , leading to unconnected bumps. CTE (Coefficient of Thermal Expansion) mismatch can also be a major issue due to high solder reflow temperature (for heterogeneous materials the X, Y misregistration can approach pitch value at solder temperature)

Thermo-compression technique (Fig. 1b) can reduce planarity issues (using force and plastic deformation of solder bumps to compensate Z non-planarity), however high pressure levels are required and can induce local over-pressure defects or generate shorted bumps during thermo-compression. X,Y CTE mismatch is still a problem if compression temperature is set too high.

To solve these issues, a new "insertion" flip-chip technique (fig 1c) is proposed [2,4]: metallic tips are inserted in solder lands to perform ultrafine pitch (< 10 µm) and high bumps count (2000x2000) interconnections: it features a fluxless, low pressure, room temperature joining process well adapted to heterogeneous imaging arrays fabrication.

The present work gives the first electrical results obtained with that approach when using "micro-tubes" as the inserted tips [2].

2. Rational for micro-tube

In the beginning of this project [4] first insertion experiments were realized using plain cylindrical tips (Fig. 2). One of the conclusions of that work was that insertion forces would be too high for future higher complexities and that sharper tips geometry were mandatory.

In a first approximation we postulated that the insertion force would be roughly proportional to the insert cross-section area: then one idea was to build a "cylinder shaped" insertion tip to reduce the insertion force.

The insertion force for a tube-like shape can be approximated from the insertion force of a plain cylinder with the formula:

F tube = ~ F cylinder / (S cylinder r/ S tube)

With:

F tube= force to insert one tube into one solder land

F cylinder= force to insert one plain cylinder into one solder land

S cylinder= cross section area of one cylinder

S tube = cross section area of one tube

Numerical application of the formula demonstrates that insertion force could hopefully be divided by 10, thanks to the using of 4µm external diameter / 0.1µm thin micro-tube (compared to the insertion force required by a 4µm diameter plain cylinder).

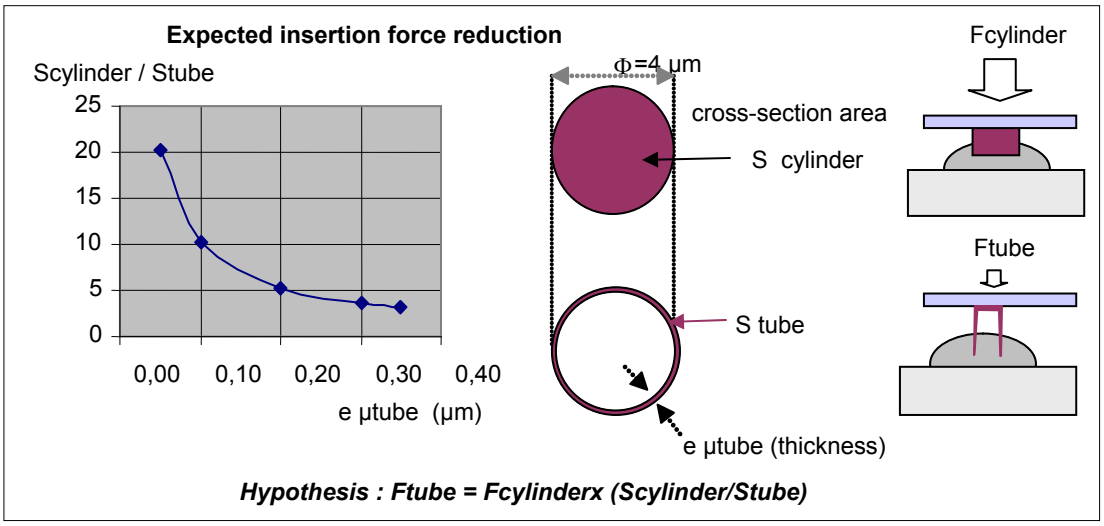


Fig. 2: Insertion force reduction

3. Process sketch

The following global process scenario was then developed: first, chip 1 is processed with soft solder lands (Fig. 3), then Chip 2 is processed with "insertion" tips/micro-tubes (Fig. 3), finally, after a classical alignment, the metallic micro-tubes arrays are inserted into solder lands arrays at low temperature and low pressure (Fig. 4)

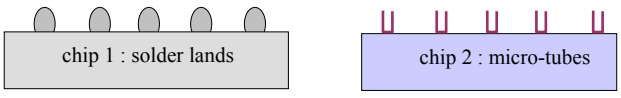


Fig. 3: chips preparation

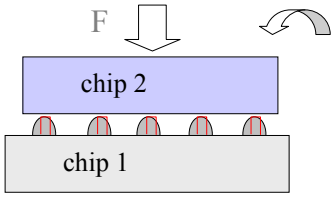


Fig. 4: chip joining (insertion)

Fluxless process: the gold plated micro-tubes break the native solder oxide film establishing an immediate electrical contact. No flux cleaning is required.

Low pressure process: thanks to the sharp micro-tubes geometry and high indium solder ductility, insertion forces are reduced (<0.5mN/connection) like the local overpressure. Applied forces can be handled by conventional flip chip bonding equipment even for very high pin counts (i.e: >4 million connections).

Room temperature process: CTE mismatch issues are suppressed; the bonding step can eventually be completed by solid-solid diffusion.

4. Processes development : solder lands and micro-tubes fabrication

Solder land fabrication results

The 4 millions indium solder lands at 10µm pitch were fabricated using a standard "lift-off" technique; solder lands were reflowed at 180°C for 1 minute (final solder reflow).

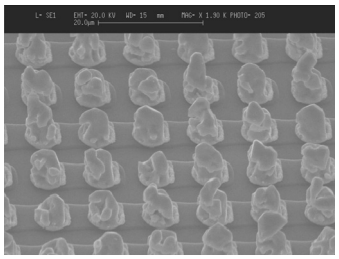
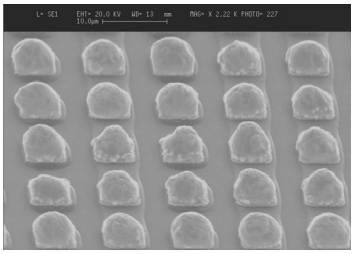
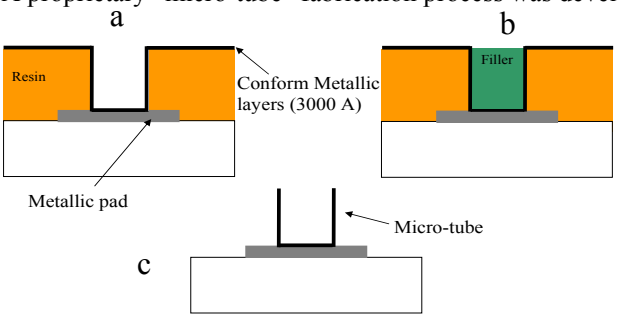
A: After liftoff  B: After reflow 

Fig. 5: SEM images of 10µm indium solder landss made by lift-off technique

Micro-tubes fabrication results

A proprietary "micro-tube" fabrication process was developed using conformal metal deposition and "gap fill" type processes.



First, a sacrificial polymer layer is spin-coated then etched over contact pads, µtube skin is then fabricated:

a- A metallic layer stack of 300nm total thickness is sputtered

b- The metal layer located inside vias is protected (thanks to a proprietary gap fill process)

c- The unprotected top metal layer is etched by RIE plasma, residual polymer inside vias is removed by plasma cleaning to complete micro-tube fabrication.

Fig. 6: Micro-tube process flow

The geometry (height, diameter) of the micro-cylinder are defined by the initial polymer photolithographic step, the micro-tubes skin thickness is controlled by the metal deposition parameters.

Test patterns with 1 to 8 µm tube diameters were fabricated for full process capability evaluation; however, electrical evaluation was limited to 4µm diameter tubes.

Arrays of 4-million micro-tubes with 10µm pitch were processed with excellent yield and uniformity.

Fig. 7 shows different micro-tubes diameters, between 2.5-2.8 µm heights, aligned on 6x6µm² metallic pads.

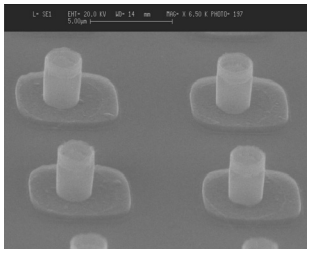
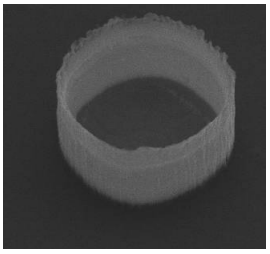
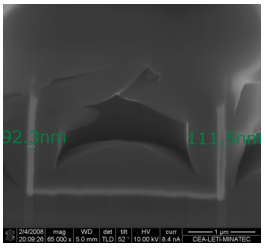
7a  7b  7c 

Fig. 7: Micro-tubes fabrication results (a, b: SEM top views, c: Micro-tube's FIB cross section)

The final vertical skin thickness was measured at 100 nm on 4µm diameter tubes (Fig. 7c).

5. Flip chip by insertion: process development

As-built chips were readily assembled by insertion with 0.5mN applied load per connection, this resumes to 2kN applied load per chip for 4. 10^6 total vertical connections. First electrical results showed that parallelism during insertion was a critical parameter.

Next section evaluates how parallelism control during insertion can influence connection yield

Parallelism control

A room temperature, low force assembly process was developed using a commercial SET FC300 type machine. Two types of chip to chip parallelism control were compared in this study (Fig. 8-9).

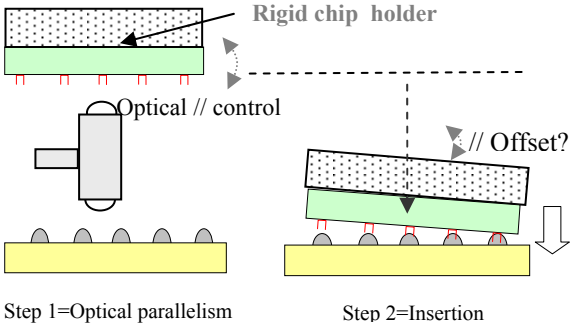


Fig. 8: parallelism without auto-levelling

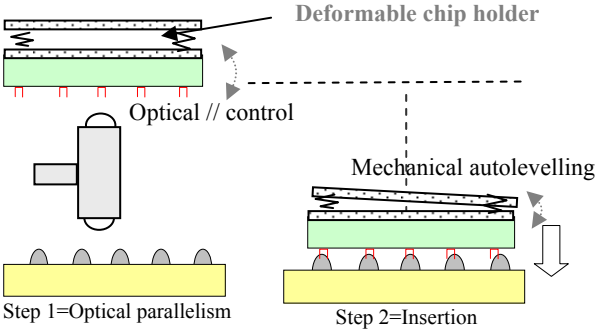


Fig. 9: parallelism aided by mechanical auto-levelling

Type 1- Pure optical parallelism (Fig. 8): upper chip is held by a rigid (flat) holder tool, chips parallelism is tuned prior to thermo-compression thanks to the integrated optical autocollimator. Parasitic parallelism offset can occur between alignment position (separated chips) and insertion position (chips in contact).

Type 2- Optical parallelism + Mechanical Auto-levelling (Fig 9): upper chip is held by a specific "auto-levelling holder tool" which deforms under applied load. Optical parallelism is still performed in upper position (same as 1) but, during the insertion step, the autolevelling tool can deform mechanically if load proves to be non uniform. This tool allows to spread an uniform load (i.e.: recovering parallelism) between mated chips surfaces while preventing X, Y in-plane misalignment.

The two parallelism principles were evaluated and compared on two hybridized chips using the SET FC300 ® bonder in thermo-compression configuration for the same 2kN insertion load (i.e. 0.5mN/connection). The alignment capability of the bonder is a primordial parameter and pre-measured misalignment proved to be less than ± 0.5 µm at the 2kN compression force required in our application, chip parallelism was pre-tuned in alignment position thanks to the built in autocollimator (spot diameter 8mm , pre-leveling accuracy of 25µrad).

6. Electrical results :

Test vehicle

The 20x20mm arrays are hybridized using chips processed with 4 µm diameter micro-tubes. Daisy chains are implemented on chips (Fig. 10) and make possible to compute either serial resistance access per connection or local defectivity yield : open and short circuits percentage are statistically calculated by a 2.56 % sampling of all connections (102312 connections are tested out of a total of 4. 10^6 total connections).

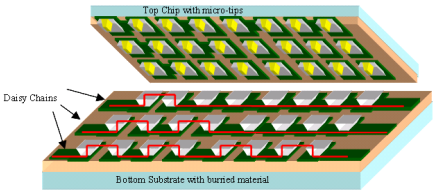


Fig. 10 Daisy Chain Test Vehicle

Test results

Connection resistance

The vertical access resistance (including contacts resistance and serial resistance) is calculated from the measurement of a large number of uniformly spread daisy chains with 2, 20 or 100 connections.

The access resistance value is directly derived from the slope of the regression line obtained when plotting the chains serial resistance versus the number of connection of the chain (Fig. 11)

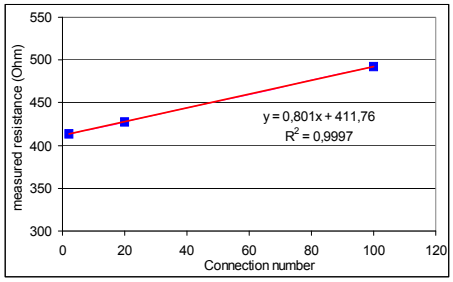


Fig. 11: serial access resistance

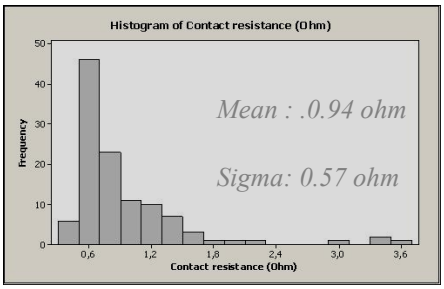
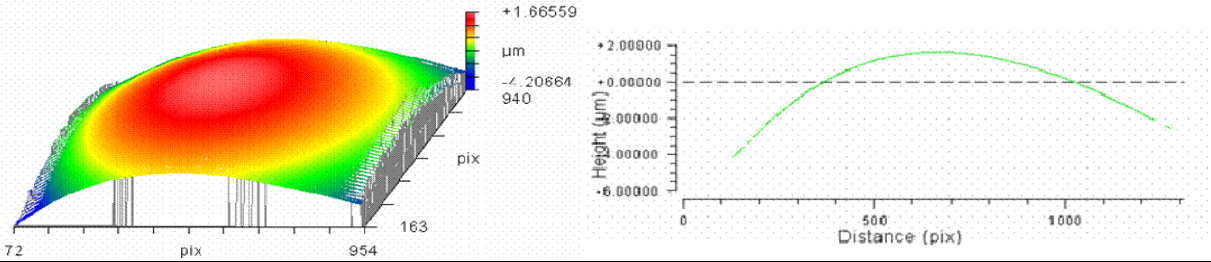


Fig. 12: serial access resistance histogram

Yield comparison (with or without autolevel):

Planarity measurements

With conventional hybridization techniques (i.e.: reflow soldering and bump to bump thermocompression), the non planarity of the chips before hybridization is a key parameter strongly impacting connection yield, the processed faces (indium lands and micro-tubes faces) need to be fully characterized before joining. Both chips were measured convex and the maximum out of plane face to face value "deltaZ" was extracted from Zygo measurement's data (Table. 1).



Experiment 1 DeltaZ		Experiment 2 Delta Z
8.3µm	Micro-tube face Indium solder face DeltaZ	8.1µm

Table. 1: out of plane deltaZ

Notice that such out of plane large values (>8µm) would have render "hybridization by reflow" technique (fig. 1) physically impossible (reflow technique does not allow to reduce warping by pressure).

Yield mapping

Each chip is divided into 60 sectors. The yield is calculated using the numbers of closed daisy chain in each sector.

Using a statistic method, we can plot the hybridization yield (Fig.13).

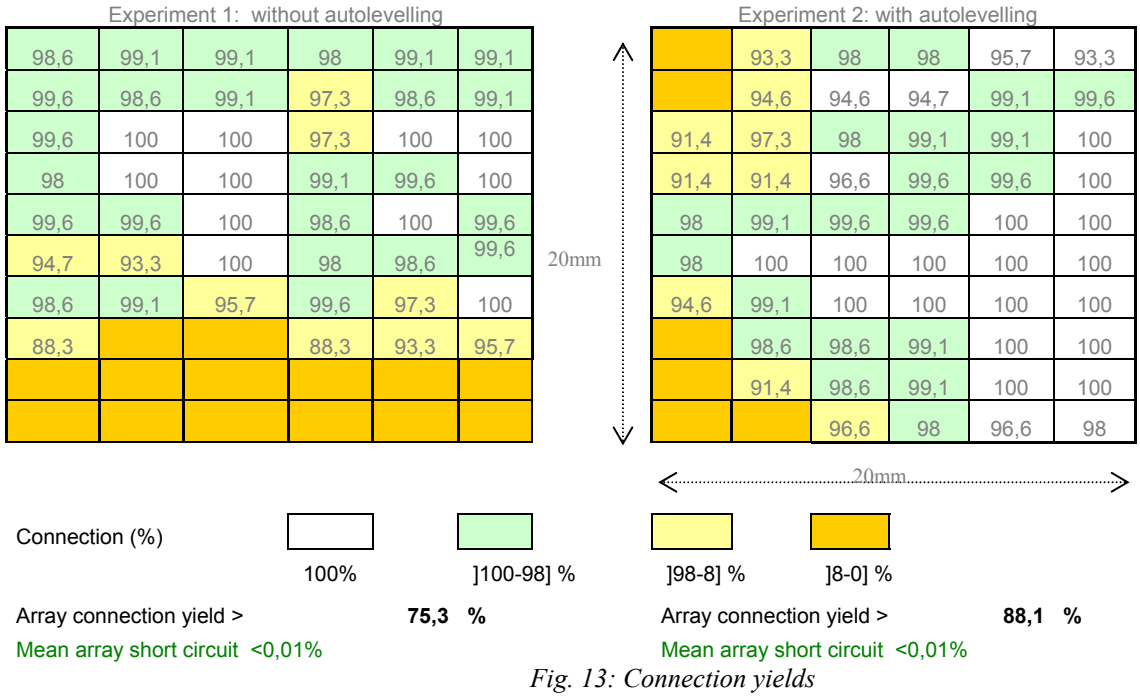


Fig. 13: Connection yields

7. Discussion

Results obtained in this work (using 4µm diameter micro-tubes) are compared with previous results obtained using 4 µm diameter plain cylinder insertion [3].

Table 2 : micro-tubes versus cylinder insertion

	Micro-tube insertion	Cylinder insertion	Gain
Insertion force (per connection)	0.5 mN	3.6 mN	7.2
Insertion T°	Room temperature	80°C	
Vertical access resistance (per connection)	0.94 Ω	7.4 Ω	7.9

Insertion force: the 7.2 fold reduction of insertion force agrees with the 10 fold initial extrapolation (fig2): standard thermocompression machines can be used for 2K*2K array insertion.

Access resistance: the mean access resistance per connection is measured at 0.94 ohms/connection (with a standard deviation of 0.57 ohms across the 20*20mm array), this is a reduction by 7.9 compared to plain cylinder insertion [3]. It can be partly explained by a larger contact surface between the tube and the solder (2 faces contact) and secondly by the different mechanical plastic deformations behavior shown by SEM analysis.

Yield discussion

1 No short circuit between adjacent connections are measured throughout the whole hybridized arrays: this demonstrate the advantages of the insertion technique over indium/indium thermo-compression technique

2 The connection yield (open circuit) is encouraging for a first experiment and, regarding the large unfavorable "out of plane" non-planarity, demonstrates the advantages of the insertion technique over pure reflow technique (note that that reflow technique would have shown many open circuits with the same initial non-planarity conditions).

Finally it is shown (fig.13) that the implementation of an autolevelling tool significantly enhances the global connection yield (from 75.3% to 88.1%).

8. Conclusion

A low temperature, low pressure flip-chip process has been developed and proved feasible using two different insertion scenarii, connection yield has been measured on first 2K*2K hybridized arrays.

We demonstrated a connection density of 10k connections /mm2 with a mean Z connection serial resistance of 0.94 ohm (σ = 0.57 ohm) per 100μm^2. First yield evaluation show 88.1% connection yield and 0 % short circuit between connections, these results are encouraging despite the large unfavorable 8µm out of plane chips non-planarity (either reflow or thermocompression techniques would have been ineffective with such conditions).

Finally, two room temperature insertion processes have been compared and show significant connection yield enhancement when using a specific "autolevelling" holder tool.

9. Future work

First, connection yield has to be improved and to be fully distributed over the 20x20mm chip, second no specific temperature baking were performed after room temperature insertion to complete intermetallic formation and to improve contact resistance: these topics will be part of our next work for imaging applications

Applying this technology to other application is also part of our objectives and, provided the choice of a new metallurgical configuration is made (solder type, tube type, etc…), a derivative low temperature insertion concept could possibly be applied to 3D interstratas interconnections : this opportunity is also under evaluation.

Acknowledgments

This work was supported by CEA-LETI, Minatec and Carnot funding, thanks to Frederic Humbert (SET) for his assistance during this work.

References

[1]: L. Kozlowski Progress in Ultra-Low Noise Hybrid and Monolithic FPAs for Visible and Infrared- Astrophysics and Space -Science Library- vol. 300 pp123-130

[2]: D. Saint-Patrice, F. Marion et al. New Reflow Soldering and Tip in Buried Box (TB2) Techniques For Ultrafine Pitch Megapixels Imaging Array Proceedings ECTC Orlando FL2008 pp 46-53

[3]: C. Davoine, M. Fendler, F. Marion, "Low temperature F/C technology for fine pitch bonding", Proc of ECTC San Diego, 2006, p 24-28

[4]: C. Davoine,''Densification des connexions flip-chip grande surface'', M.S. thesis, CEA-LETI, MINATEC, Grenoble, France, 2006.

[5]: G.Humpston, D. Jacobson Principles of soldering pp 199-203 Ed ASM International The material Information Society