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Interconnect and bonding techniques for pixelated X-ray and gamma-ray detectors

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ABSTRACT: In the last decade, the Detector Development Group at the Technology Department of the Science and Technology Facilities Council (STFC), U.K., established a variety of fabrication and bonding techniques to build pixelated X-ray and γ -ray detector systems such as the spectroscopic X-ray imaging detector HEXITEC [1]. The fabrication and bonding of such devices comprises a range of processes including material surface preparation, photolithography, stencil printing, flip-chip and wire bonding of detectors to application-specific integrated circuits (ASIC). This paper presents interconnect and bonding techniques used in the fabrication chain for pixelated detectors assembled at STFC. For this purpose, detector dies ($\sim 20 \times 20 \text{ mm}^2$) of high quality, single crystal semiconductors, such as cadmium zinc telluride (CZT) are cut to the required thickness (up to 5mm). The die surfaces are lapped and polished to a mirror-finish and then individually processed by electroless gold deposition combined with photolithography to form 74×74 arrays of $200 \mu\text{m} \times 200 \mu\text{m}$ pixels with $250 \mu\text{m}$ pitch. Owing to a lack of availability of CZT wafers, lithography is commonly carried out on individual detector dies which represents a significant technical challenge as the edge of the pixel array and the surrounding guard band lies close to the physical edge of the crystal. Further, such detector dies are flip-chip bonded to readout ASIC using low-temperature curing silver-loaded epoxy so that the stress between the bonded detector die and the ASIC is minimized. In addition, this reduces crystalline modifications of the detector die that occur at temperature greater than 150°C and have adverse effects on the detector performance. To allow smaller pitch detectors to be bonded, STFC has also developed a compression cold-weld indium bump bonding technique utilising bumps formed by a photolithographic lift-off technique.

KEYWORDS: X-ray detectors; Detector design and construction technologies and materials; Gamma detectors (scintillators, CZT, HPG, HgI etc); Manufacturing

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1 Introduction

A wide range of techniques for integrated circuit packaging, assembly and interconnections is commonly used for electronics worldwide [2]. Interconnect and bonding techniques are also useful for X-/ γ -ray detectors systems, in order to achieve low-noise configurations for flip-chip-bonding radiation sensors directly to the ASICs [3]. The Technology Department of the Rutherford Appleton Laboratory established a variety of these sensor fabrication and bonding techniques. These are used for pixelated X-/ γ -ray detectors such as in the HEXITEC imaging and spectroscopy system [1]. The techniques comprise: a) die cutting and polishing for sensor preparation from raw material, b) photolithography for pixelation, c) bonding techniques such as stencil printing, flip-chip bonding, cold-weld indium (In) bump bonding, and wire bonding.

For the HEXITEC system, individual detector dies ($\sim 20 \times 20 \text{ mm}^2$) are prepared from raw material such as cadmium zinc telluride (CZT). Processes such as photolithography and stencil printing are performed on single dies because of the lack of commercially available high quality CZT wafers. In order to reduce stress and to minimize adverse effects such as crystalline modifications in the detector, each die is bonded at low temperatures ($\leq 45^\circ\text{C}$) to an application-specific integrated circuit (ASIC) and a printed circuit board (PCB) module which allows mounting and de-mounting of the detector to the data-acquisition system. The pixel array of HEXITEC has a typical pitch of $250 \mu\text{m}$. For smaller pitch and pixel size, indium bump bonding is used. These techniques and the assembly facility are also extensively used for the Large Pixel Detector (LPD) designed for XFEL at DESY [4].

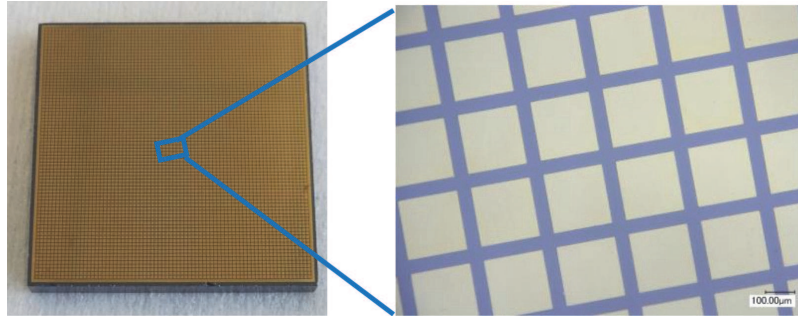


Figure 1. Pixelated CZT detector die after lithography (left); array of pixels on die (inset on the right).

2 Detector die preparation

2.1 Die cutting and surface preparation

The HEXITEC detector was designed for detection of hard X-rays (> 30 keV) using thick high-Z materials like cadmium telluride and CZT. In order to prepare thick detector sensors, individual dies are cut to customized thickness (1–5 mm) with the *LOGITECH AWS1* wire saw using a 0.3 mm diamond-coated wire. Subsequently the detector die's surfaces are lapped and polished using the *LOGITECH PM5*. In order to achieve a mirror-like surface finish, Al_2O_3 slurry with grain size down to $0.05 \mu\text{m}$ is used. For CZT a typical RMS surface roughness (R_q) of $29 \pm 6 \text{ \AA}$ is achieved by pure mechanical polishing. Chemo-mechanical polishing with bromine in methanol can also be carried out in our laboratory but in our experience it degrades the surface roughness of CZT ($R_q \cong 80 \pm 10 \text{ \AA}$). Subsequently the CZT surface is gold coated using an electroless process with a gold chloride solution [5]. This is carried out either after the polishing process or after the lithography depending on the subsequent photoresist used. The gold-coated CZT surface roughness is $R_q \cong 111 \text{ \AA}$.

2.2 Lithography and detector pixelation

Photolithography is carried out in-house to create 74×74 array of $200 \times 200 \mu\text{m}^2$ pixels with $250 \mu\text{m}$ pitch on polished dies for the HEXITEC detector (figure 1). An ISO 5 clean room facility equipped with spin coaters (*Laurell* and *Suss Gyrset*) and a mask aligner (*Suss MA6*) allows the pixelation of individual detector chips ($\sim 20 \times 20 \text{ mm}^2$). The pixelation is carried out using either a lift-off process or an etching process. For the lift-off, the electroless gold coating is carried out after the photoresist patterning and the resist is then stripped leaving the desired pixel array. Alternatively, an already gold-coated CZT die can be patterned with SU-8 photoresist which is inert to a vast number of chemicals so that exposed areas of unprotected gold can subsequently be chemically etched. For the metallization of polished CZT surfaces, an electroless gold deposition process is used as described before [5].

3 Detector/ASIC bonding

For assembling a complete detector, a customized pixelated detector die has to be bonded to an ASIC readout chip (e.g. to an in-house designed HEXTEC 80×80 ASIC [1]). Prior to bonding,

gold studs are put on the contact pixels of the ASIC using the *Palomar P8000* wafer bonder or *Questar 2119* ball bonder. Gold balls are typically deposited at room temperature on the ASIC; however, the bonding systems also allow the forming of gold balls at 150 °C. The *SET FC150* flip-chip bonder is employed for joining the detector and studded ASIC after conductive epoxy is printed on the detector pixel array. Indium bump bond can be used as an alternative on Si or GaAs sensors with a smaller pixel pitch.

3.1 Conductive epoxy bonding

An array of silver(Ag)-loaded epoxy dots is printed in good alignment to the detector pixels (250 μm pitch) with a custom-built manual stencil printer. The typical height of printed Ag epoxy dots is $30 \mu\text{m} \pm 10 \mu\text{m}$ standard deviation (σ) and the diameter is $136 \mu\text{m}$ ($\sigma \cong 10 \mu\text{m}$) (figure 2a). Subsequently the detector is transferred to the *SET FC150* flip-chip bonder ($\pm 0.5 \mu\text{m}$ placement accuracy and $\pm 1 \mu\text{m}$ post-bond accuracy). When the die is aligned to the studded ASIC, low pressure ($\sim 0.8 \text{ mN/bump}$) is applied to bond the detector/ASIC at 30°C. The assembled detector/ASIC with the Ag-loaded epoxy can then be cured on the flip-chip bonder but usually it is cured in an oven at a low temperature (45 °C) for a long period. Use of low bonding and curing temperatures reduces the stress between the detector and the ASIC which is a common issue for bonding materials with different thermal expansion coefficients at high temperatures. In addition, excessive bonding temperatures can lead to modifications of the crystal structure that have a detrimental effect on detector performance. Regardless of the substantial height variation of the printed Ag dots, the final bonds in a cured and bonded detector/ASIC assembly have a uniform height of $43.5 \mu\text{m}$ ($\sigma \cong 1 \mu\text{m}$) and a diameter of $153 \mu\text{m}$ ($\sigma \cong 4.5 \mu\text{m}$). Figure 2b shows a profile image of a bonded test structure (figure 2c) which consists of a studded ASIC bonded to a quartz plate using a printed array of Ag dots similar to that shown in figure 2a. The profile in figure 2b is viewed with an optical profiler through the transparent quartz. Several weeks after bonding and curing, a shear test was carried out on the test structure. The quartz plate was sheared off the ASIC with a force of 517 N; this correlates to approximately 94.4 mN/bond. The fracture always occurred between stud and apex of a silver dot. This mechanical test also indicated that all Ag dots formed a bond with a stud. However, tests of real detector devices in spectroscopic operation show that in average only 2 pixels out of an array with 6400 pixels had no proper electric contact. This is a bond yield better than 99.9%.

3.2 Cold-weld indium bump bonding

As an alternative to the conductive epoxy bonding and for a pixel size smaller than $200 \times 200 \mu\text{m}^2$, In bumps can be deposit on pixelated detectors and ASICs using a vacuum evaporation technique. In particular, this is suitable for Si or GaAs detectors. Heights of In bumps up to 12 μm are potentially achievable using the *MPS 800 (JSL Design Ltd.)* indium evaporator and a lift-off process. A typical resist profile suitable for the lift-off is shown in figure 3. Here the total resist height is $\sim 12.8 \mu\text{m}$ and the profile has a re-entrant sidewall $\sim 130^\circ$ down from the top to approximately the middle of the resist cross-section. An intentional undercut of $\sim 7 \mu\text{m}$ appears for the remaining 6.4 μm of resist towards the substrate. This facilitates the lift-off process after the resist cavities are filled with indium. Under-bump metallization with a chromium layer was carried out beforehand. Typical $\sim 6.5 \mu\text{m}$ high In bumps on contact pads are shown in figure 3b. No reflow process was

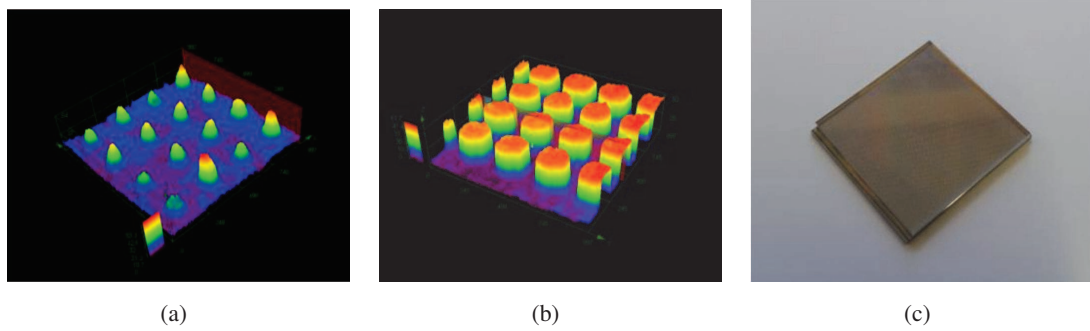


Figure 2. (a) Typical height profile of stencil printed Ag dots; (b) uniform profile of Ag dots printed onto a quartz plate and bonded to a studded ASIC; (c) photo of the bonded quartz plate/ASIC test structure.

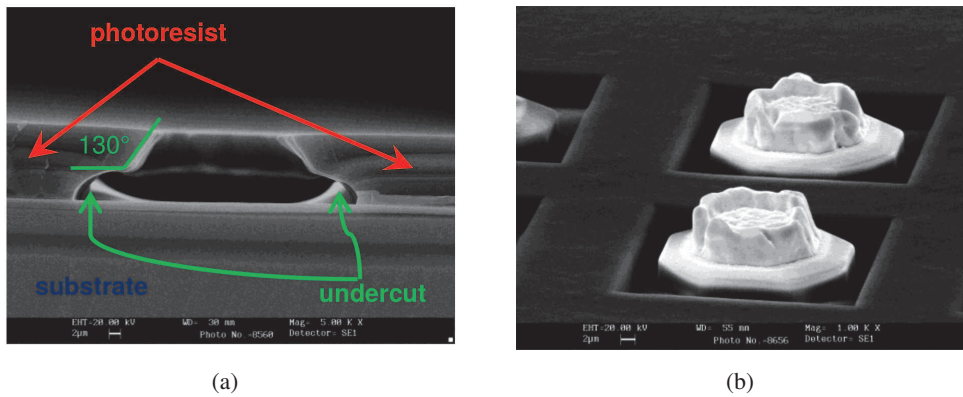


Figure 3. (a) SEM image of a typical cross-section through a negative photoresist used for the In bump lift-off; (b) typical $6.5 \sim \mu\text{m}$ high In bumps on contact pads.

used here. STFC has facilities and equipment to perform reflow processes but this reflow step was omitted here for process simplification. The In bumps (figure 3b) formed on both the detector and the ASIC are then flip-chip-bonded with the application of $<1 \text{ g}$ per bump using the *SET FC150* and similar bonding conditions as for the bonding with conductive epoxy.

4 Wire-bonding and assembly

After the flip-chip bonding of a detector with an ASIC, a *Hesse & Knipps Bondjet 715M* ultrasonic wedge bonder is used to contact the ASIC pads with a PCB module which allows mounting and demounting of the detector to the data-acquisition system. This module is typically glued to an aluminium block that facilitates detector handling during wire bonding and that also allows joining a number (n) of detector/ASIC modules together in a large array of $(1 \times n)$ or $(2 \times n)$ detectors [6].

5 Summary and outlook

STFC successfully fabricates pixelated spectroscopic X-/ γ -ray imaging detector systems using a chain of fabrication and bonding processes. These processes include photolithography on single small dies ($20 \times 20 \text{ mm}^2$) with patterns up to the edge of the die. Furthermore, the subsequent

bonding of a die to an ASIC can be carried out at low temperatures $\leq 45^\circ\text{C}$ with stencil-printed silver-loaded epoxy glue dots so that residual stress between the detector die and ASIC is minimized. Typically a 74×74 array of $200\times 200\ \mu\text{m}^2$ pixel on $250\ \mu\text{m}$ pitch can be achieved on such detectors. In addition, for smaller pixel sizes, STFC has established a cold-weld indium bump bonding process. The fabrication of these detectors from a single die is an important first step towards the tiling of detectors into larger arrays [6].

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